OIF-28G-VSR Channel Simulations

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Introduction

- Considerable effort was spent refining the OIF-28G-VSR link budget to meet the VSR project goal of "*enabling smaller and lower power 100G optical modules*".
  - Link simulation results were contributed by various companies
  - Unfortunately access to these contributions is only available to OIF members.
  - As one of those companies, Inphi wants to open up it's simulation results to the wider 802.3bj audience
- Inphi presented a succession of increasingly refined VSR channel simulations to the OIF
  - This contribution contains Inphi's final simulation results and our rationale for supporting a 10dB link Budget for VSR
    - Original OIF contribution is oif2010.245.08
  - We believe these results are relevant to CAUI-4 discussions

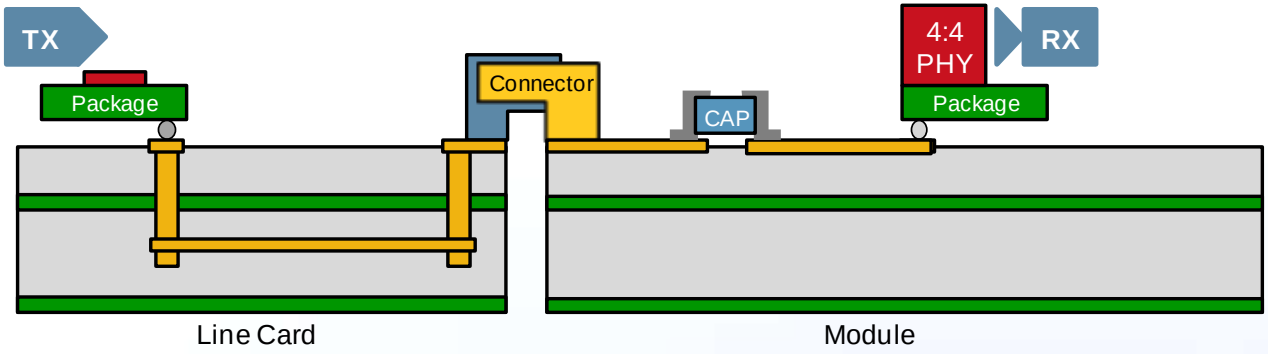
Overview

- OIF-28G-VSR Project Statement
  - A narrow chip-to-module interface is needed to enable smaller and lower power 100G optical modules.
- CTLE Receiver equalization is inherently lower power than DFE equalization
  - Choosing a channel loss budget compatible with CTLE equalization addresses VSR project goal
- In this presentation we show simulation results that explore the practical limits of CTLE equalization

Simulation Update – April 2011

- Differences from previous simulations :
  1. Used Persidio caps (0502, 0.1uF) in the module
  2. Eliminated the vias in the module
  3. No XTALK aggressors
  4. Tx peak amplitude reduced to 600mVppd instead of 800mVppd
  5. Reporting eye height and eye widths to 1E-15 BER instead of 1E-12

Channel model



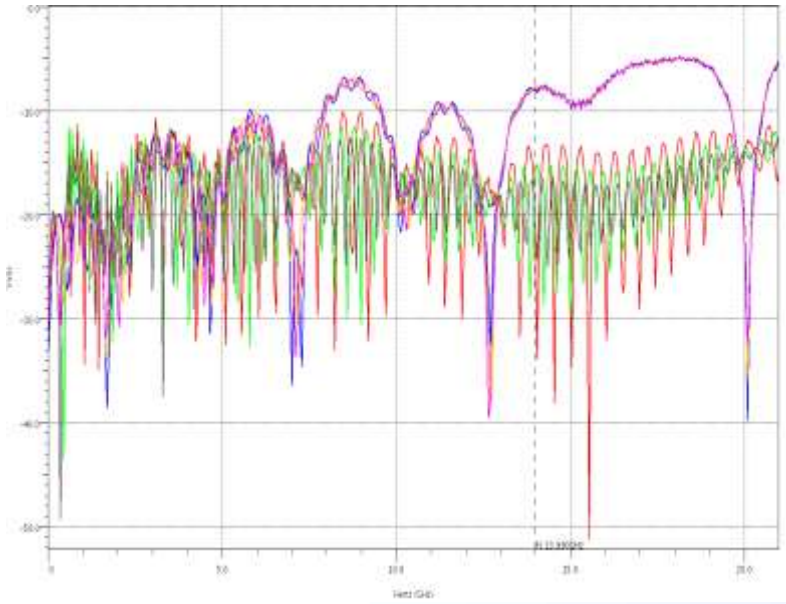
- In addition to the Quattro2 Connector the Channel consists of :
  - Back-drilled vias in the line card.
  - Line Card Trace lengths beyond 4” were simulated to determine where the CTLE approach would break down
  - Module routing (0.5” micro-strip + AC coupling cap + 0.5” micro-strip
- Gearbox and Retimer package models are also included in the simulation
- No crosstalk was included

Channels

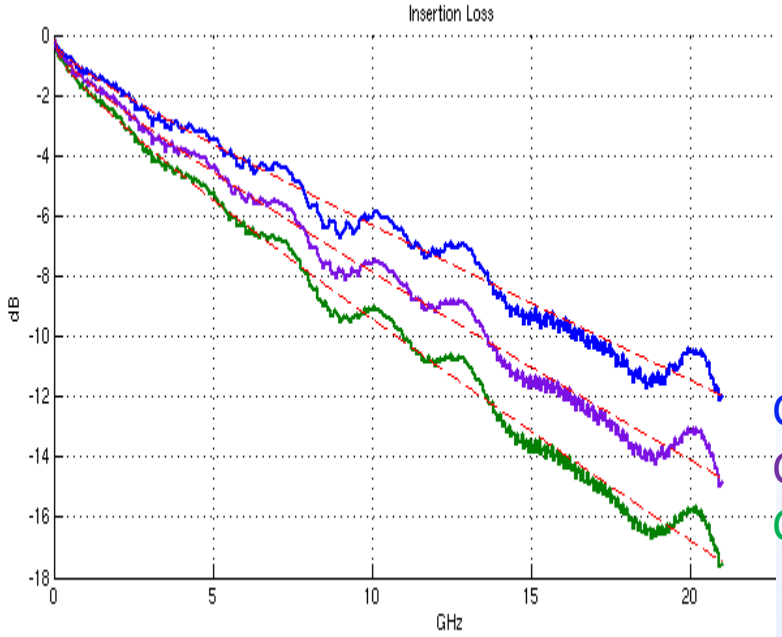
- 3 channels compared
  - 3 channel losses : 8, 10, and 12dB
- Channels are labelled as Cxx
  - xx = average channel loss at Nyquist (14GHz) in dB
- Channel consists of :
  - Back-drilled vias in the line card.
  - Line Card trace lengths beyond 4” were simulated to determine where the CTLE approach would break down
  - Quattro2 connector
  - Module routing (0.5” micro-strip + AC coupling cap + 0.5” micro-strip)

Channel insertion and return loss (dB)

SDD11, SDD22



SDD21



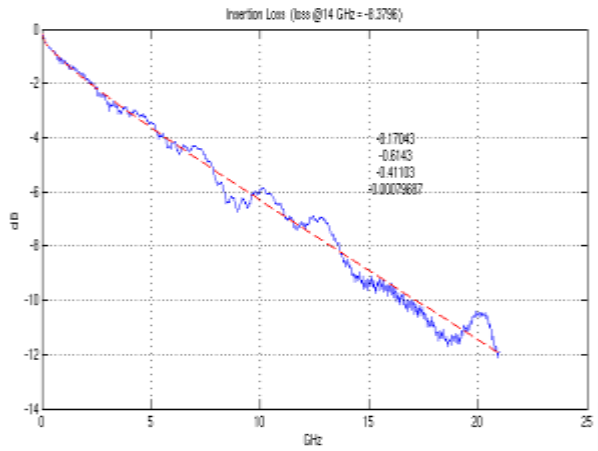
- The channel loss does NOT include package loss, however the Time domain/Statistical simulation include package model and non-ideal Rx/Tx termination

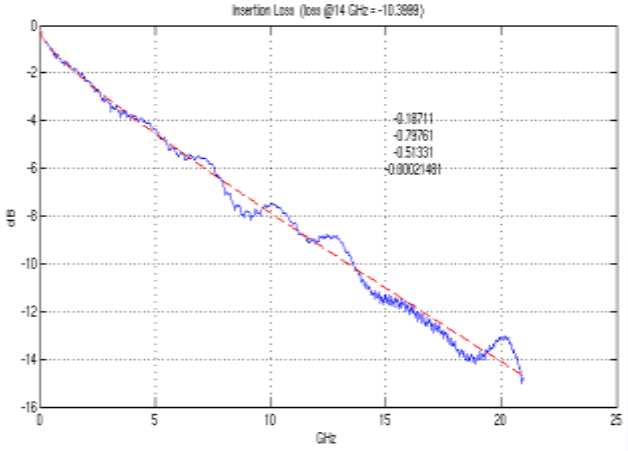
ILfit and ILD

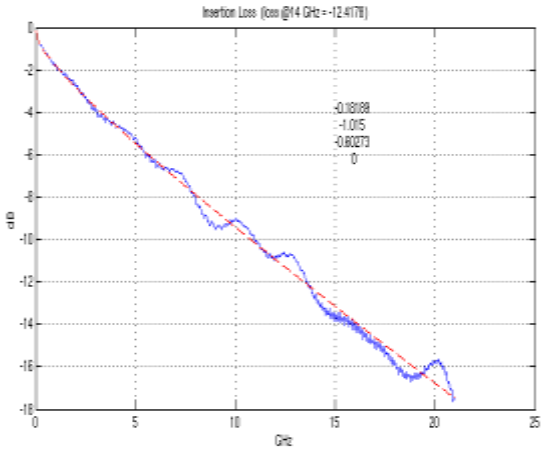
C08 (loss=8.4dB)
a=[-0.17 -0.61 0.4 0.0008]

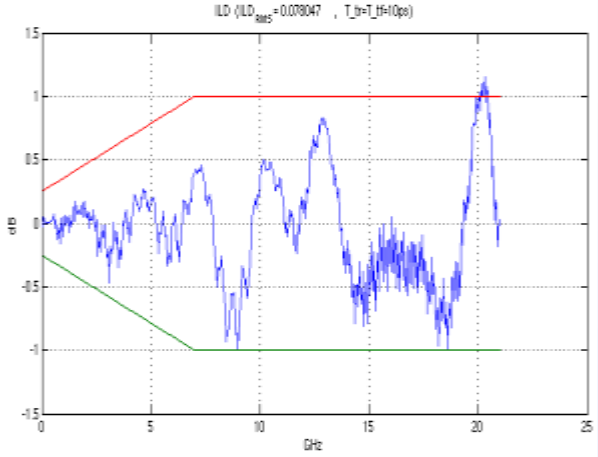
C10 (loss=10.4dB)
a=[-0.19 -0.79 -0.51 -0.0002]

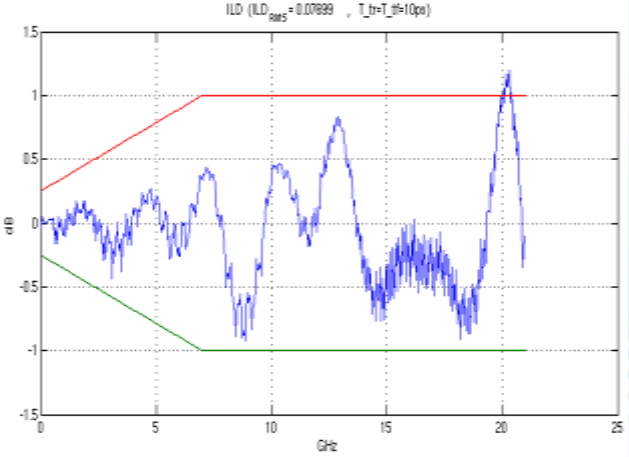
C12(loss=12.4dB)
a=[-0.18 -1.01 -0.6 0]

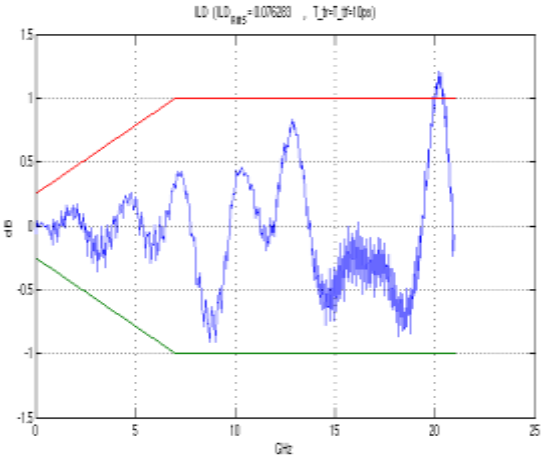




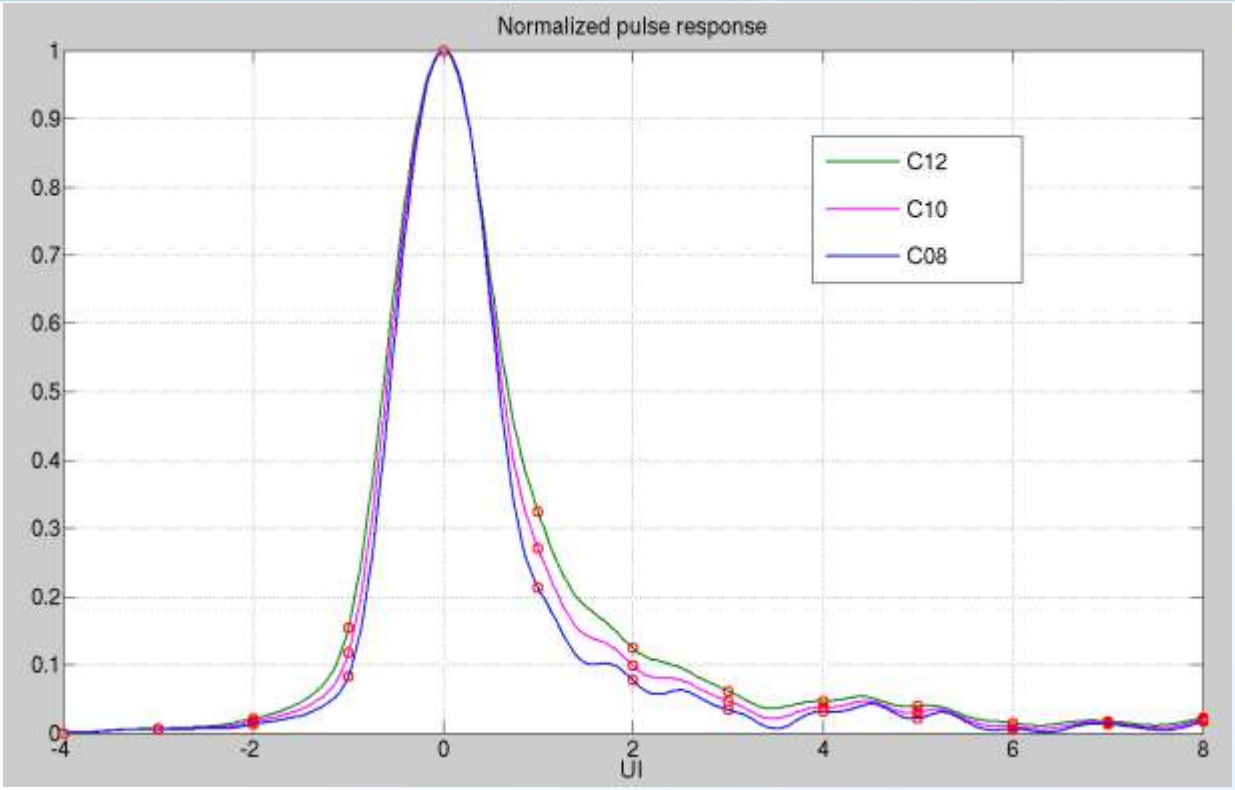








Normalized Channel Pulse Response



- The pulse response of the channel shows sizable precursor ISI
  - CTLE cannot equalize precursor ISI
  - TX FIR with 5-10% precursor weight is needed to equalize precursor ISI

Equalization & Modeling

- Continuous time Linear Equalization (CTLE) at the receiver with finite granularity
  - Discrete set of fixed equalizer settings
  - Parasitic poles are modelled to achieve practical finite bandwidth
  - Adaptive equalizer
- Chip impairment such as non-50 ohm termination and reactive loading are also modeled (i.e., RX/TX mismatch)
- Receiver input referred noise as well as the random jitter of the transmit and recovered clock are also modeled
- Results with and without TX pre-emphasis are presented
- Time domain simulations with extrapolation to 1E-15 BER
- Tx output includes both Rj and Dj

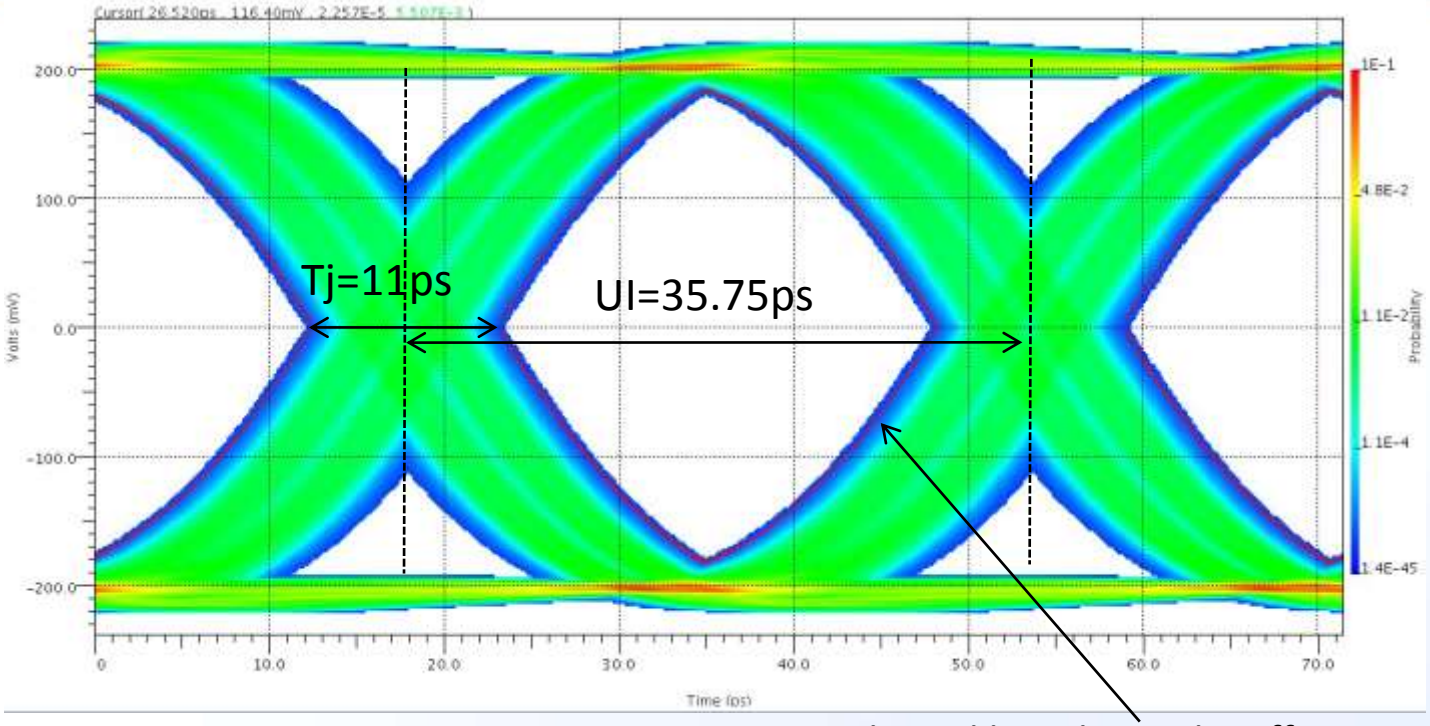
Non-idealities

- There are several non-idealities that limit the performance of an equalizer
  - Package loss and discontinuity
  - Transmitter finite rise and fall time as well as jitter (Dj, Rj)
  - Non-perfect 50-ohm termination for Rx and Tx as well as discontinuity between different components of the channel
  - Receiver noise
  - Parasitic poles of the Receiver/equalizer components
  - Cross talk
- On top of the above non-idealities the retimer has practical limitations:
  - Uncorrelated Dj between Rx data and Recovered Clock
  - Rj of the Recovered Clock
  - DCD and other imperfections in the retimer and recovered clock
  - Non-zero setup and hold time

Simulations with non-idealities

- All non-idealities listed in the previous slide are included in the Equalizer model used in our simulations
- The uncorrelated Dj between Rx data and recovered clock is modeled by plotting the equalized eye vs. recovered clock
  - No other non-idealities of the retimer are modeled.
- Time domain simulation for 2M bits using PRBS21 pattern + statistical extrapolation to 1E-15

Transmit Eye at Package Output (Based on 28G-SR Specification)

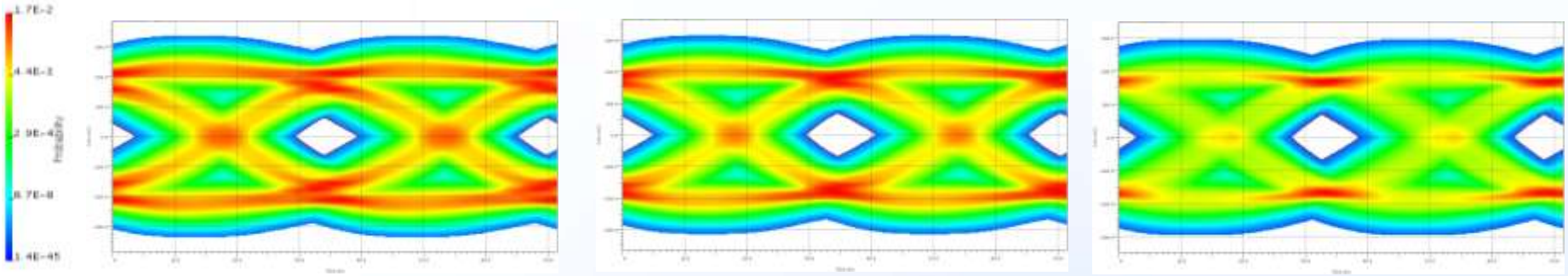


The red line shows the effective eye opening for 1E-15 BER (i.e., 1E-15 contour)

- Data Rate=27.95Gb/s ⇒ UI=35.75ps
- Tj (1E-15 BER) = 11ps
- Rj (1E-15 BER) = 5.1ps
- Color gradients are used to show eye contours for different probabilities

C08

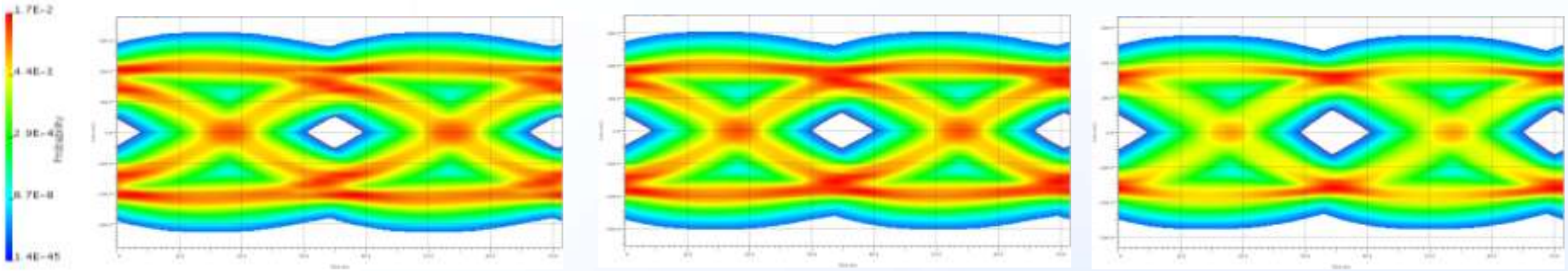
C08	No TX EQ			5% TX precursor			10% TX precursor	
Eye Width @ IE-15:	10.2	ps		11.3	ps		11.0	ps
Eye Height @ 1E-15:	127	mv		140	mv		134	mv



- 5% weight on TX pre-cursor tap increases the eye width by more than 1ps
- 5% is an optimal value and increasing the pre-cursor weight to 10% degrades both eye width and eye height

C10

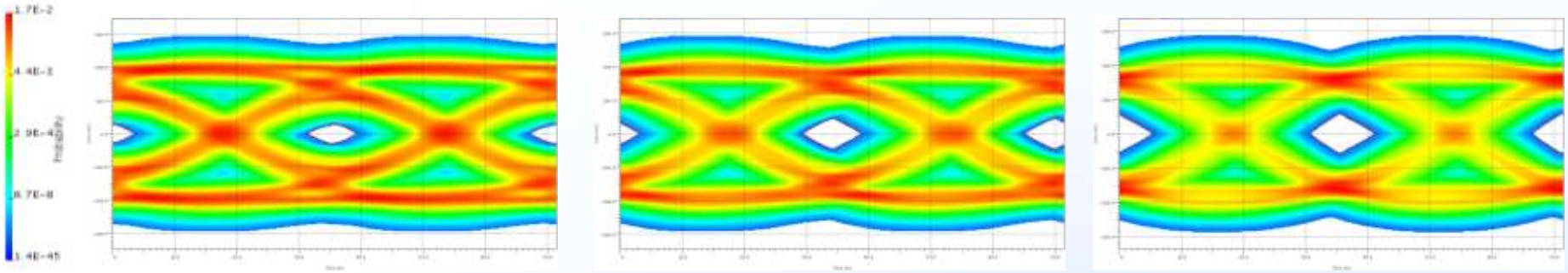
C10	No TX EQ			5% TX precursor			10% TX precursor	
Eye Width @ IE-15:	9.2	ps		10.3	ps		11.3	ps
Eye Height @ 1E-15:	108	mv		113	mv		131	mv



- 5% weight on TX pre-cursor tap increases the eye width by more than 1ps
- 10% weight on TX pre-cursor increases the eye width by another 1ps and also increases the eye height to 131mV

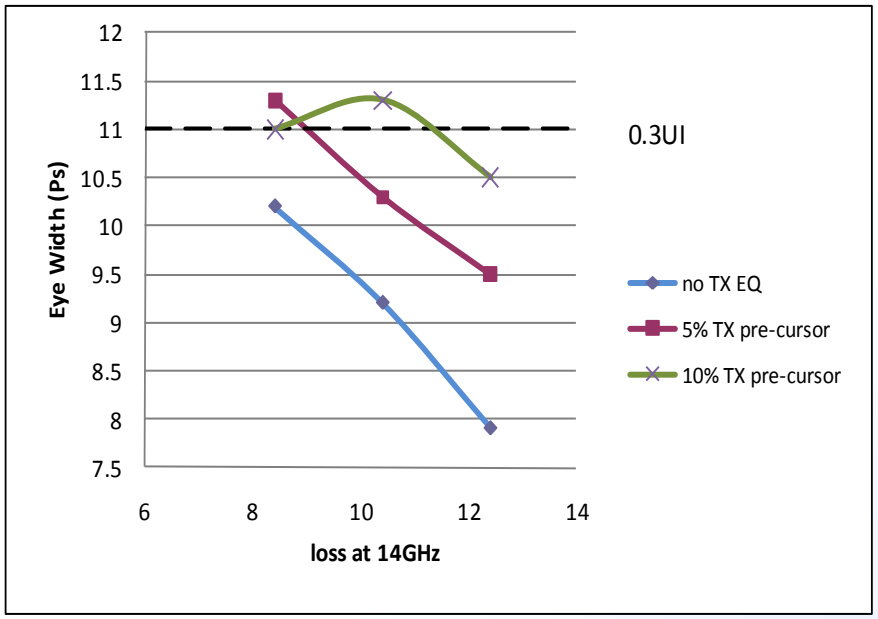
C12

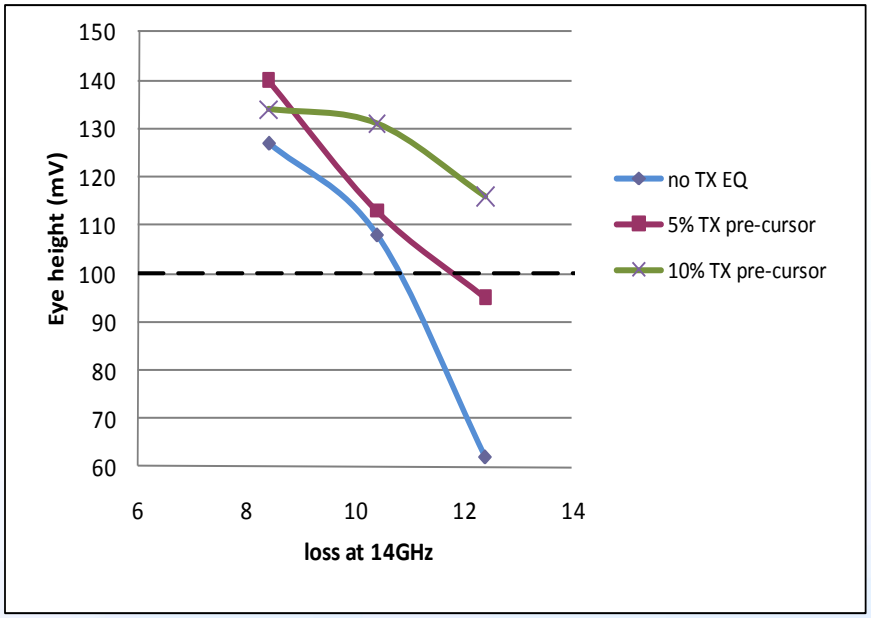
C12	No TX EQ			5% TX precursor			10% TX precursor	
Eye Width @ IE-15:	7.9	ps		9.5	ps		10.5	ps
Eye Height @ 1E-15:	62	mv		95	mv		116	mv



- 5% weight on TX pre-cursor tap increases the eye width by more than 1.4ps
- 10% weight on TX pre-cursor increases the eye width by another 1ps and also increases the eye height to 116mV

Channel sim summary
Eye width and Eye Height at 1E-15





- 5% Tx pre-cursor has the same effect on eye width as reducing the channel loss by ~2dB
- 10 and 12dB channels require 10% TX pre-cursor weight

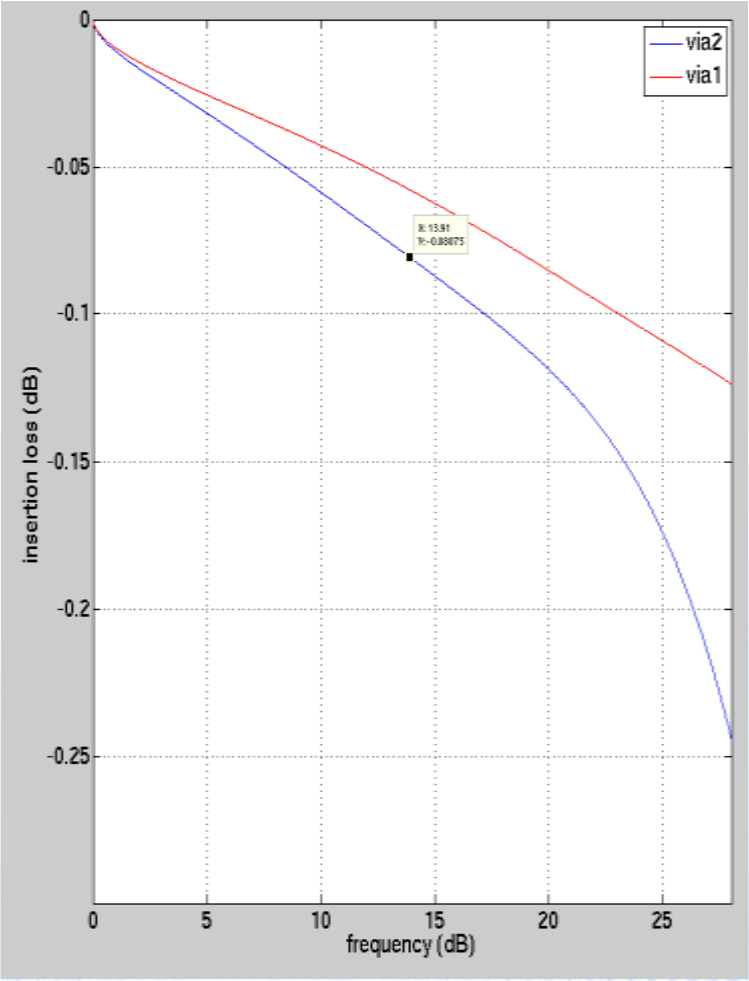
Loss Budget

	FR4-6	N4000-13	Megtron 4	Megtron 6
loss @ 14 GHz/in	2.4	1.5	1.4	0.9
Worst Case Connector loss @ 14 GHz	1.2			
Loss allocation for 2 vias in the channel	0.5			
Max Module PCB loss	1.2			
PCB Trace length Assuming 8 dB loss Budget	2.13	3.40	3.64	5.67
PCB Trace length Assuming 10 dB loss Budget	2.96	4.73	5.07	7.89
PCB Trace length Assuming 12 dB loss Budget	3.79	6.07	6.50	10.11

- With 10dB loss budget even N4000-13 provides more than 4” reach

Via loss

- Two pairs of differential via structures are simulated
  - Via1 (Via length 11 mil)
  - Via2 (Via length 41 mil)
- Common parameters
  - Via stub 10mil
  - Antipad 40mil
  - Each via structure includes short traces at each end
  - Megtron 6 material
- The loss of via2 at 14GHz is 0.08dB



(VSR) Conclusions

- Channel loss should be no more than 10dB to enable use of CTLE and hence provide lowest power
- Provision of 5-10% pre-cursor tap at the transmitter is beneficial
- Tx amplitude should be no less than 600mV ppd

CAUI-4 Conclusions

- The choice of a 10dB channel budget for OIF-28G-VSR was the result of considerable technical diligence by the VSR working group
- Building on OIF-28G-VSR will give CAUI-4 a technical head-start