The case for a 10dB CAUI-4

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Inphi

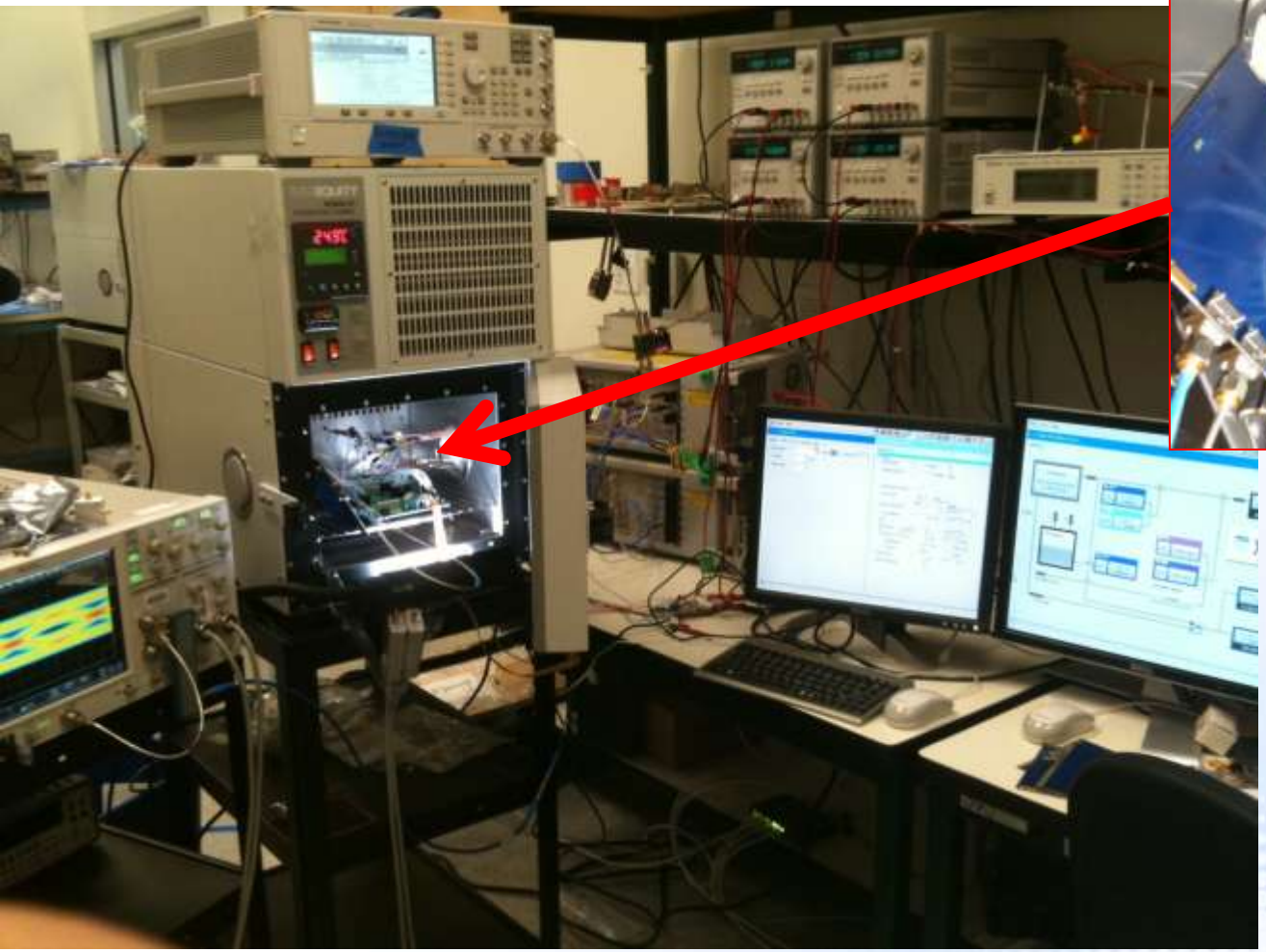
Supporters

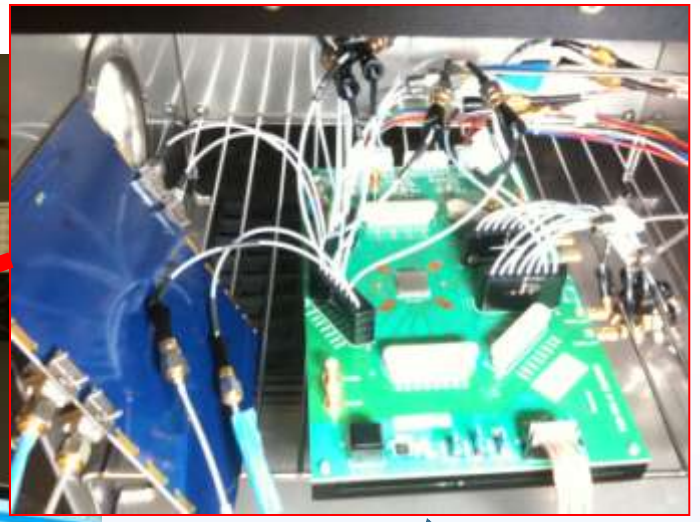
- Jon Anderson, Opnext
- Vipul Bhatt, Lightwire
- Chris Cole, Finisar
- Mike Dudek, Qlogic
- Ali Ghiasi, Broadcom
- Mark Gustlin, Xilinx
- Hiroshi Hamano, Fujitsu Labs. Ltd
- Hideki Isono, Fujitsu Optical Components
- Sanjay Kasturia, PLX/Inphi
- Scott Kipp, Brocade
- David Lewis, JDSU
- Mike Li, Altera
- Jeff Maki, Juniper
- Arthur Marris, Cadence
- Brian Misek, Avago
- Gary Nicholl, Cisco
- Mark Nowell, Cisco
- Tom Palkert, Luxtera
- Iain Robertson, TI
- Nathan Tracy, TE

Overview

- 10dB channel re-timer capabilities
  - Measured results for Inphi's low power 40nm CMOS CDR
- Future trends in re-timers
- The real reach of a 10dB channel budget
- Conclusions

Lab Setup



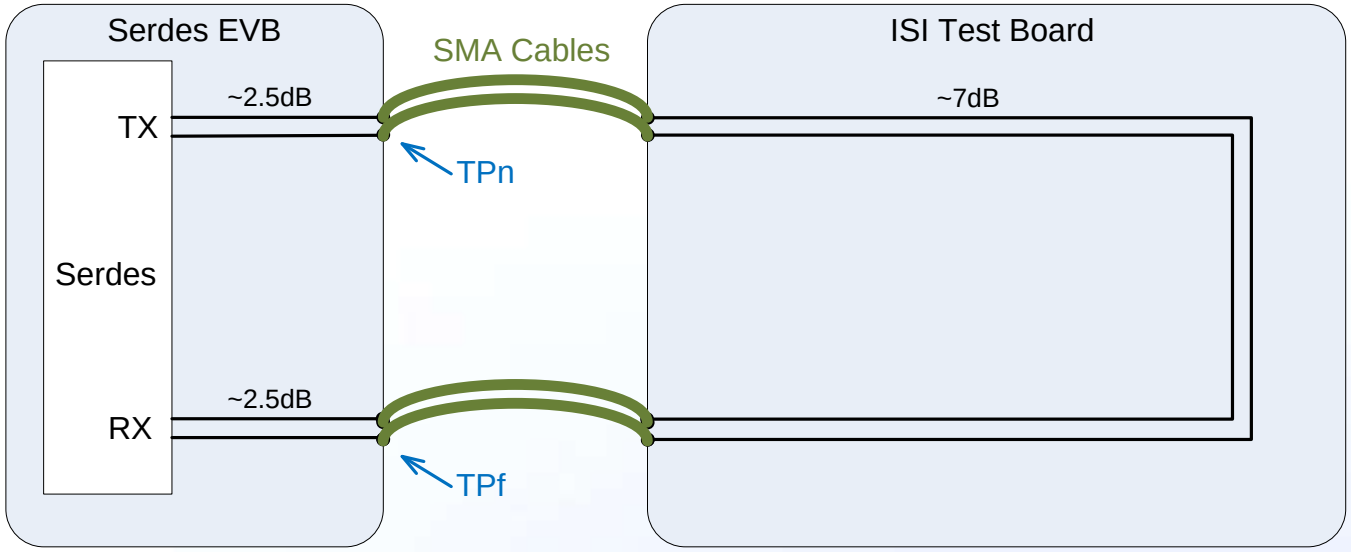


SERDES EVB

ISI stress channel

Thanks to Ishwar Hosagrahar (Inphi) for these Lab Measurements

Test Setup

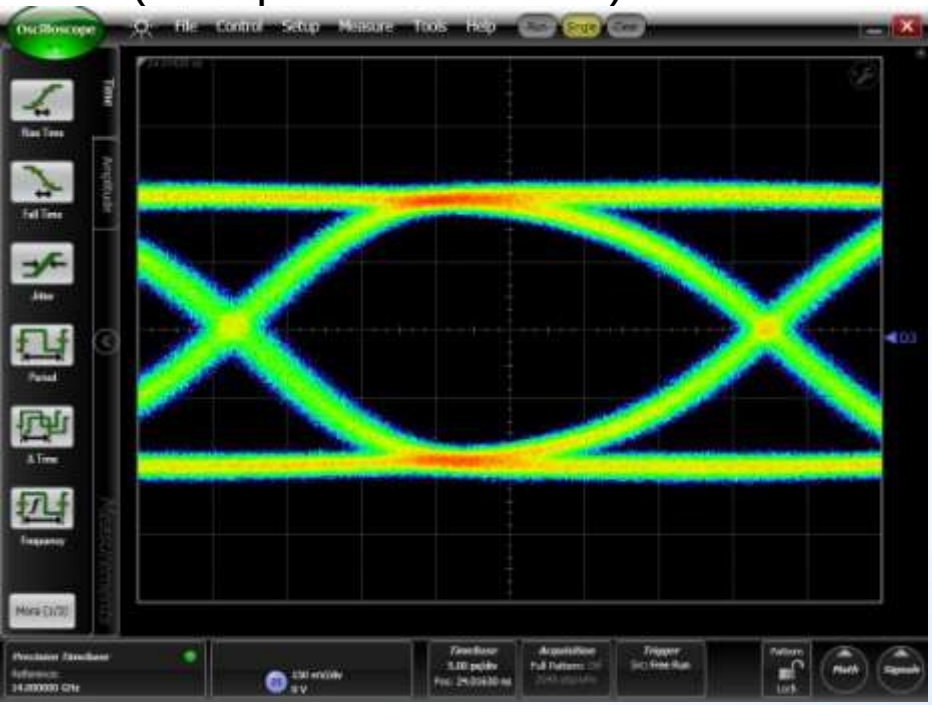


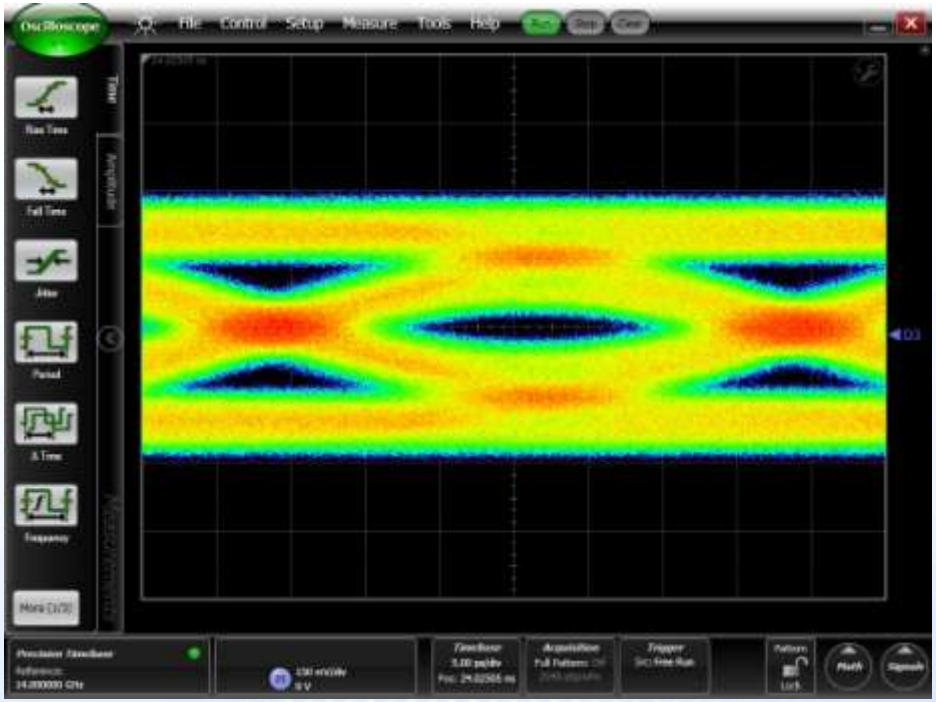
- Total estimated loss ~12dB
  - (ISI board + GB board (TX + RX) = ~7dB + 2x(~2.5dB))

Transmit Near-end Eye @ 28Gbps

Sampling scope measurements
(PRBS31 data pattern)

(10% postCursor used)

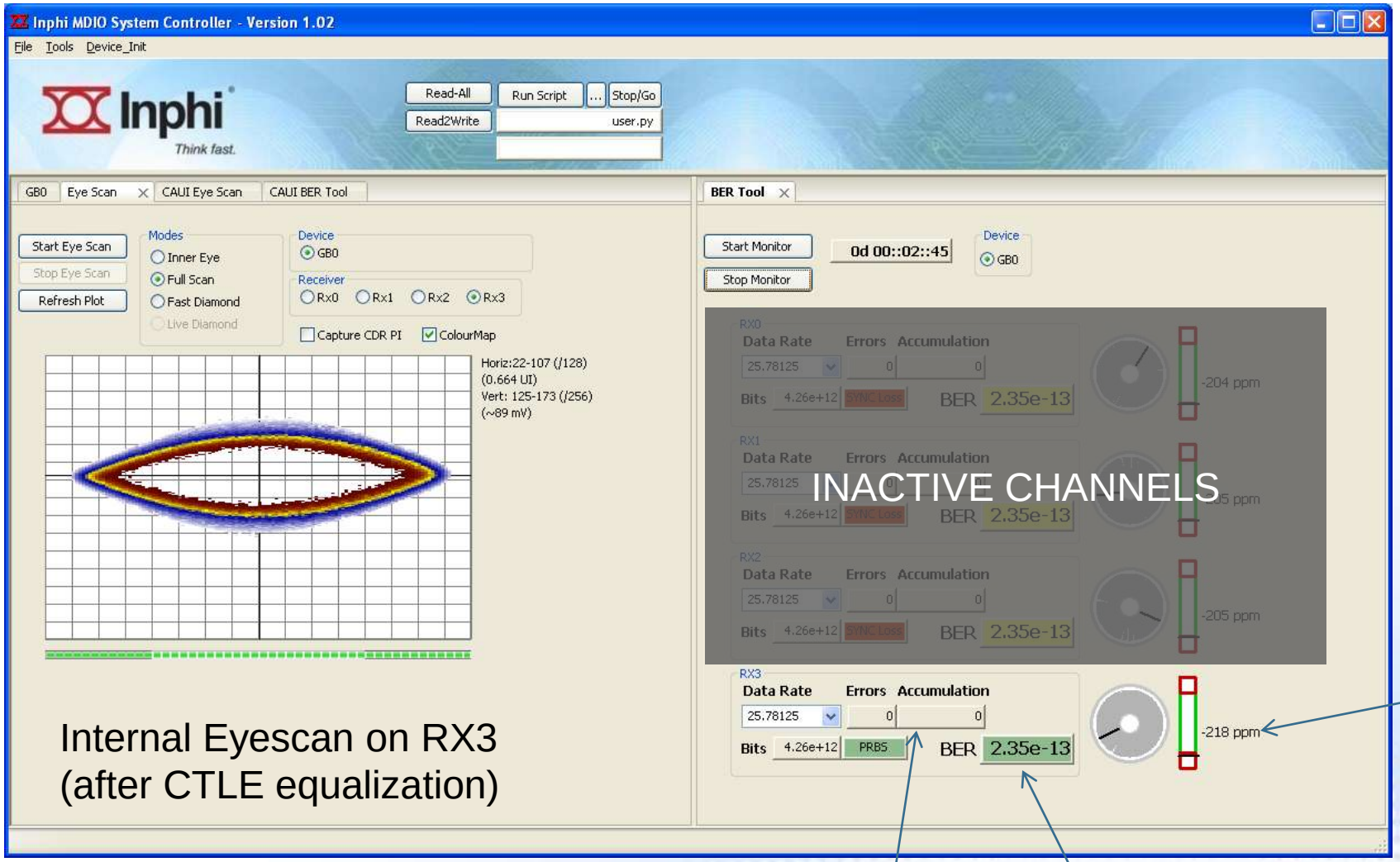




Near-End (TPn)

Far-end (TPf)

RX Internal Eyescan and BER (>2.5 min gate)



>-200ppm offset

0 errors

Better than 1E-12 BER (in this time period)

Re-timer technology for a 10dB channel

- CMOS & SiGe retimers are available for the 10dB VSR channel
  - CTLE only equalization keeps complexity/power down
  - ~2W for a re-timer pair (4 duplex lanes)

- CMOS retimers will leverage process improvements
  - 28nm and beyond
  - Power for a retimer pair (4 duplex lanes) will fall
    - ~20mW/Gbps → ~10mW/Gbps
  - This reduction in device power will allow smaller packaging
    - smaller packages, finer ball pitches

Implications of a 10dB Loss Budget

	Worst Case	N4000-13	N4000-13SI	Megtron 4	Megtron 6
loss @ 14 GHz/in	1.7	1.5	1.2	1.175	0.9
Connector loss @ 14 GHz (note 1)	1.2	1.2	1.2	1.2	1.2
Loss allocation for **2 sets** of vias in the channel **(note 2)**	0.5	0.5	0.5	0.5	0.5
Max Module PCB loss **(note 3)**	1.5	1.5	1.5	1.5	1.5
Host PCB Trace length with 10 dB loss Budget	**4.00**	**4.53**	**5.67**	**5.79**	**7.56**

Note 1: The 1.2dB connector loss budget was based on Quattro 1 connector

Note 2: OIF assumed 0.5dB total via loss (via to layer 9, 10mil stub, 40mil anti-pad, megtron6 has less than 0.08dB loss)

Note 3: The max trace length in a module may be as short as 4mm using Meg6 in the module with 0.5dB loss for cap results in 0.64dB loss in the module

- The VSR 10dB loss budget was agreed to support a **minimum** of 4" host trace
  - Better materials, design practises, and connectors can extend this reach
  - A compliance methodology based on compliance boards facilitates this

Conclusions

- The choice of a 10dB channel budget for OIF-28G-VSR was the result of considerable technical diligence by the VSR working group
  - It allowed the development of low power re-timer chips
- Staying with a 10dB channel will allow development of even lower power & form-factor re-timer chips
  - This is key to "*enabling smaller and lower power 100G optical modules*".
- Technical and economic feasibility of a 10dB CAUI-4 link is self-evident
- Recommend a Next Gen 100GbE Optical SG objective of :

  "Define a retimed 4-lane 100G chip-to-module interface based on OIF-28G-VSR"