WDM PICs for Optical Interfaces

Integrated Photonics for 100G Interfaces

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ONECHIP PHOTONICS

Contributors and Supporters

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Why Integrate?

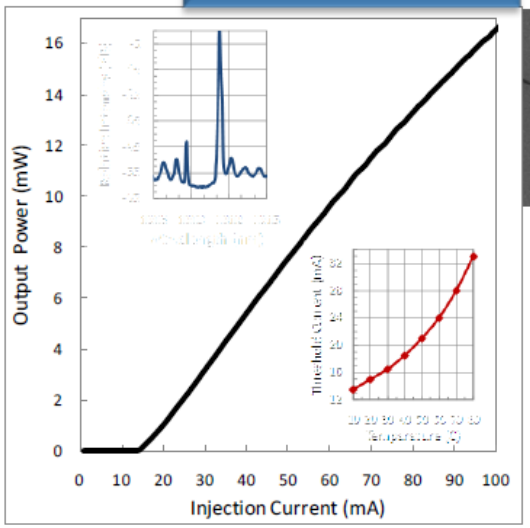
- History of electronics shows that integration reduces cost
  - Reduces manual assembly cost
  - Improves manufacturing yield and uniformity
  - Improves robustness
- Functions that are presently expensive benefit most from future cost reduction through integration
  - Computers were once expensive, are now pervasive and cheap… and even contained in the least expensive PON transceivers
  - The largest future cost reduction due to integration will likely be enjoyed by more feature-rich blocks, e.g. WDM vs. single-λ interface

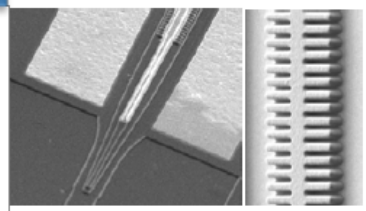
Photonic Integrated Circuits (PICs)

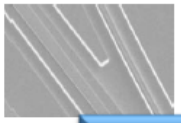
- Much has been presented to the Task Force about using PIC architectures:
  1. Palkert_01_1111
  2. Palkert_01c_0312
  3. Palkert_02b_0312
  4. Palkert_03b_0312
  5. Palkert_01_0512
- To date, the predominant architecture presented has been a parallel fiber architecture utilizing silicon photonics.

PIC structures in InP

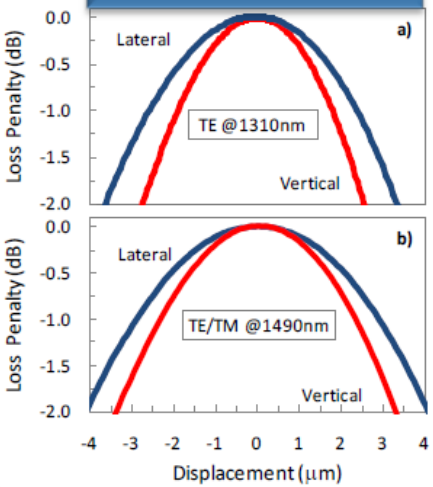
distributed feedback laser

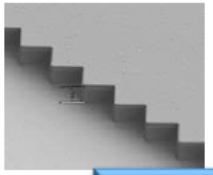




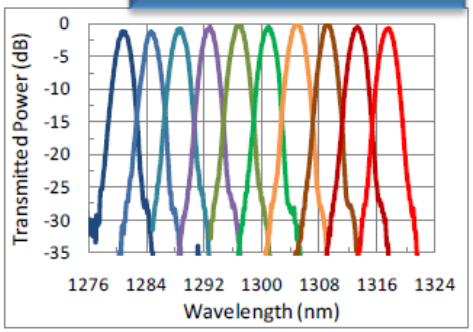


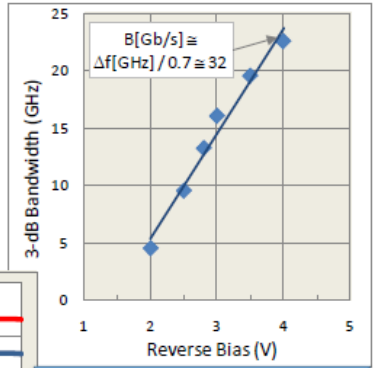
laterally-tapered spot-size converter

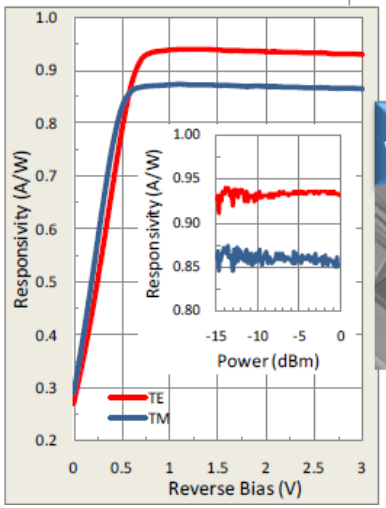




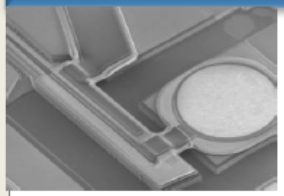
planar wavelength division (de)multiplexer

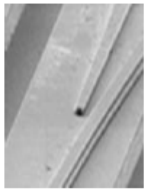


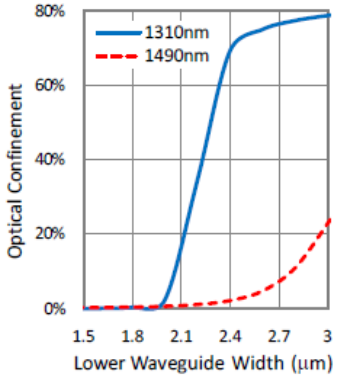




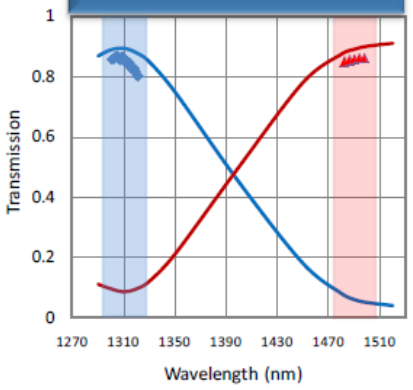
waveguide photodetector







vertical wavelength splitter



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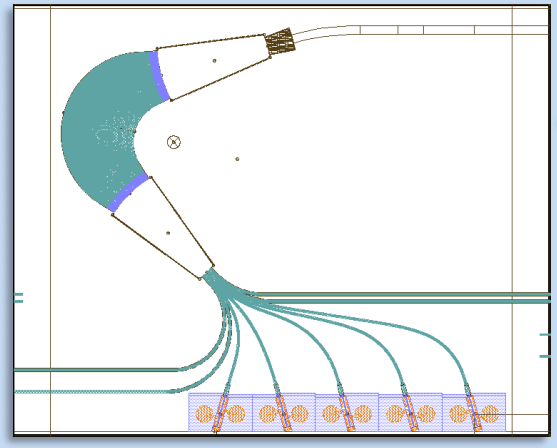
WDM PICs

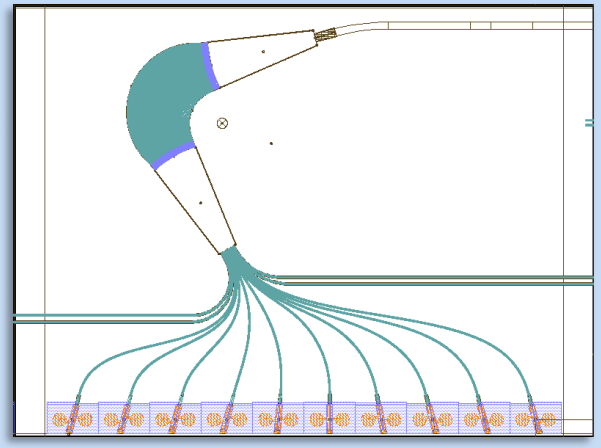
- Providing multi-channel WDM functionality in planar devices has been well-demonstrated in the industry using either Arrayed Waveguide Grating or Echelle Grating structures.

AWG Receiver PICs



4x25 Gb/s

10x10 Gb/s



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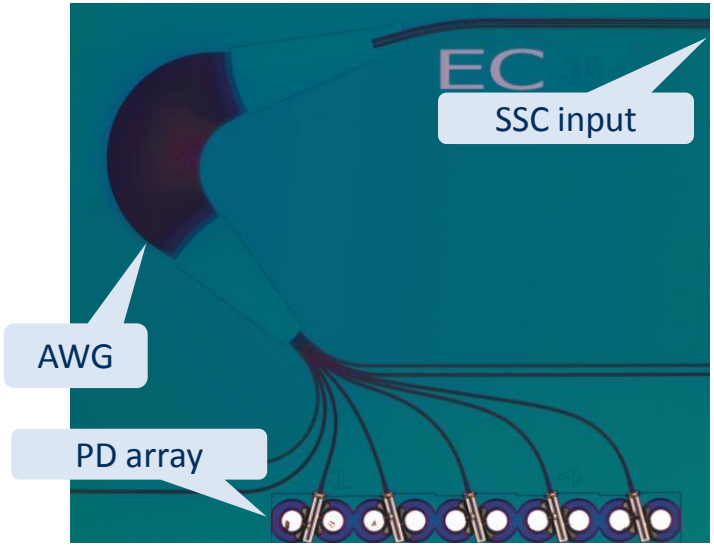
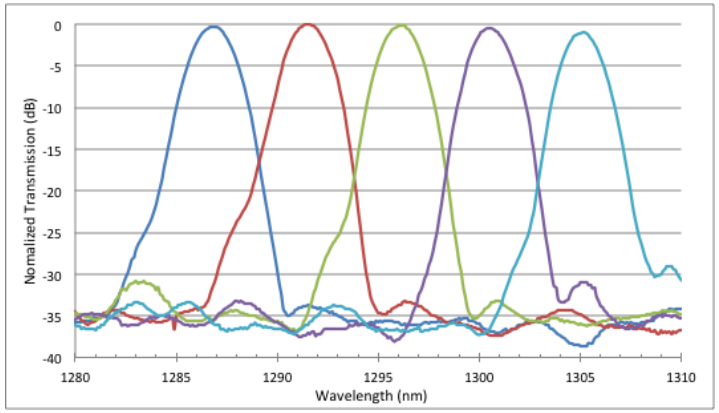
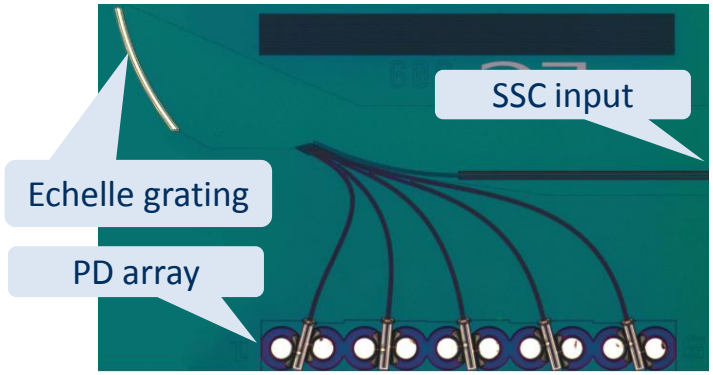
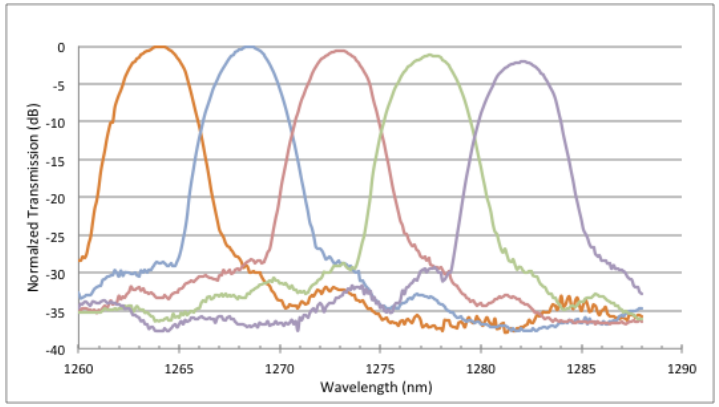
WDM Receiver PICs





- **Key performance features**
  - **FC responsivity**: 0.25 A/W
  - **Adjacent (non-adjacent) xtalk**: -30 dB (-35 dB)
  - **Polarization dependent λ (FC responsivity)**: 0.03 nm (0.3 dB)
  - **3-dB BW**: 21 GHz (>25 GHz in Phase 2)





ONECHIP PHOTONICS

WDM PICs

IC (CMOS)	PIC (MGVI)
Standard material: Si/SiO_2	***Material***: InP and related compound semiconductors on Fe:InP substrate
Standard device design / processing	***Devices***: design / fabrication building blocks
Standard design rules for building the circuit out of individual devices	***Circuits***: functional integration – vertical, parallel integration – at the same vertical level
Standard process flow and wafer fabrication steps	***Fabrication***: generic processes, e.g. dry / wet etch, passivation, planarization, metallization
Standard (s/w) design tools for converting the circuit design into photomasks compatible with standard fabrication process	***Design tools:*** some commercial (e.g. BPM) but mostly in-house, still long way to go towards automated computer-aided design toolset
Standard on-wafer testing techniques and procedures	***Testing:*** once PICs have on-chip active devices, automated wafer probing is a very real option
Standard pin layout and packaging	***Packaging:*** application driven, on a Si bench
Fabless model that enables for ASIC design to be decoupled from the device design at one end and wafer fabrication – at the other	**Fabless model that *potentially* allows for ASPIC design to be decoupled from both the device design and wafer fabrication**

Conclusions

- End user comments(in palkert_02b_0312) that users are looking for the lowest cost connectivity solution:
  - Medium sized data center: I don't like parallel fiber because I have to carry spares in the data center, however, cost is absolutely king and I will deploy the lowest cost technology.
  - Very Large data center: I will deploy the lowest cost solution regardless of the fiber type. If PSM4 is not standardized I encourage the formation of an MSA outside the IEEE.
  - Large MSO: We deploy only SMF in our data centers.

Conclusions

- As noted in Kolesar_01b_0112 8-lane cabling is 4x to 5x more expensive than 2-lane cabling
- As noted in Kipp_01_0112 there is only a 20% cost premium nR4 (with WDM) versus nR4 (without WDM).
- The additional cost of parallel fiber in PSM4 will be greater than a WDM module implemented with PICs.
- A duplex fiber nR4 could be compatible with existing LR4 implementations.