Choosing Host PCB for CR4 Optimally with an Eye Toward Unretimed Interface

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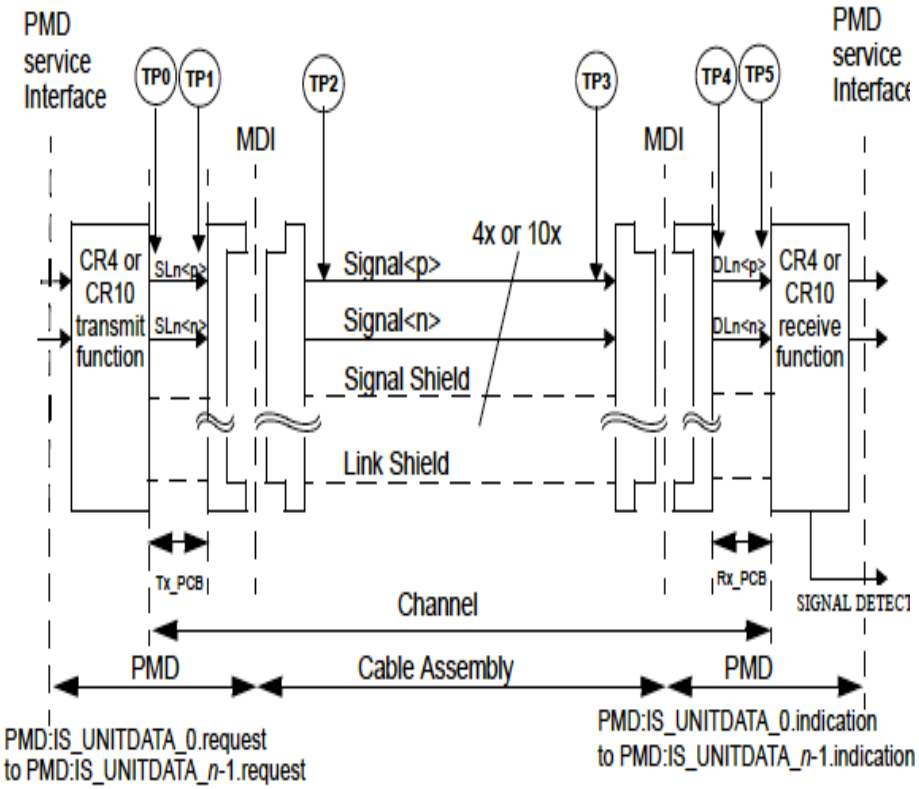
Kona

Overview

- Review of 802.3ba
  - nPPI
  - CAUI
- Application requirements of retime and unretime
- Why sacrificing cable reach for host PCB not worth it
- Why CR4 is a cPPI-4 instantiation

Application Reference Diagrams

- CRx/nPPI vs CAUI



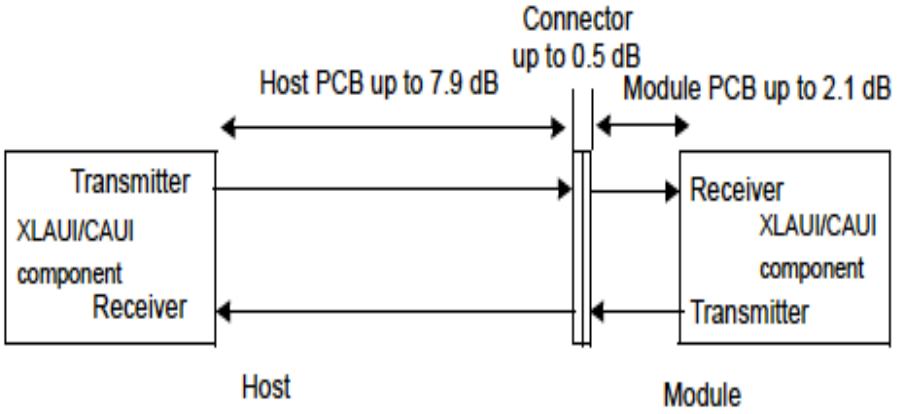


Figure 83B–2—Chip-module loss budget at 5.15625 GHz

Review of 802.3ba Uretimed and Retime

- CL85/86 were unretime with 6.5 dB loss budget
- CL83A/B were retimed with 10.5 dB loss budget

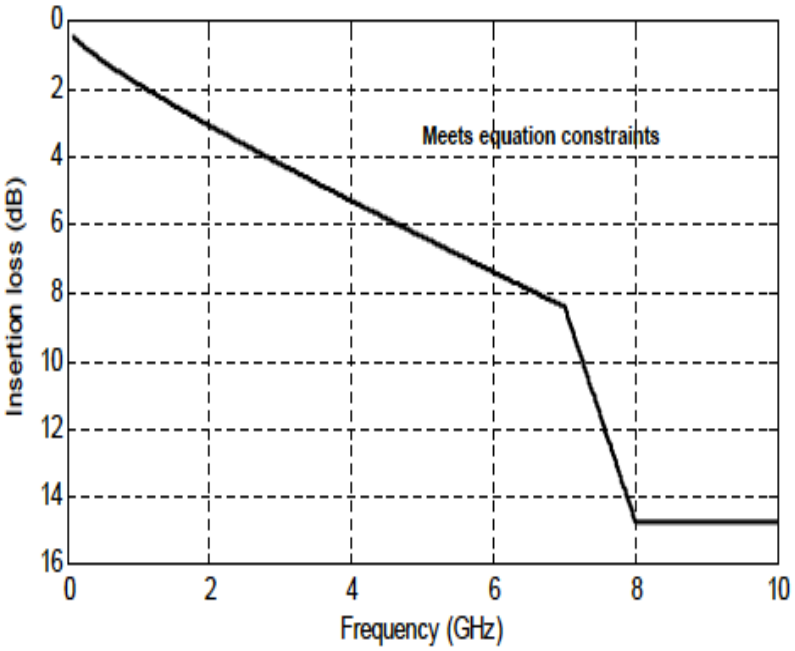


Figure 85–4—Maximum insertion loss TP0 to TP2 or TP3 to TP5

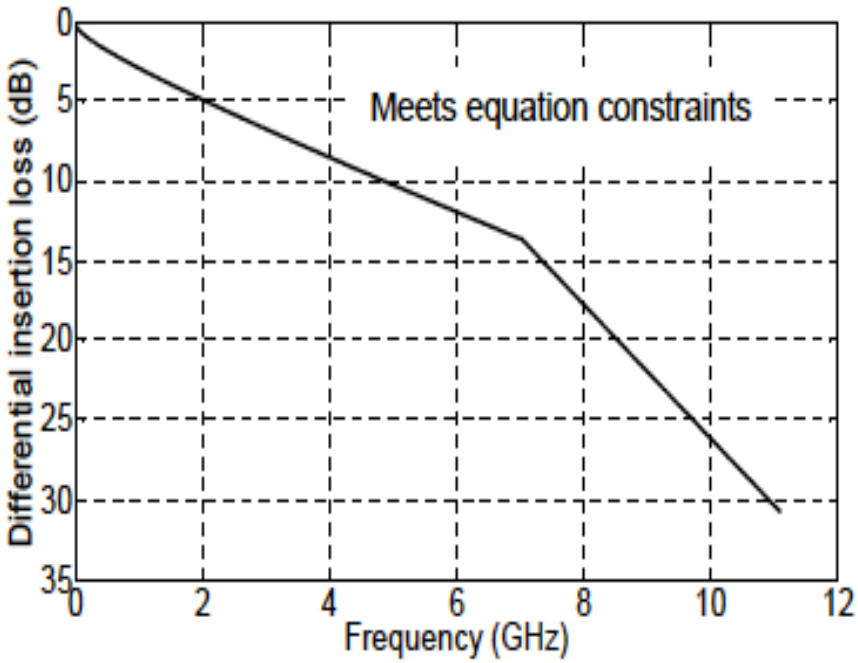


Figure 83A–13—Differential insertion loss

Review of 802.3ba Uretimed and Retime Cont.

- Retime has more relax RL for obvious reasons

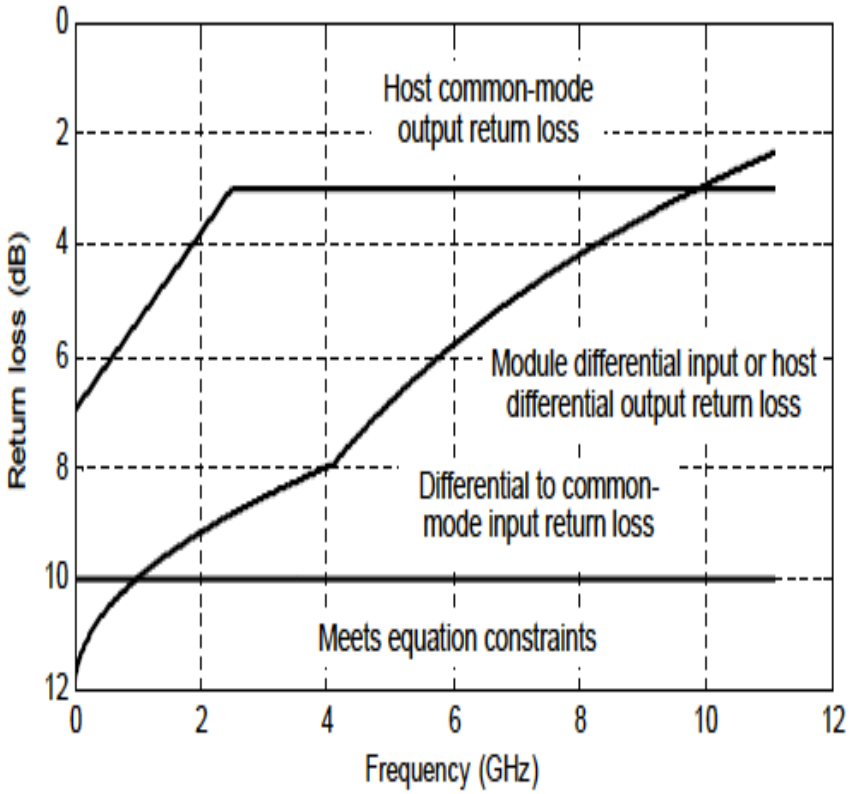


Figure 86A–1—Return loss specifications

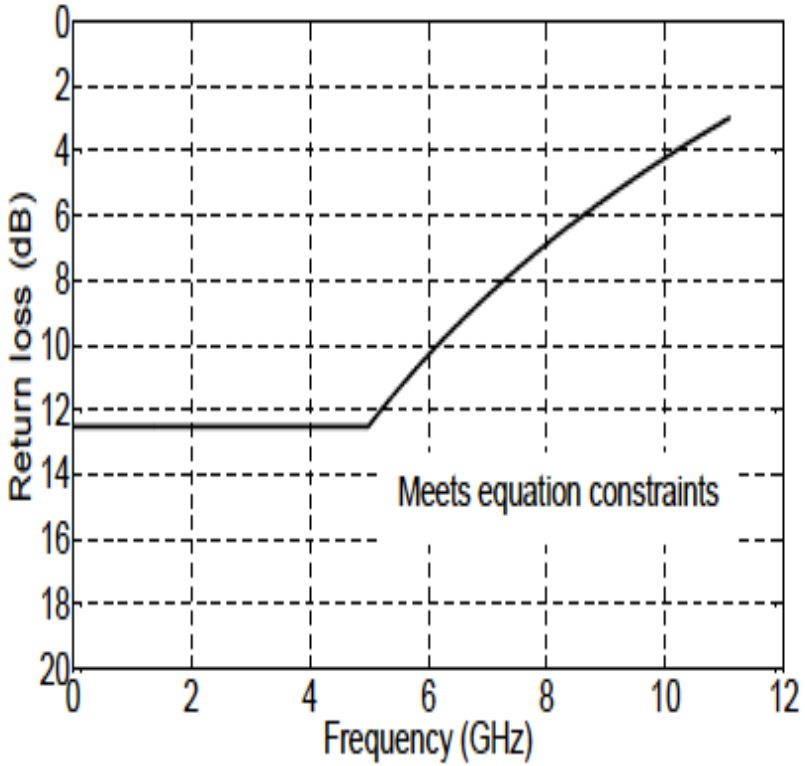
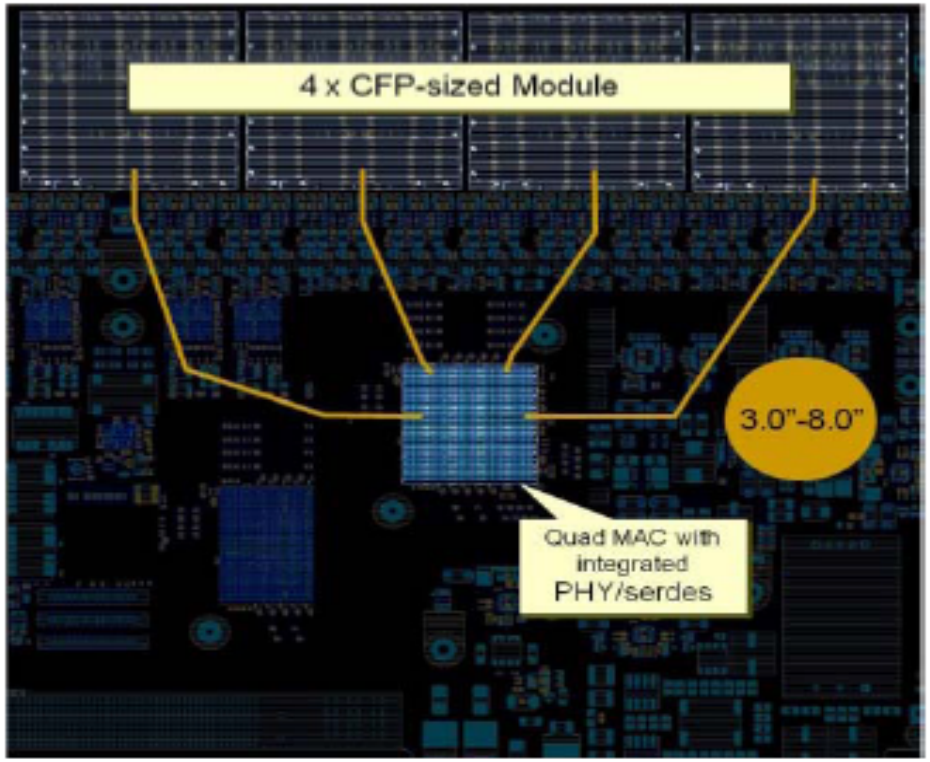


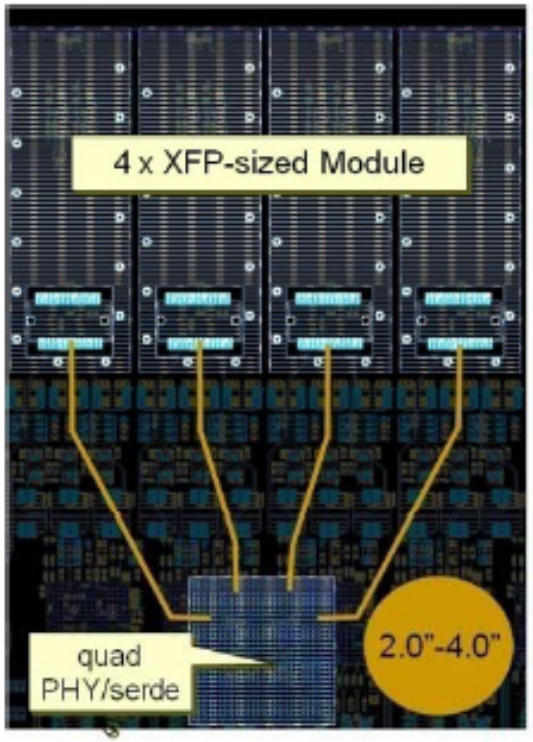
Figure 83A–14—Differential input return loss

Applications Requirements

- Per nicholl_01_1111 “Host PCB should be long enough to support 4 modules”
  - QSFP28/CFP4 sizes are comparable to XFP and 2-4” is sufficient



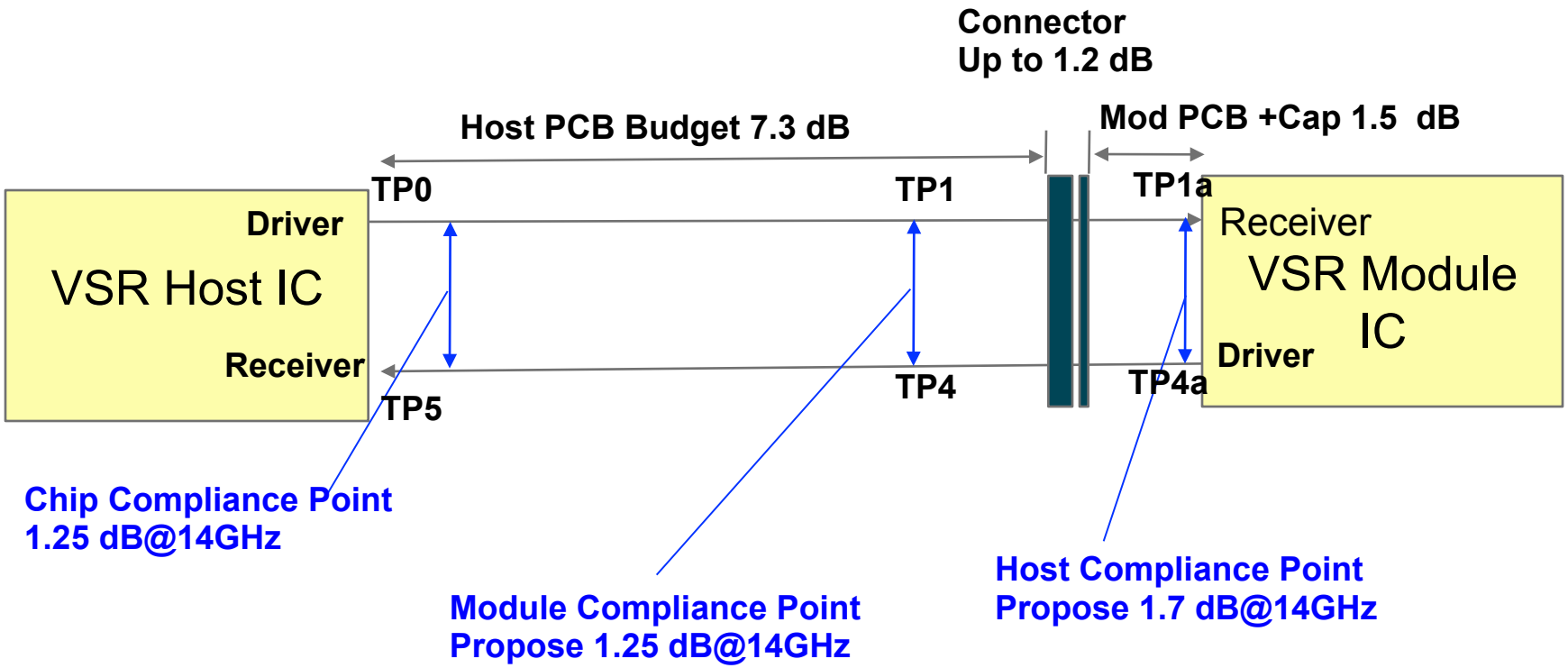
4 port CFP



4 port ‘XFP’

OIF 28G-VSR Architecture and Reference Points

- Follows 802.3 CL83B (CAUI)



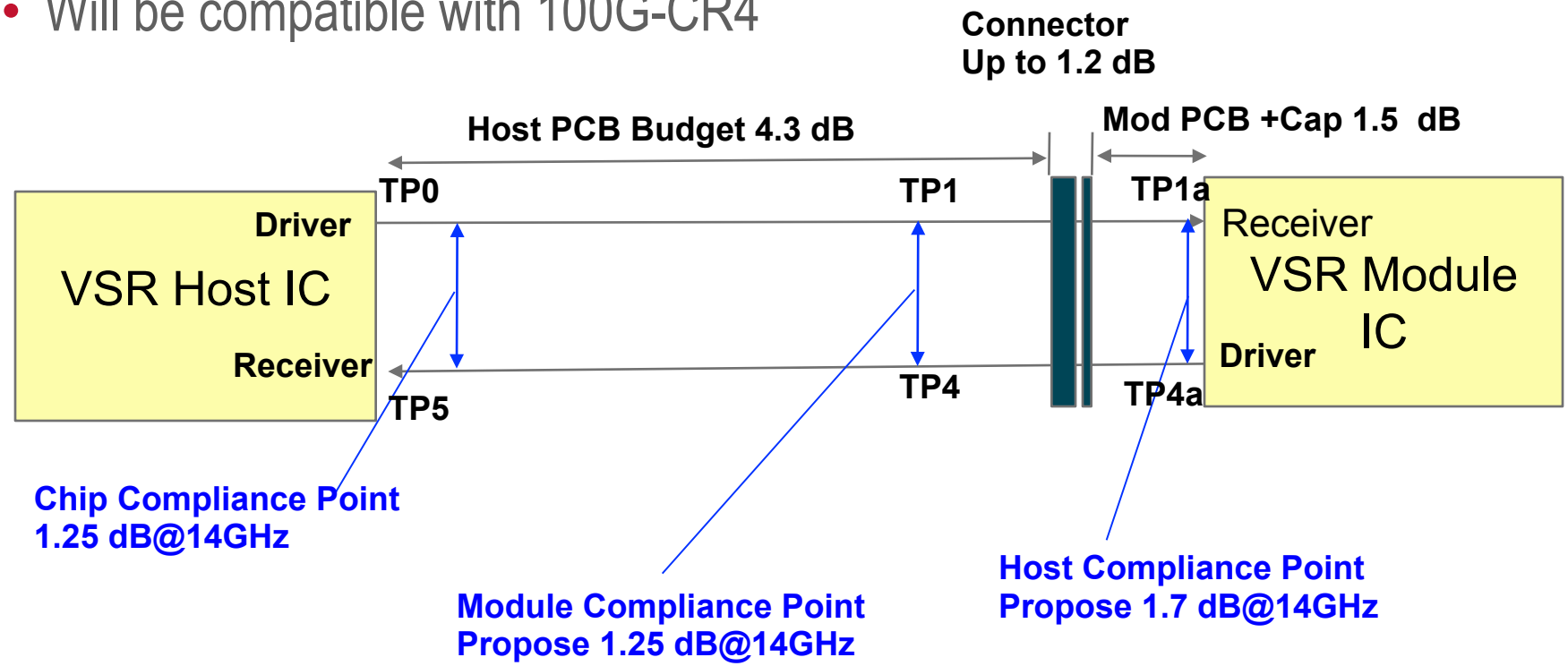
VSR Channel Loss Budget Table

- Assumes 10 dB loss from host IC balls to module IC ball
  - Not enough to support switch to module applications without external retimer

Traces	FR4-6	N4000-13	N4000-13SI	Megtron 6
Loss at 14 GHz /in	2.0	1.5	1.2	0.9
Worst Case Connector loss at 14 GHz	1.2			
Loss allocation for 2 Vias in the channel	0.5			
Max Module PCB Loss	1.5			
Host PCB Trace Length Assuming 10 dB Loss Budget	3.4000	4.5333	5.6667	7.5556

cPPI-4 Architecture and Reference Points

- Follows 802.3 CL86(nPPI) and CL85
- Will be compatible with 100G-CR4



cPPI-4 Proposed Channel Loss Budget

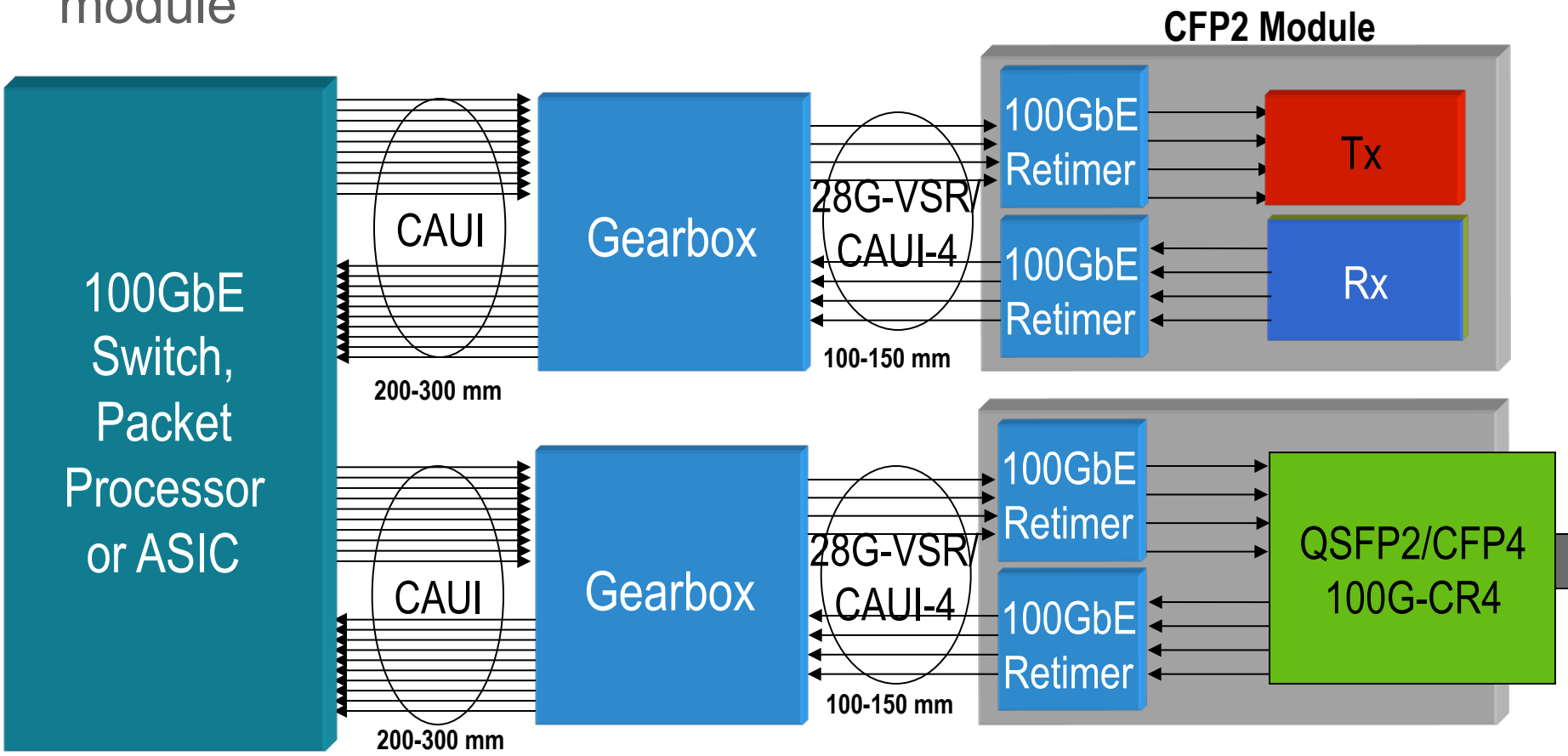
- Attach cPPI-4 with 7 dB loss budget can support unretimed optical PMDs as well as100GCU copper cables

Traces	FR4-6	N4000-13	N4000-13SI	Megtron 6
Nominal Loss at 14 GHz /in	2	1.5	1.2	0.9
Connector loss at 14 GHz*	1.2			
Loss allocation for 2 Vias in the channel	0.5			
Max Module PCB Loss/DC Blocks at 14GHz*	1.5			
PCB Trace Length Assuming 7 dB Loss Budget	1.9000	2.5333	3.1667	4.2222

* For 100 GbE operation since the HCB and connector are specified for operation up to 28GBd there will be 0.2-0.3 dB unallocated margin.

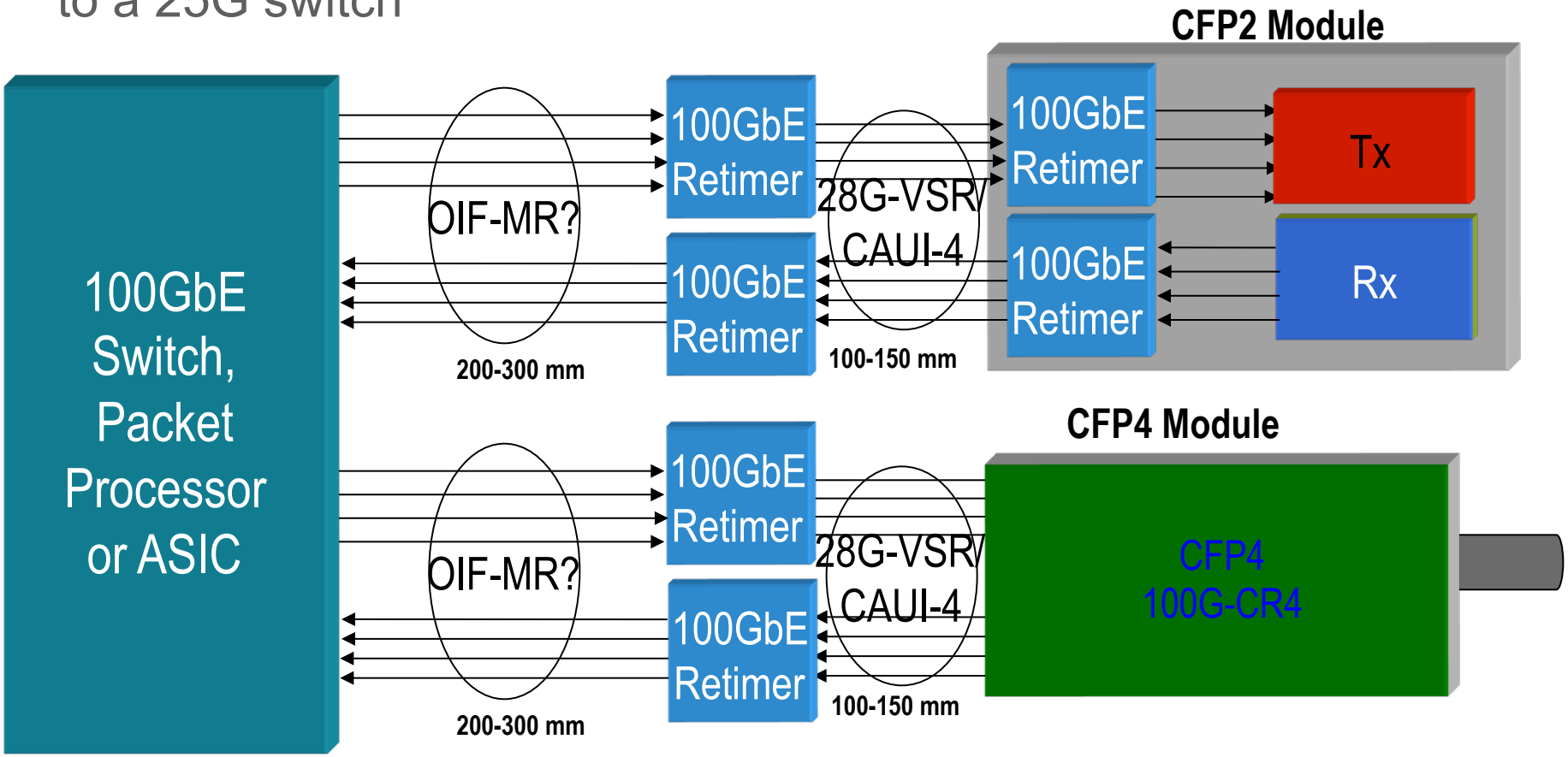
Current Retimed Applications with "CFP2"

- CFP2 is retimed interfaced works nicely with current silicon generation where Gearbox is placed 4-6" away from module



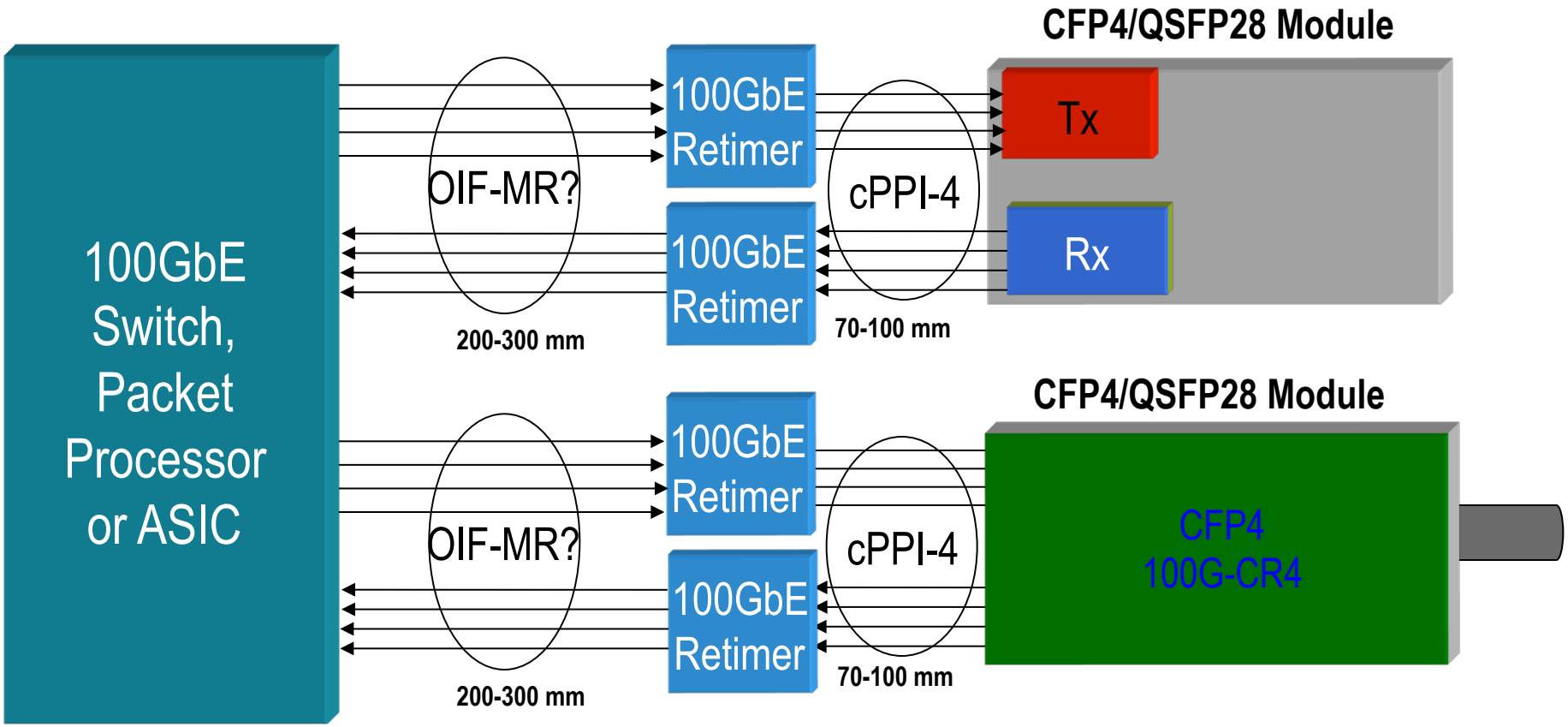
Next Generation Retimed Applications with "CFP2/CFP4"

- Require doubling up on the retimers and Cu reach gets sacrificed for no good reason
- In most application VSR loss budget is not sufficient to connect to a 25G switch



cPPI-4 Applications Diagram with CFP4/QSFP28

- Follows the SFP+/QSFP+ model
  - Allow smaller lower power module implementations
  - Adding 8 retiemrs to the module doubles VCSEL based PMD PD at 25G!



Summary

- CR4 fits unretime application
- In CR4 instantiation such as QSFP28/CFP4 up to 4 module can be supported with proposed cPPI-4 loss budget
- VSR/CAUI loss budget of 10 dB allow building simple CTLE based CDR to keep the module low but when ASIC/Switches go to 25G I/O it will require doubling up on retimers
  - Defining retime interface with 15-20 dB loss can significantly increase the CDR PD which is a dilemma!
- cPPI-4 can allow full 5 m CR4 reach without FEC and 7 m with FEC
  - Instead of about 3 m without FEC and 5 m with FEC
- If CR4 loss is higher when we define the cPPI-4 to support optical module we could end up having wasted the CR4 budget as the host would have lower loss.