Low Latency NRZ and PAM4 FEC Architecture

IEEE P802.3bj

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Stephen Bates – PMC-Sierra, Matt Brown – APM, Sudeep Bhoja- Broadcom,
Roy Cideciyan – IBM, Mark Gustlin – Xilinx, Adam Healey - LSI,
Martin Langhammer - Altera, Jeff Slavick – Avago,
Zhongfeng Wang – Broadcom

Introduction

- Over the past few meeting cycles many different FEC options have been presented, for both NRZ and PAM4 PHY options, this paper discusses the currently proposed candidate FEC codes for the possible NRZ and PAM4 PHYs

- Considerations are:
  - Effective gain required for the application (includes raw FEC coding gain and burst error behavior)
  - Logic complexity and power
  - Achievable latency
  - Over-clocking requirements

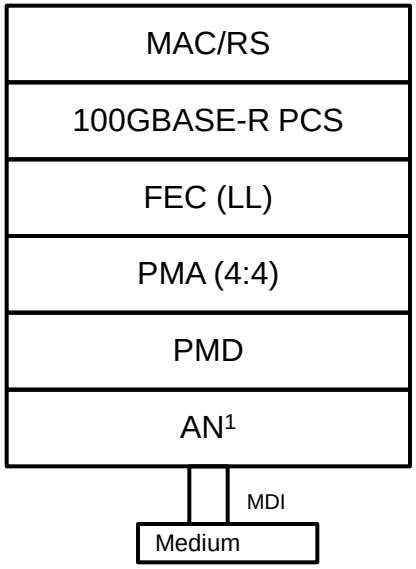
- The FEC architecture is shown along with an update to the FEC processing for each proposal

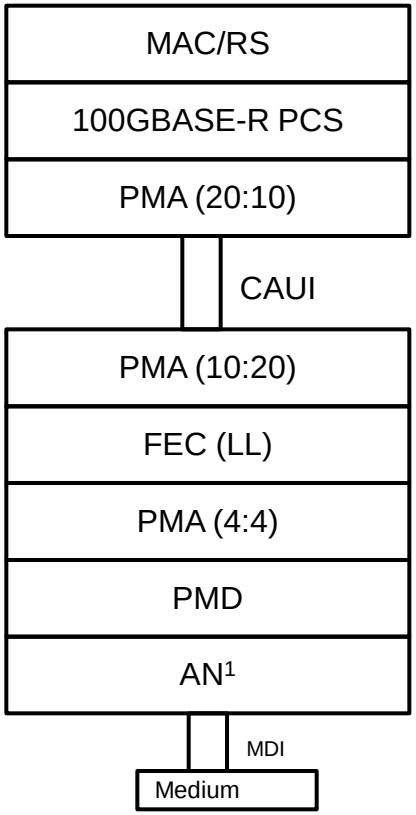
- A proposal is shown for an NRZ backplane FEC

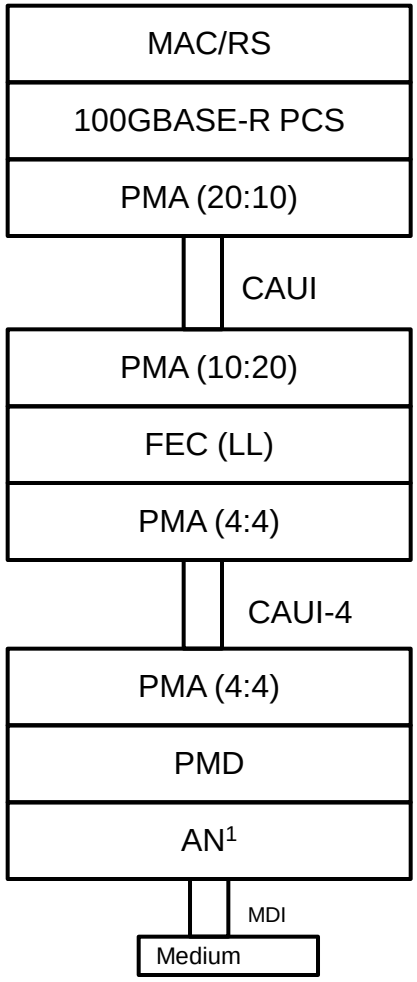
- A proposal is shown for a PAM4 backplane FEC

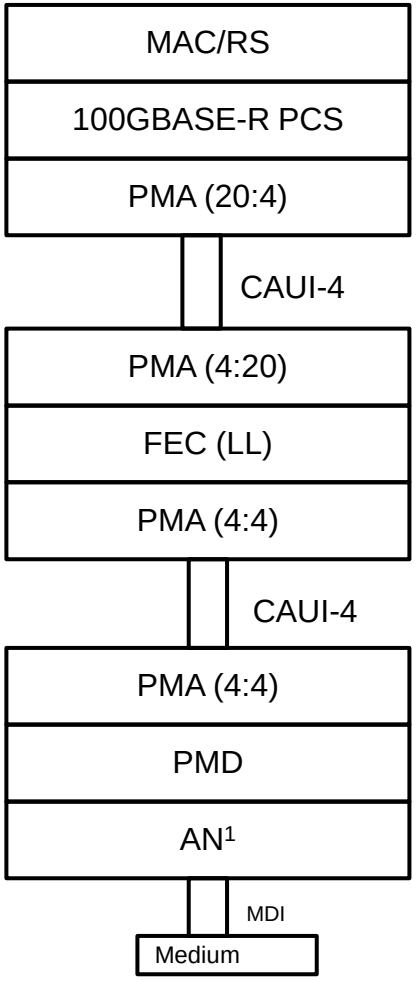
Low Latency FEC Architecture

- The figures below show possible striped (and therefore low latency) FEC architectures









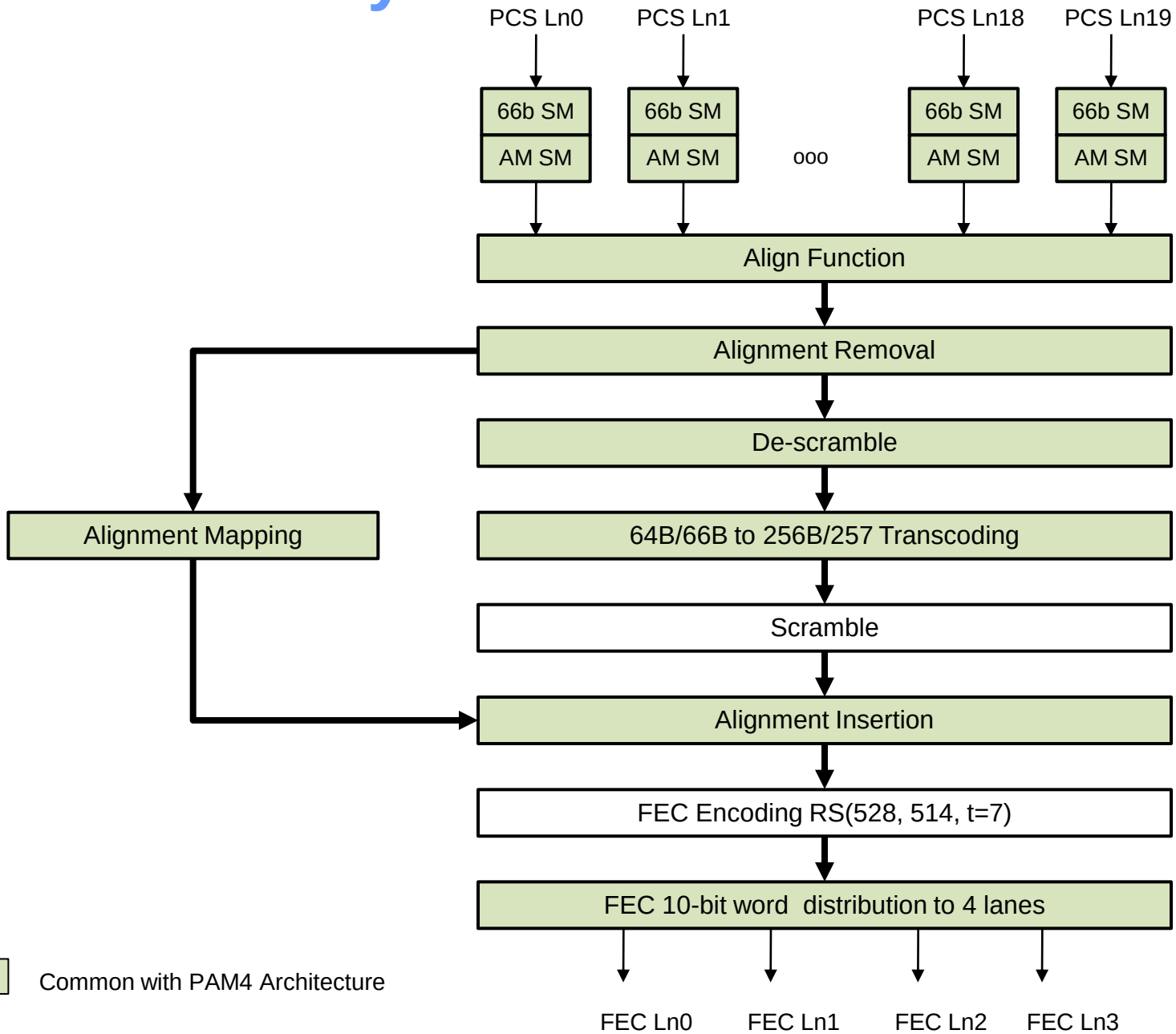
Note 1: Conditional on PMD type and solution chosen

Note: LL = Low Latency CAUI-4 – assumed new 25G+ interface

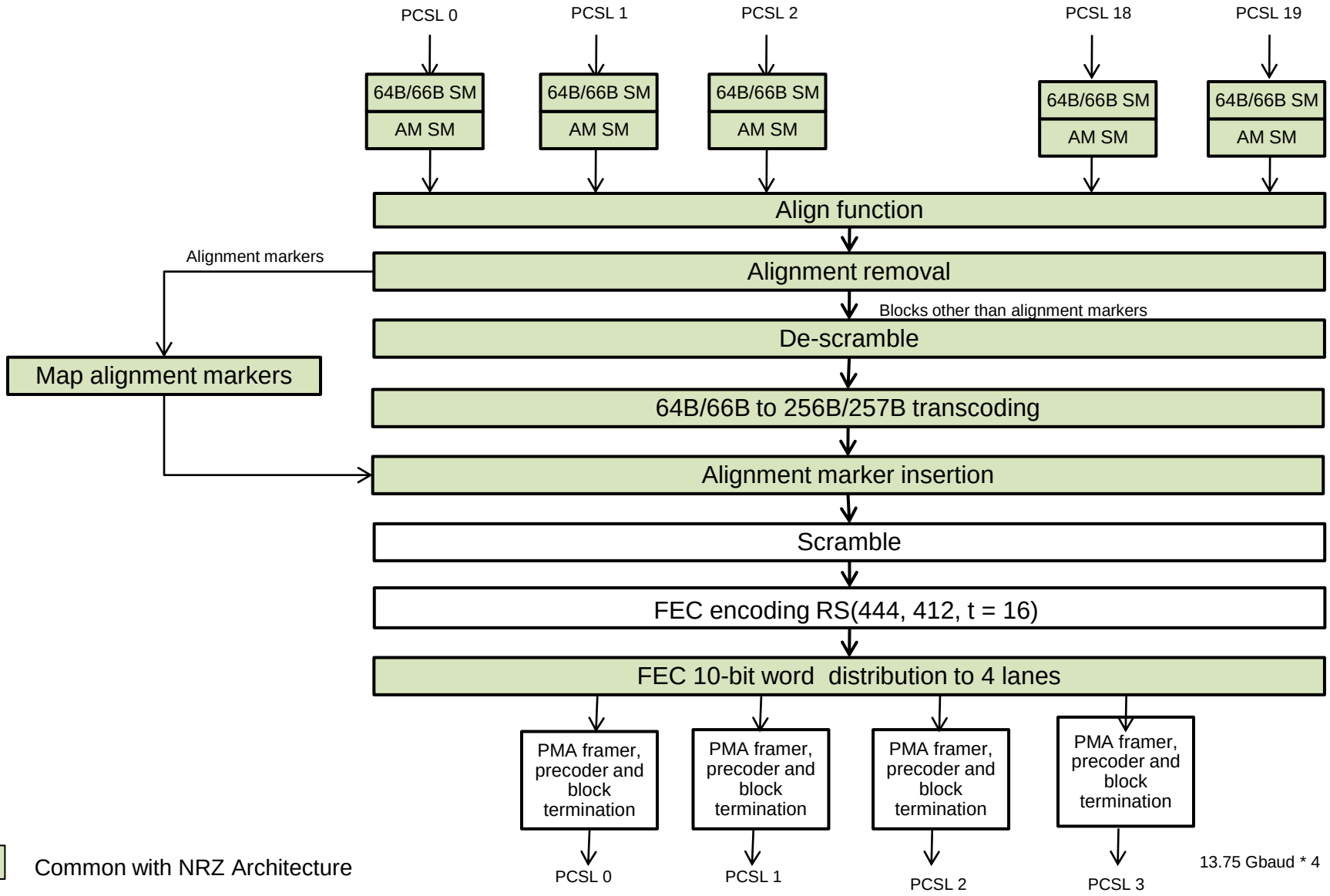
Proposed FEC Operation

- Backplane NRZ:
  - Covered in detail in gustlin_01_0312
  - Same lane rate (25.78G) with or without FEC
  - FEC is optional (to implement and to use) for a channel loss of 30dB or less, and FEC is required for a channel > 30dB up to 35dB
  - Without FEC enabled there is no transcoding (64b/66b encoding)
  - With FEC enabled we use 256B/257B transcoding
  - FEC use is auto-negotiated
  - Proposed FEC code is RS(528, 514, 7, 10) (~4.9dB of gain at 1e-15)
- Backplane PAM4:
  - Covered in detail in brown_01_0312
  - FEC is required and operates at 13.75G
  - FEC uses 256B/257B transcoding
  - Proposed FEC code is RS(444,412,T=16,M=10) (~5.3dB of gain, includes pre-coding)
- Copper cable:
  - At this meeting it is being proposed to use FEC to achieve 5m cable length
    - Use same FEC as NRZ backplane, need to decide how to enable

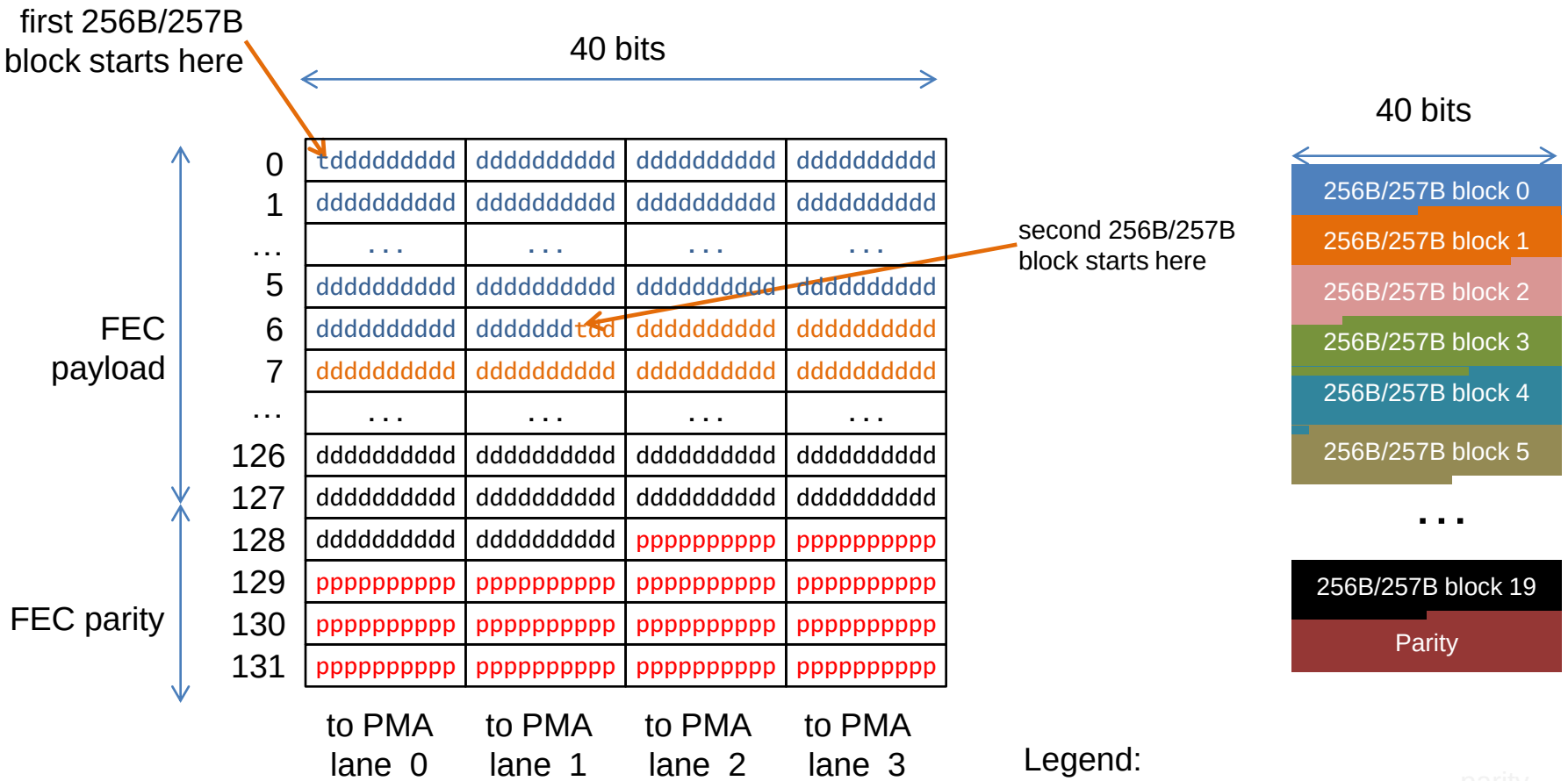
Low Latency NRZ TX FEC Architecture



Low Latency PAM4 TX FEC Architecture

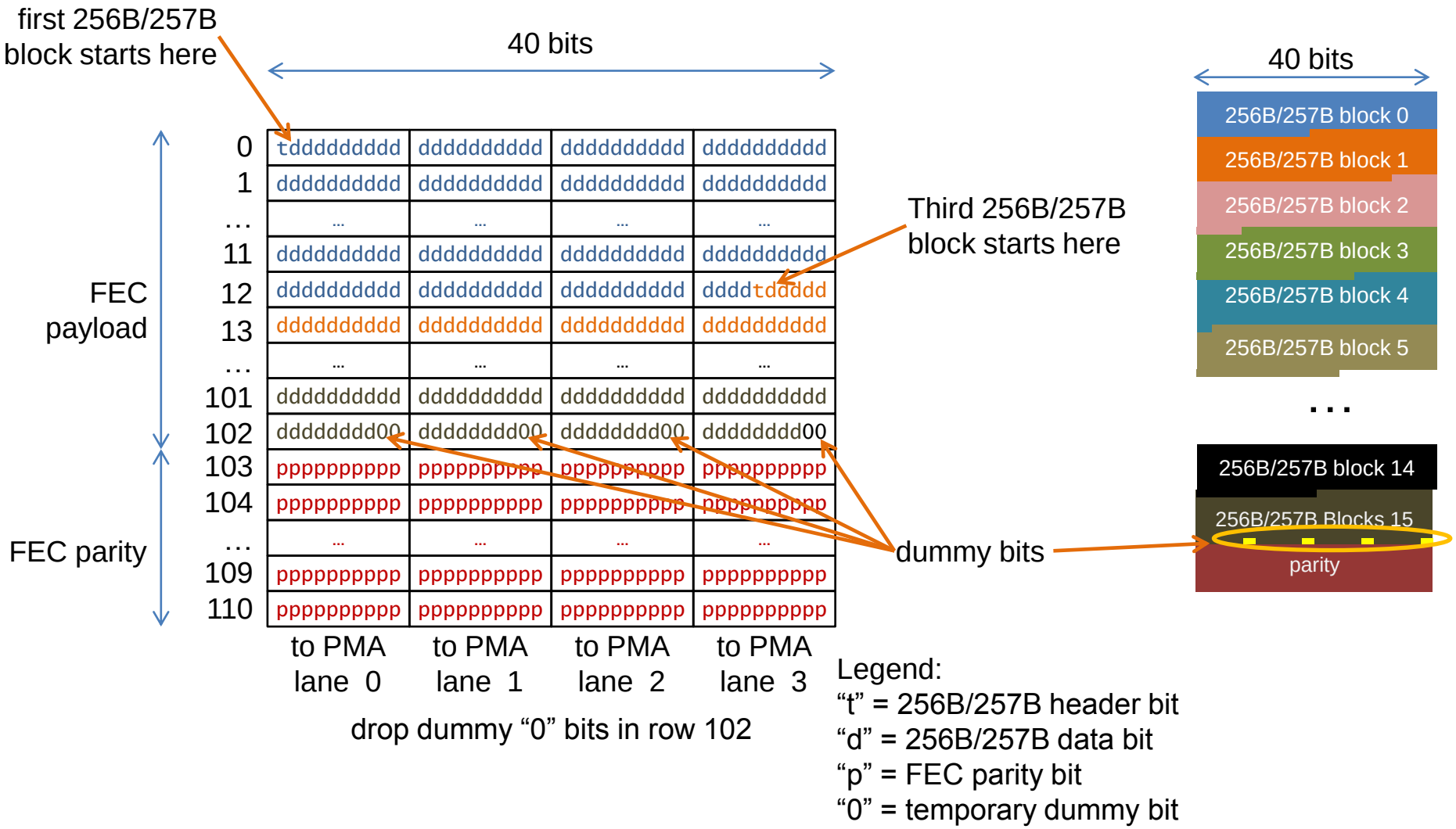


NRZ FEC frame structure



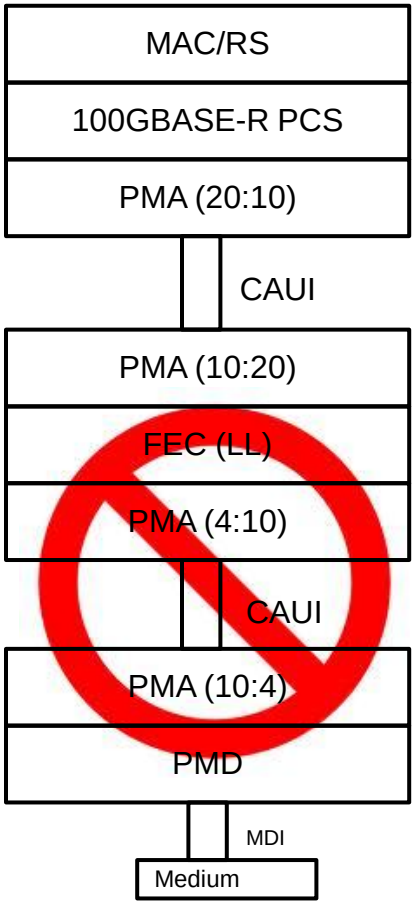
Legend:
“t” = 256B/257B header bit
“d” = 256B/257B data bit
“p” = FEC parity bit

PAM4 FEC frame structure



Low Latency FEC Architecture

- The figure below shows an incorrect architecture, once the Low Latency FEC is inserted, the number of lanes cannot change!
  - At least not with the standard 802.3ba PMAs
  - Architectural restrictions being evaluated, exploring the possibility of supporting 4, 2 and 1 lane options. But we need to look at burst error behavior.



Summary

- The Low Latency FEC codes that have been discussed so far within 802.3bj can fit cleanly into the 802.3 architecture, for both a NRZ and a PAM4 PHY
- However, the LL FEC codes are point to point codes across 4 lanes, and after the FEC code is inserted, normal 802.3ba bit manipulation cannot take place
- There is much in common for the proposed NRZ and PAM4 FEC processing flows that can be re-used if the task force chooses to adopt two PHYs, except for the specific FEC code, though they do share a common symbol size (10bits) which can lead to leverage
- If we do adopt one of the proposed FEC codes for optics or copper cable PMDs, we will need to decide how to handle turning it on for those PHYs or cables that require it

Thanks!