CMOS Photonics 101

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What is CMOS Photonics?

CMOS IC Platform

Electronic IC
manipulates electrons
using transistors

DC Electron
Supply

Electrical I/O

CMOS Photonics IC Platform

Opto-Electronic IC
manipulates both photons
and electrons using
transistors

DC Electron
Supply

Optical I/O

DC Photon
Supply

Electrical I/O

CMOS Photonics IC Platform leverages existing multi-billion dollars of investment, Infrastructure and discipline of the CMOS IC industry to manipulate both Electrons & Photons to achieve desired Opto-Electronics functions using External DC Sources.
By controlling the voltages on terminals, MOS Transistor controls the flow of electrons from source to drain. Today, 100s of millions can be placed on a single electronics chip.

By controlling the voltages of the two arms of the modulator, one controls the flow of photons from source to drain with one major difference – Photons cannot be stopped and hence the unwanted will go to Drain. A large numbers of these can be integrated on a single chip.

Just like the transistor is the basic building block for all ICs, Broadband Modulator is the basic building block for all high speed optical interconnects.
Optical Components and Libraries in CMOS

**Silicon waveguides:**
- SOI and etched trenches for respectively vertical and horizontal light confinement
- Small mode size $\rightarrow$ small bending radii $\rightarrow$ compact photonic ICs
- Demonstrated losses < 0.1 dB/cm

**Library of passive waveguide structures**
- Termination
- Splitters
- Directional couplers

**Library of fiber-to-the-chip couplers**
- Single and polarization splitting grating couplers
- Low loss-coupling waveguide to single mode fiber
- Enable wafer scale optical testability

**Library of waveguide photo-detectors**
- Selective epitaxy of germanium on silicon
- Enable low cost, high-sensitivity integrated receivers

**Library of phase modulators**
- Building block for intensity modulators (MZI, ring,...)
- Very high modulation bandwidth: $\sim$ 160 GHz
• Basic set of optical design rules
  − Process checks
  − Device checks
  − Interaction of optics and electronics
  − Run separately from electrical DRC

• LVS
  − Additional optical LVS for optical connectivity
  − Additional OE LVS for devices connecting to electrical circuits

• Simulation
  − OE simulation of complete subsystems
  − Using electrical models to represent subset of optical devices
Photonic/Electronic LVS, DRC and Simulation

LVS verifies that the layout (devices and connectivity) matches exactly the schematic, at all levels of hierarchy.

All optical design rules are documented in a design manual with tables and diagrams, and implemented for automated checking in an Assura rule deck. Assura is the Cadence physical verification tool.
Single Chip 4x28Gbps Optical Transceiver

- Die size (5 mm x 6 mm)
- Die size is driven by laser and fiber attachment
- White space available for additional logic

RXs

TXs

Digital core
8 Fiber array I/Os
4 for transmit and 4 for receive

Receiver / Photo-Detector

Transmitter / Modulator

LAMP Packaged Light Source

Single CW Laser
Split 4 ways
Waveguides & Refractive Index in CMOS

- Optically smooth surfaces are now possible in mature CMOS processes
- CMOS photonics uses standard CMOS equipment and processes
- Silicon is transparent at $\lambda > 1.1$ um
- High index contrast waveguide enables micron size devices

Starting Wafer Material
SOI (Silicon on Insulator)

Thin Silicon Layer
Glass Insulator (BOX)

Bulk Silicon

Used in many CMOS foundries
Si refractive index $\sim 3.45$
Glass index $\sim 1.46$

Etched waveguides

Glass Insulator

Bulk Silicon

Deposited Glass

Glass Insulator

Bulk Silicon

Glass Insulator

Bulk Silicon

Optical Intensity

$n_1 \ n_2 \ n_1$

$n_2 > n_1$

Losses are 0.0043 dB per 10 um turn

Vlasov, et al, IBM
Mach Zehnder Interferometer (MZI)

Modulator overview

- When $Q_R - Q_L = 0$ Optical ‘1’
- When $Q_R - Q_L = \Pi$ Optical ‘0’
- Applying a + / - voltage on $V_{right}$ decreases / increases $Q_R$ respectively.
- Applying a + / - voltage on $V_{left}$ decreases / increases $Q_L$ respectively.
- For silicon modulators, the applied + / - voltage injects / removes electrons and holes in the optical path which changes the optical index $\Rightarrow$ Free Carrier Plasma Dispersion Effect

MZI deployed in optical systems for over 20 years
Tx Optical Eyes at 28Gbps – Simulation and Measurement:

Cadence MZI Simulation Model

- 28G optical eye
- PRBS-31
- ER = 9.3 dB
- Trise/Tfall ~ 12ps (20%-80%)

Excellent correlation between simulation and measurement
Demonstrated 25G Performance

25G Modulator Demonstrated in Silicon

25G Photodetector Demonstrated in Silicon
CMOS Photonics enables several ways to increase channel capacity beyond raw data rate:

- **Wavelength diversity (WDM):** Enabled by on-chip MUX/DEMUX.
- **Multi-level signaling (i.e. PAM-4):** Simplified by external laser modulation

- Channel spacing = 1.6 nm = 200 GHz
- Typical optical insertion loss < 2.5 dB
- Thermal phase tuners are used to shift the spectral response providing:
  - Temperature compensation
  - Process compensation
  - Agile wavelength plan
CMOS Photonics Integration - Advantages

• Low power
  – 780mw for 4x10G QSFP today (20mW/Gbit)
• Enables high density solutions
  – CMOS Photonics Physical Density > 130 Gbps/mm²
  – CMOS Photonics I/O Density > 400 Tbps/mm²
  – Show CFP going to SFP
CMOS Photonics
Summary of Capabilities

- **Performance**
  - Reliable (1M ports shipped to date)
  - Extremely small devices due to high contrast index waveguides
  - Multitude of optical building blocks – modulators, detectors, muxes, switches, etc
  - High Speed Modulation at extremely low power
  - CW laser source => low cost

- **CMOS Compatibility**
  - CMOS fabrication process => low cost
  - CMOS IC Simulation tools
  - CMOS IC layout tools
  - Monolithic integration of multiple opto-electronic building blocks in simulation tools => Large scale integration

CMOS Photonics enables a new class of low power, low cost, high density solutions