Performance Studies of 100 Gigabit Ethernet Enabled by Advanced Modulation Formats

Jinlong Wei, Jonathan D. Ingham, Richard V. Penty and Ian H. White

E-mails: {jw748, jdi21, rvp11, ihw3}@cam.ac.uk

Thank you to David Cunningham for useful discussions and advice

Outline

- ❑ Background
- ❑ Part I: Simulation Evaluation
  - ❑ System Descriptions and Parameters
  - ❑ Link Power Budgets
  - ❑ Power Dissipation
- ❑ Part II: Experimental Demonstration

Next Gen 100 Gigabit Ethernet with a Single Channel

- IEEE 802.3 NG 100 Gigabit Ethernet PMD study group proposed PAM
  - Single-laser 100 Gigabit Ethernet
  - FEC is incorporated
  - Use of MZ modulator is considered

- We have developed a full simulation tool to evaluate various 100 Gb/s systems
  - In addition to PAM, we have investigated performance for NRZ, CAP and optical OFDM
  - In addition to MZ modulators, directly-modulated lasers (DMLs) are also considered
  - FEC is included

- We have experimentally demonstrated CAP
  - CAP is implemented without using DAC/ADC, providing high power-efficiency

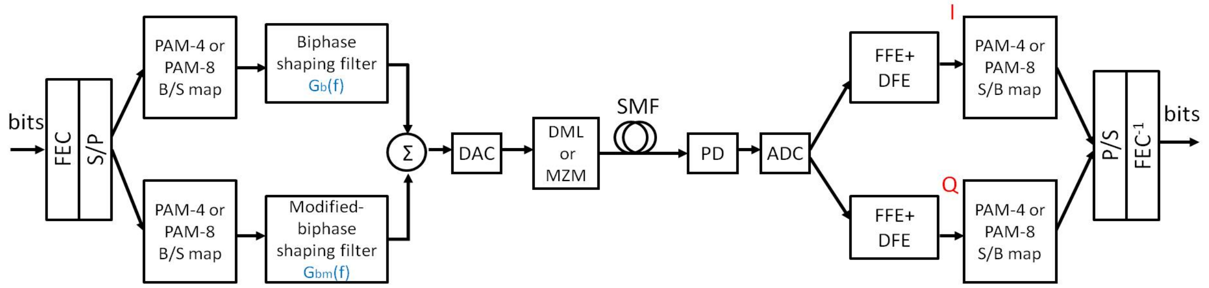
- Work reported in this presentation
  - Theoretical evaluation and comparison of link power budgets of NRZ, PAM, CAP and OOFDM
  - Power dissipation evaluation and comparisons between NRZ, CAP and OOFDM to demonstrate the potential of high power-efficiency for CAP
  - Experimental demonstration of CAP

Reference 28 Gb/s NRZ System Parameters

Component	Parameter	Value
Laser	Type	Gaussian response or rate equations
	Wavelength	1300 nm
	Rise time	12 ps (20% to 80%), i.e., 18.6 GHz 3-dB BW
SMF	Minimum dispersion λ	1324 nm
	Laser centre wavelength	1295 nm
	Dispersion slope	0.093 ps/km/nm^2
	Length	500 m to 2 km
Receiver	Filter type	4th-order Bessel-Thomson
	Cut-off frequency	21.038 GHz
	Responsivity	0.9 A/W
	Sensitivity	-10 dBm (@ BER = 10^{-12})

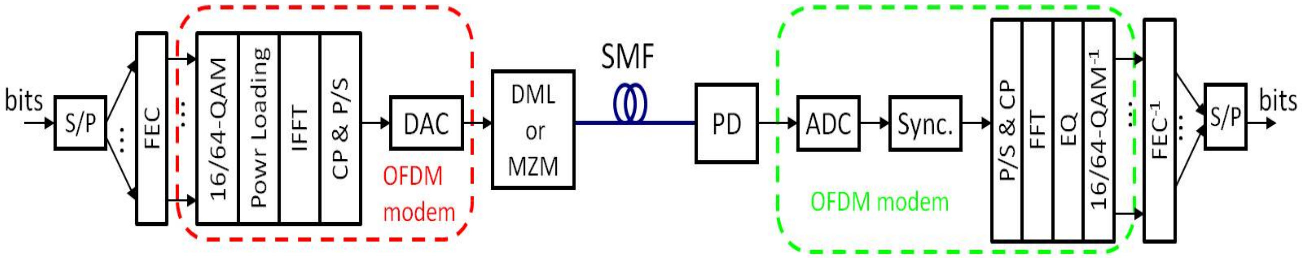
- ❑ The parameters are based on what might be needed for a SMF 32GFC proposal
- ❑ PMD and DGD are ignored for 500 m to 2 km SMF links
- ❑ The above components and corresponding parameters are used for various 100 Gb/s multilevel systems for comparisons

100 Gb/s System Architecture with a Single Channel



P/S: parallel to serial conversion **B/S**: bit to symbol mapping **DAC:** digital to analog convertor
DML: Directly modulated laser **MZM:** Mach-Zehnder modulator **PD**: photo-detector
FFE: feedforward equalizer **DFE:** decision feedback equalizer

CAP-16 or CAP-64



FEC: forward error correction **P/S**: parallel to serial conversion **CP:** cyclic prefix **Sync.:** Synchronization **PD**: photo-detector
(I)FFT: (inverse) fast Fourier transform **DAC/ADC:** digital to analog/analog to digital conversion

QAM-16-OFDM or QAM-64-OFDM

- Digital implementation is considered using DAC/ADC for all systems
- The CAP shaping filters are based on square-root raised-cosine (RRC) pulse shaping
- FEC and equalisation are necessary for the 100 Gb/s single-channel systems
- PAM systems can be obtained by simplifying the CAP system shown
  - Only In-phase component included
  - RRC shaping filters are replaced with rectangular shaping filters
  - NRZ is equivalent to PAM-2

100 Gb/s System Parameters

	NRZ	PAM-4	PAM-8	CAP-16	CAP-64	QAM-16-OFDM	QAM-64-OFDM
Bit rate (Gb/s)	100	100	100	100	100	100.3	100.3
Symbol rate (Gbaud)	100	50	33.3	25	16.7		
SE (b/s/Hz)	1	2	3	4	6	3.65	5.47
DML model type*	1	1	1	2	2	2	2

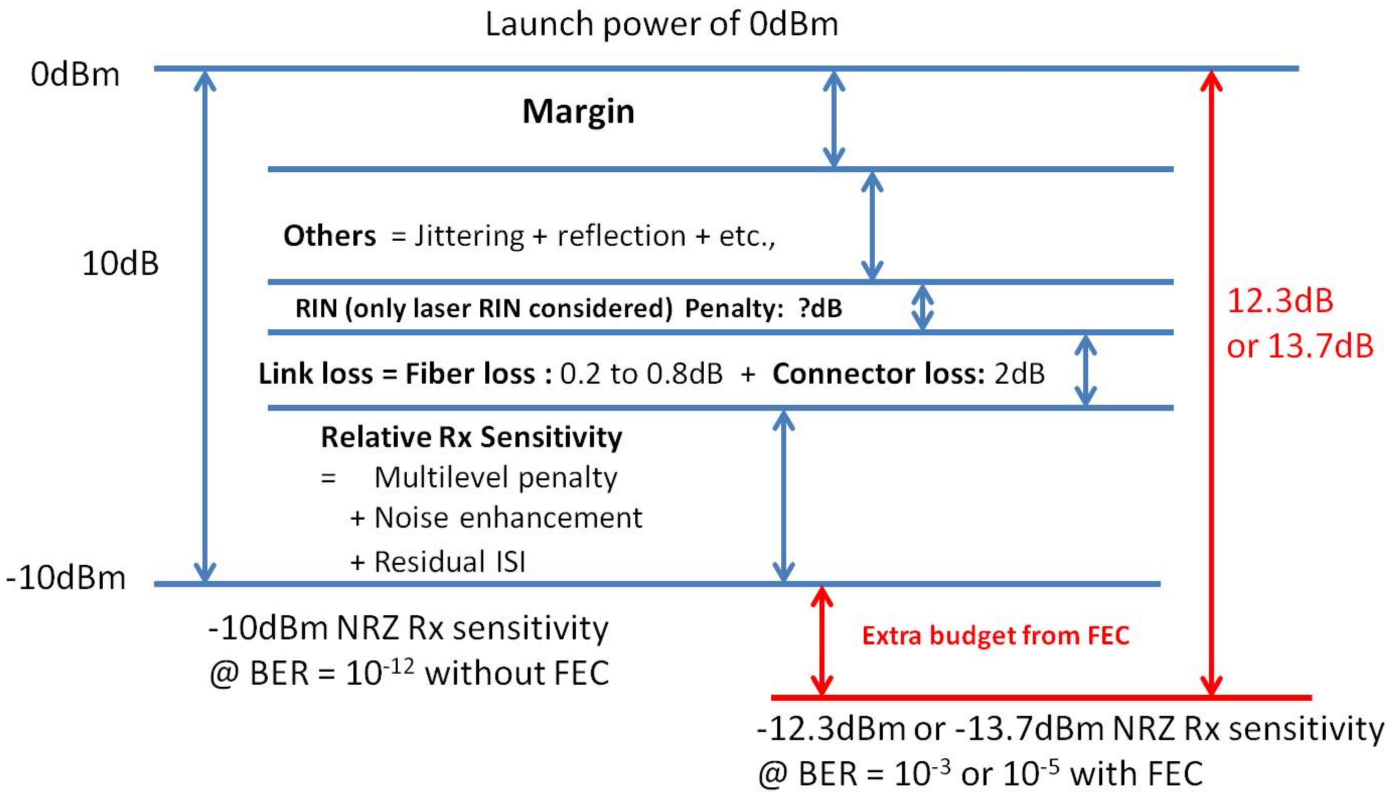
*Type 1 refers to a rate equation model and Type 2 refers to a Gaussian model

- **Rule of Thumb: When the bandwidth of the DML transmitter (~18.6 GHz) is less than about 0.5 of the baud rate, DML nonlinearity has to be considered by using rate equations (Type 1); otherwise a simple Gaussian model (Type 2) can be used**

- **Note that laser nonlinearity can be ignored for all of the coding schemes when MZ modulators are used**

- **Trade-offs between DAC/ADC sampling rate and link power budget determine the choice of the order of multilevel modulation schemes**
  - ✓ Higher DAC/ADC sampling rate allows lower-order multilevel modulation, giving rise to lower multilevel penalties
  - ✓ On the other hand, higher signal bandwidth means stronger ISI due to limited system bandwidth

Power Budget Constituents for Various 100 Gb/s Systems

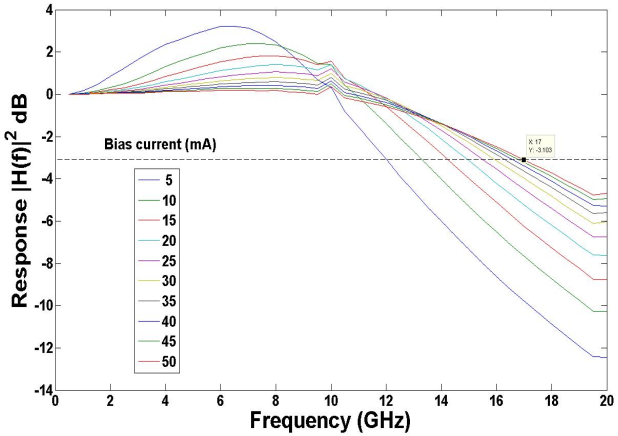


- The power penalty due to reflection, jitter etc. can be obtained from a presentation to the IEEE 802.3 NG 100 Gigabit Ethernet study group[1]

[1] S. Bhoja, "Study of PAM modulation for 100GE over a single laser," Jan 23-27, 2012.

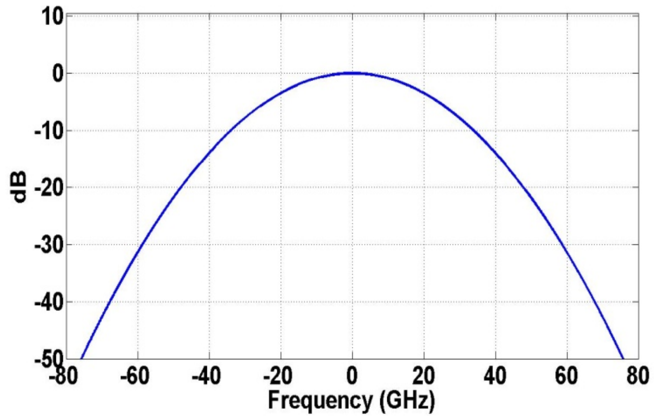
Laser Models

Laser Model 1: Rate equations[1]



- Based on a lumped DFB model with rate equations taking into account nonlinearities[1]
- The 3-dB BW is approximately 17 GHz @ a bias current of 50 mA

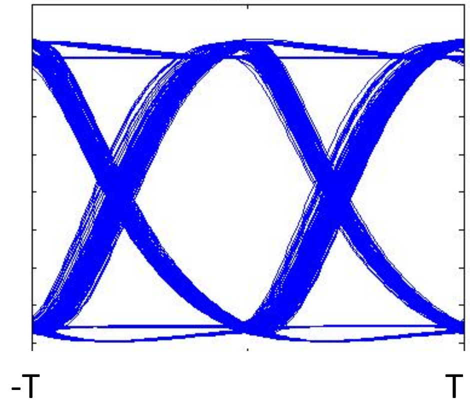
Laser Model 2: Gaussian response



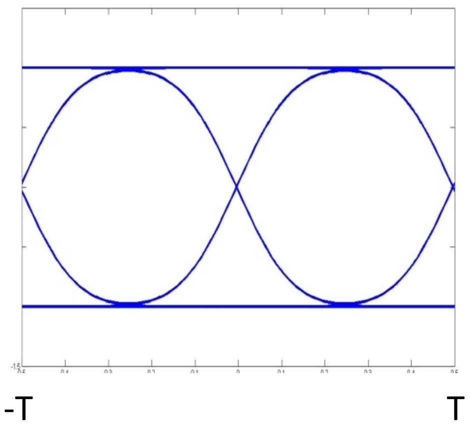
- The 3-dB BW is approximately 18.6 GHz
- Laser nonlinearity is not considered, indicating that the DML induced distortion can be compensated by the receiver equalisation

[1] J.M. Tang, et al, J. Lightwav. Technol., vol. 24 no. 1, 2006

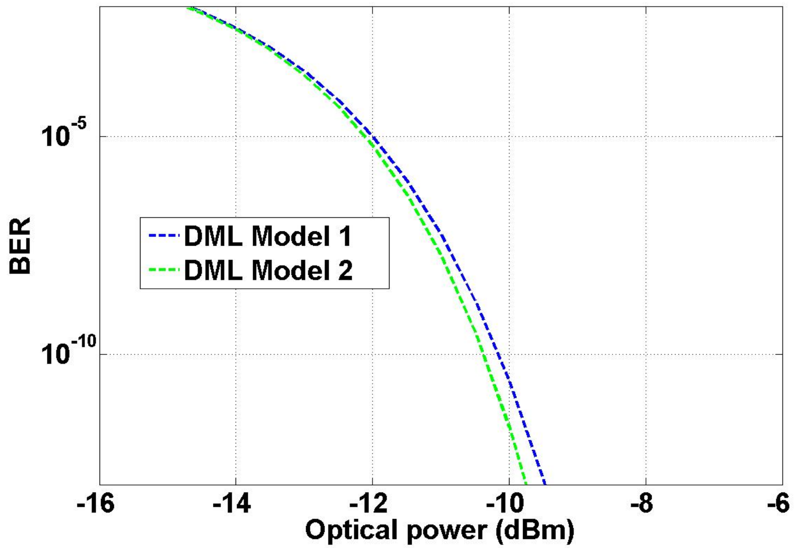
Reference 28 Gb/s NRZ System Using both Laser Models



Output of DML (Model 1)

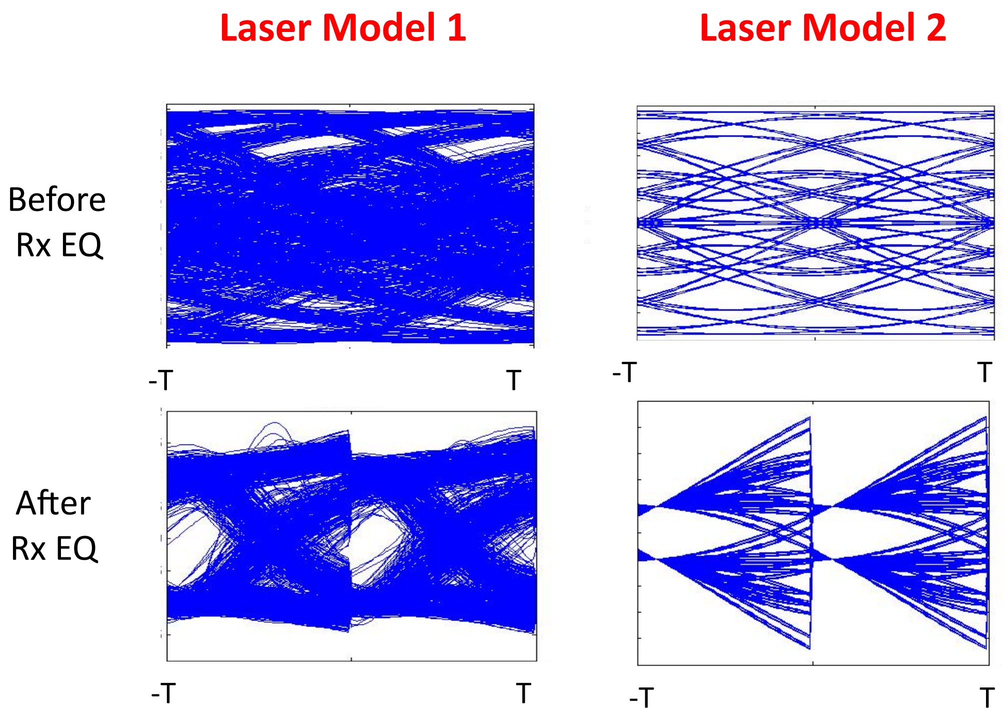


Output of DML (Model 2)

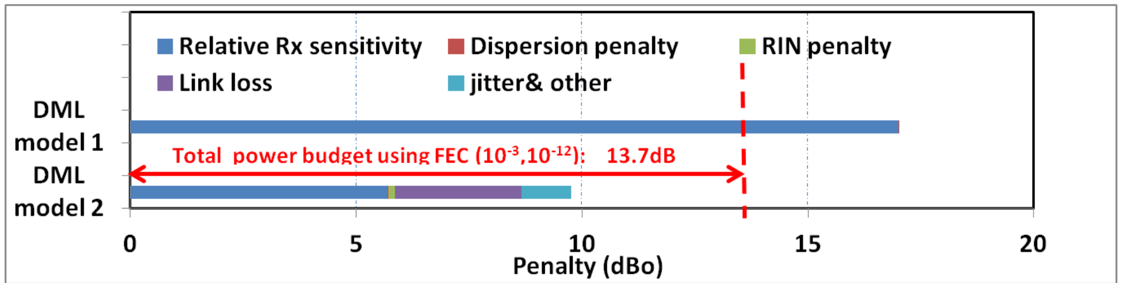


- Sensitivity is -10 dBm @ BER = 10^{-12}
- The DML nonlinearity causes a power penalty of ~0.3 dB @ BER = 10^{-12} , indicating DML model 2 can be used.
- Similar DML nonlinearity penalty of < 1 dB is also observed in 100 Gb/s CAP-16/CAP-64 and QAM-16-OFDM/QAM-64-OFDM

100 Gb/s NRZ System using both Laser Models

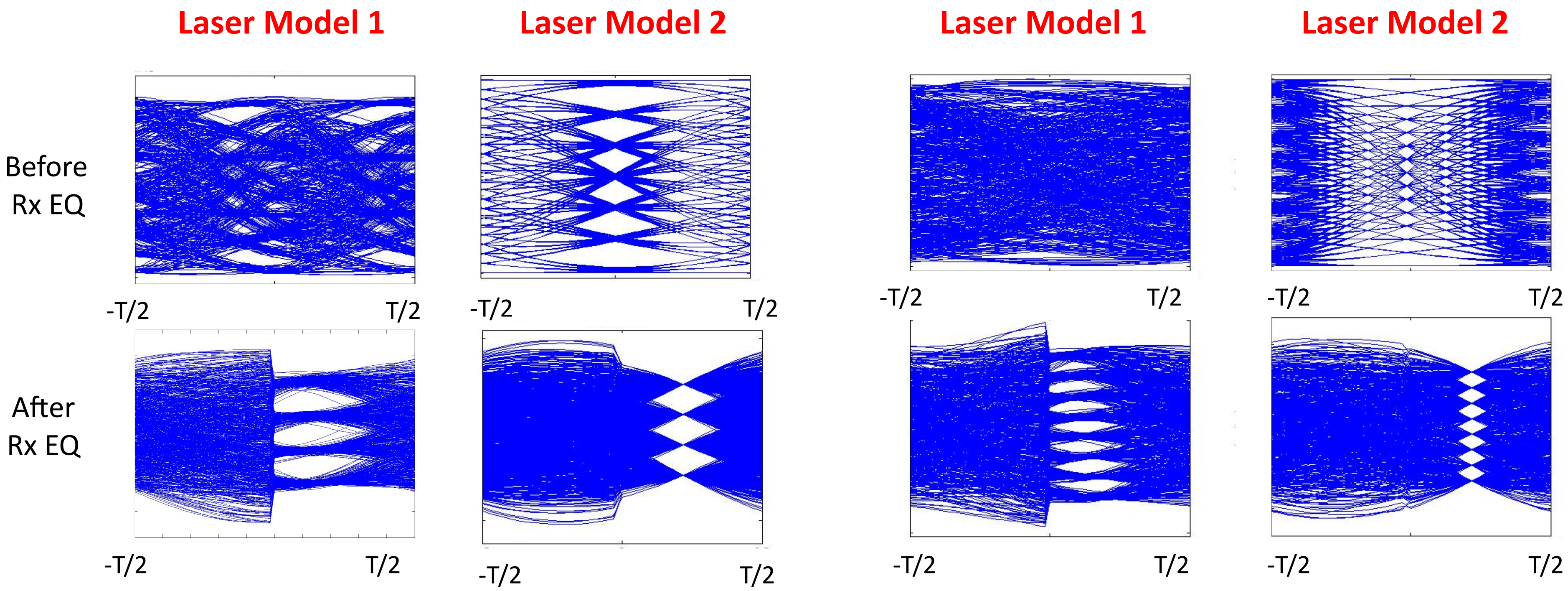


20 taps T/4 spaced FFE +3 taps DFE and 2km SMF

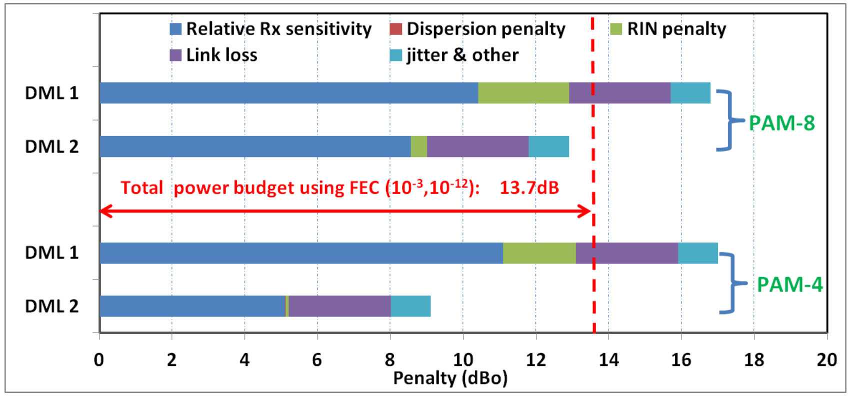


- The difference in terms of system power budget is huge
- The DML nonlinearity is significant and 100 Gb/s NRZ fails as the power budget does not satisfy the requirement
- Verifies the rules of thumb

100 Gb/s PAM Systems using both Laser Models

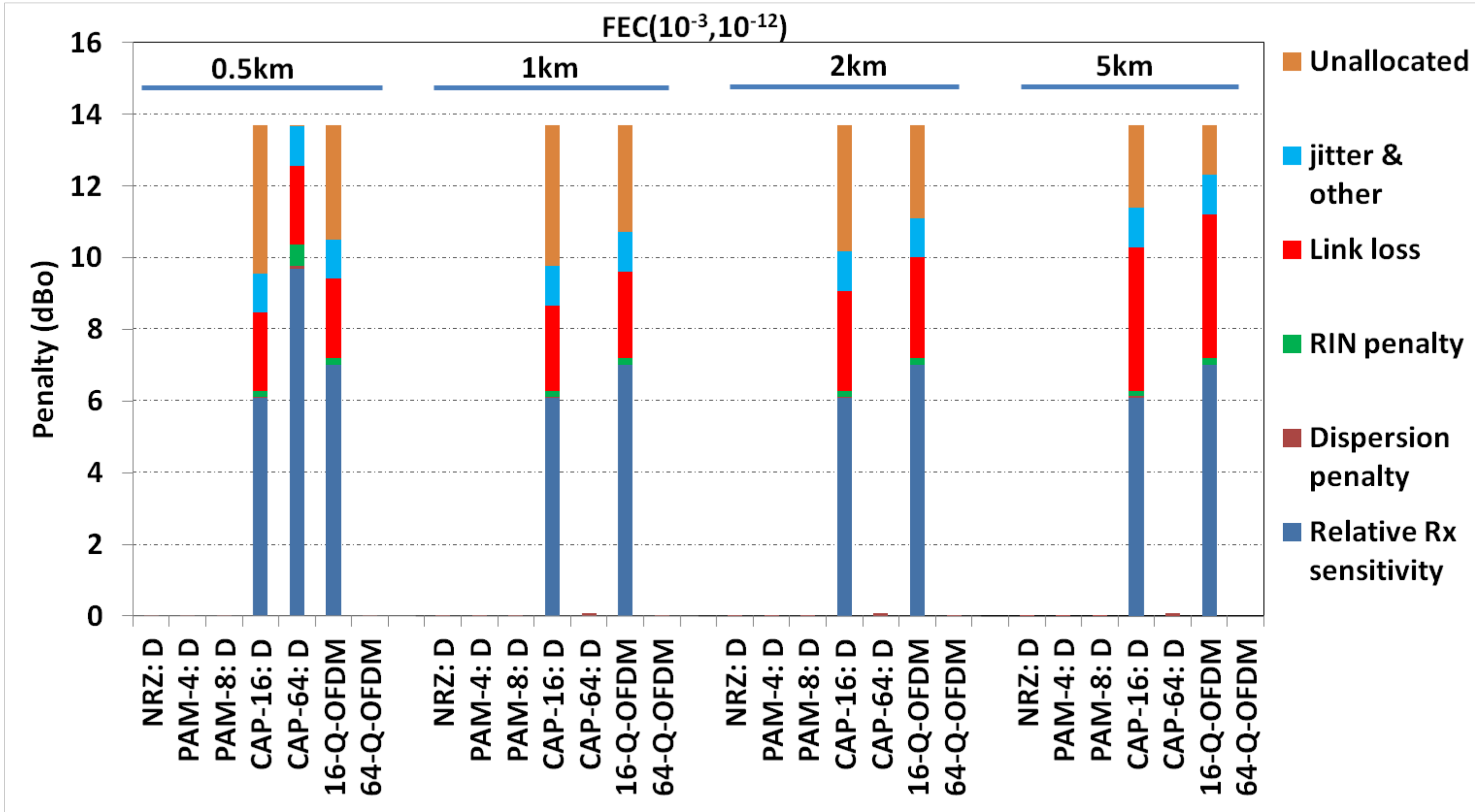


20 taps T/4 spaced FFE + 3 taps DFE and 2 km SMF



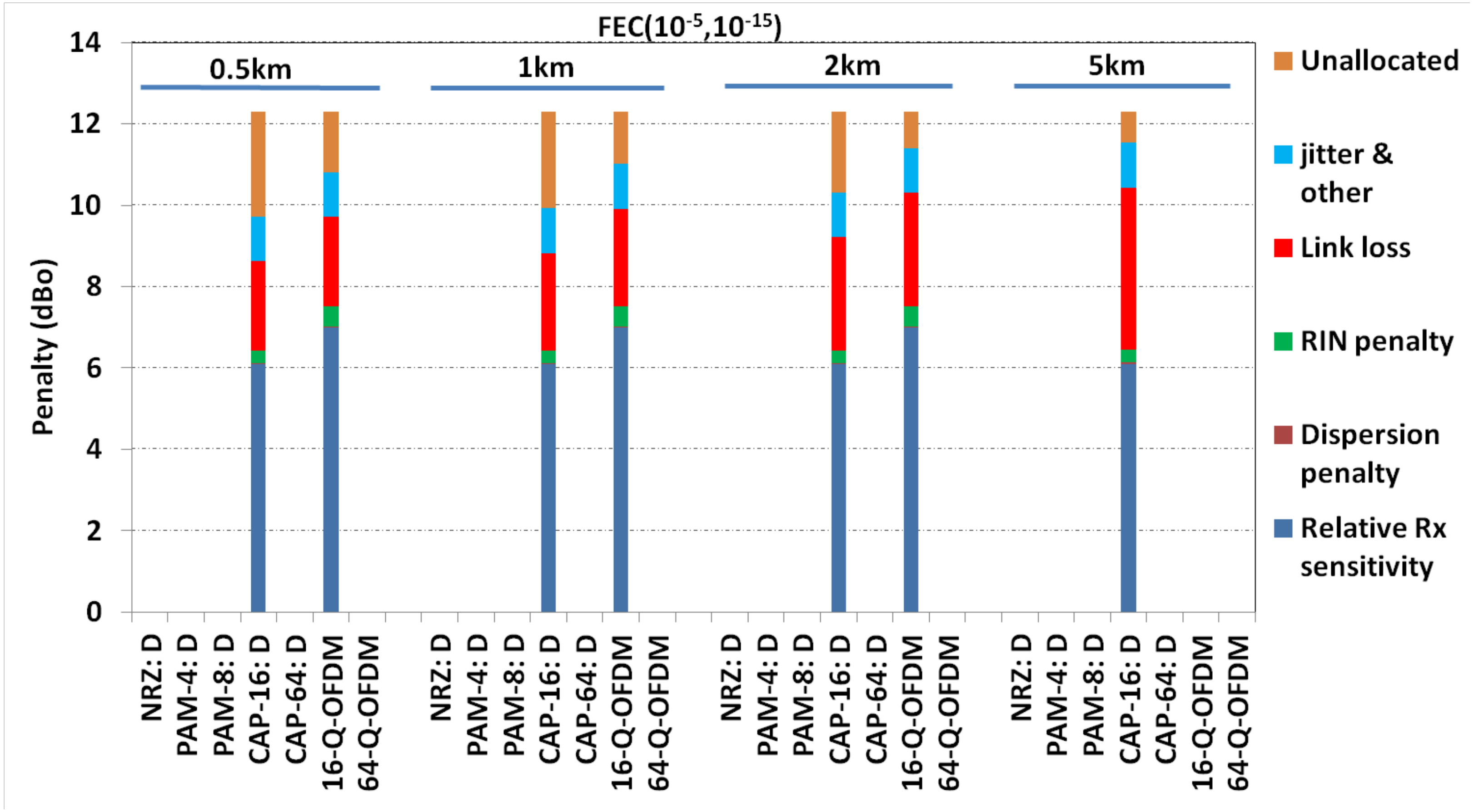
- Similarly to NRZ, PAM-4 and PAM-8 also fail when taking into account DML nonlinearity
- Verifies the rules of thumb
- CAP and OOFDM are the only survivors if using DMLs
- By default, for DML case, Laser Model 1 is used in NRZ and PAM systems and Laser Model 2 is used for CAP and OOFDM systems. For MZM case, Laser Model 2 is used for all schemes

Link Power Budget Performance using *DMLs* and FEC(10^{-3}, 10^{-12})



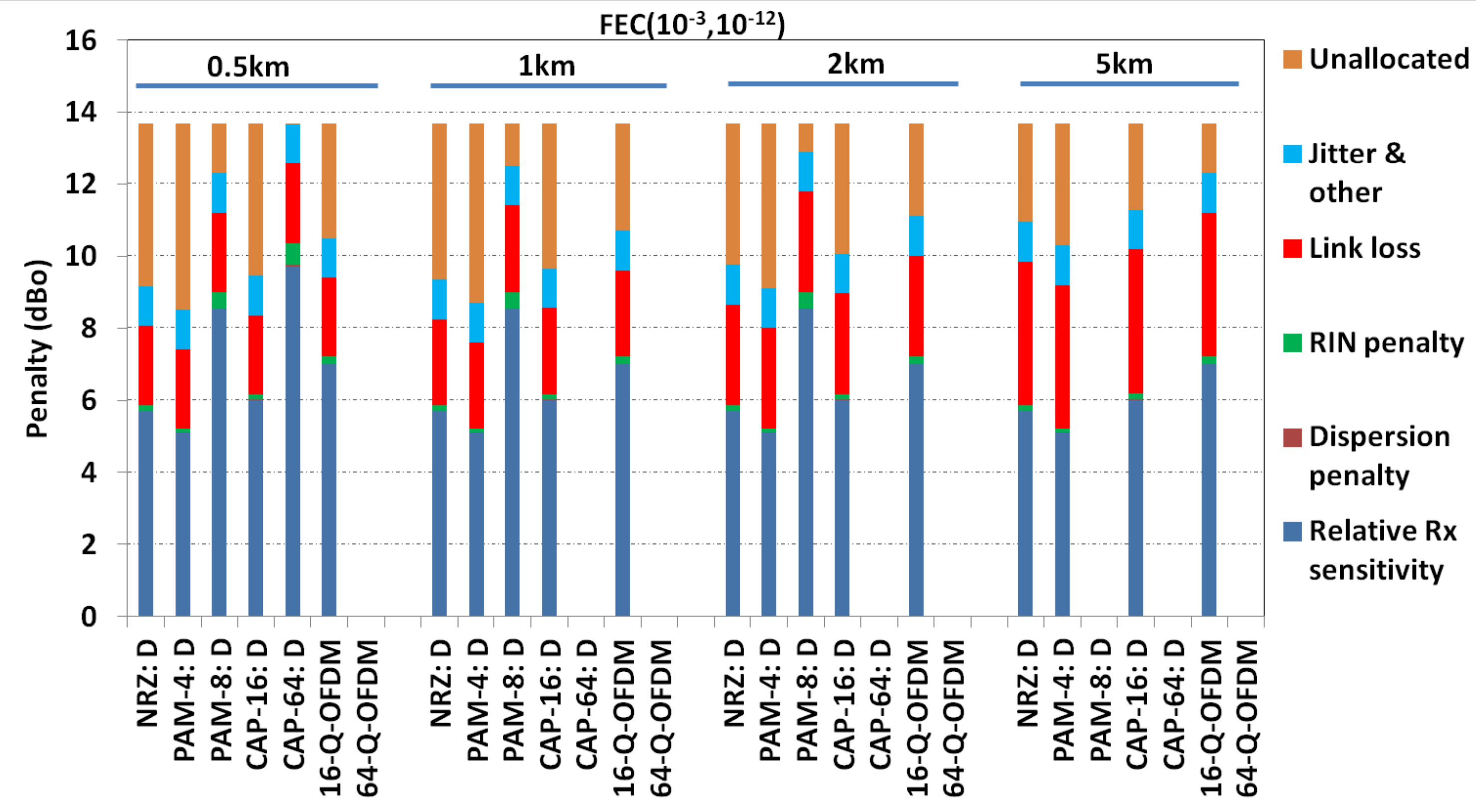
- FEC(10^{-3}, 10^{-12}) means that a BER of 10^{-12} is achievable given that the input BER is 10^{-3}
- The total link power budget is 13.7 dB
- D: FFE-DFE containing 20 taps T/4 spaced FFE and 3 taps DFE

Link Power Budget Performance using *DMLs* and FEC(10^{-5}, 10^{-15})



- FEC(10^{-5}, 10^{-15}) means that a BER of 10^{-15} is achievable given that the input BER is 10^{-5}
- Total link power budget is 12.3 dB
- D: FFE-DFE containing 20 taps T/4 spaced FFE and 3 taps DFE

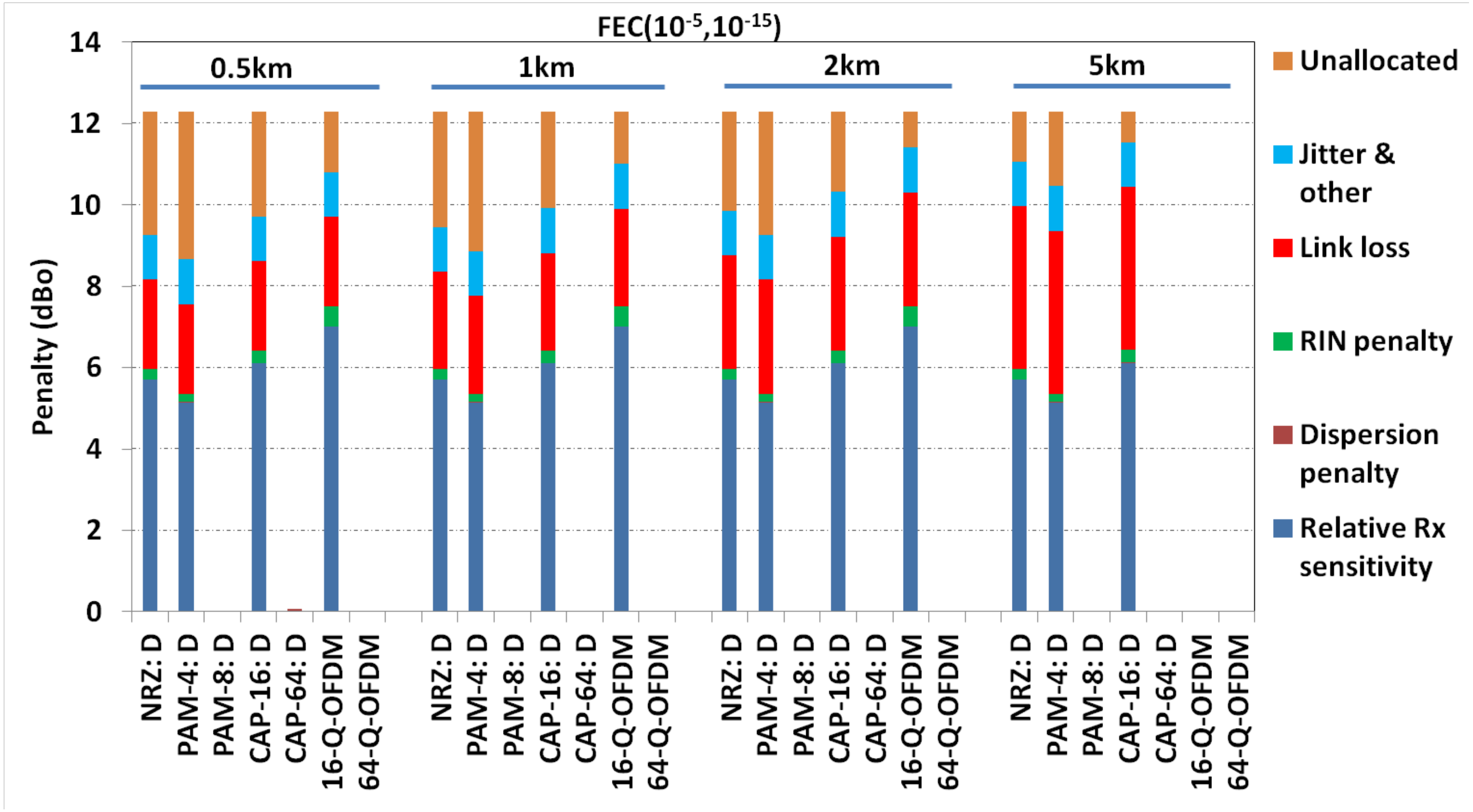
Link power budget performance using *MZMs* and FEC(10^{-3}, 10^{-12})



- ❑ Laser Model 2 is used for all modulation formats
- ❑ The nonlinear P-I curve of MZM can be compensated by unequal symbol mapping[1], thus is ignored
- ❑ The total link power budget is 13.7 dB
- ❑ D: FFE-DFE containing 20 taps T/4 spaced FFE and 3 taps DFE

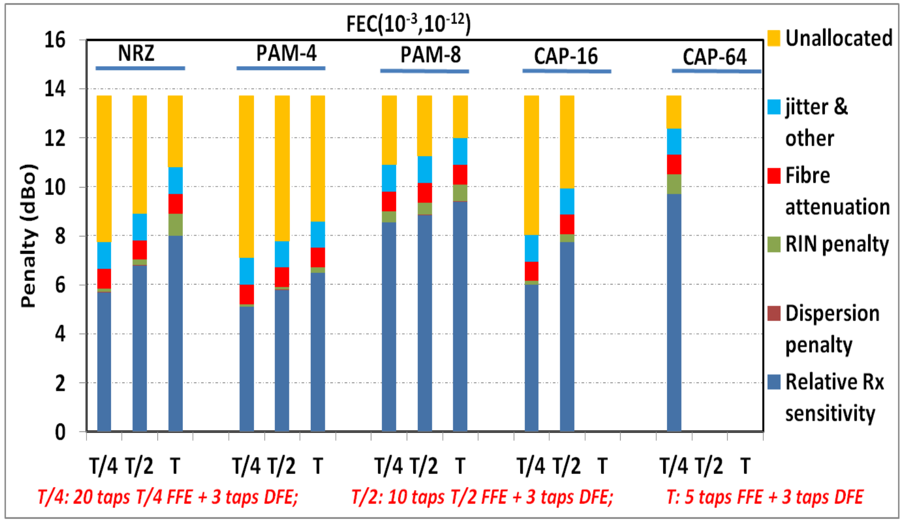
Ref [1] G. Nicholl, et al, "Update on technical feasibility for PAM modulation" IEEE 802.3 NG 100GE PMD study group, Mar. 2012

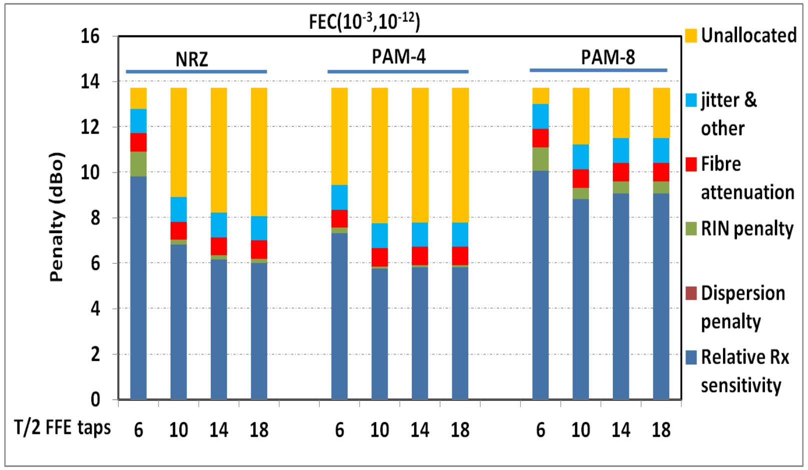
Link Power Budget Performance using *MZMs* and FEC(10^{-5}, 10^{-15})



- ❑ Laser Model 2 is used for all modulation formats
- ❑ Total link power budget is 12.3 dB
- ❑ D: FFE-DFE containing 20 taps T/4 spaced FFE and 3 taps DFE

The Effect of FFE Tap Spacing and Tap Count on System Performance

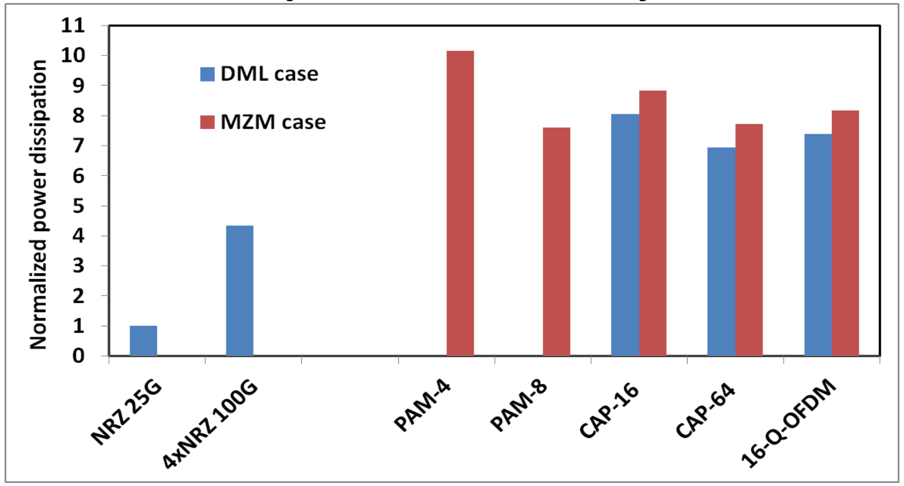




- ❑ FFE tap spacing of T/4, T/2 and T are considered and MZMs with 2 km SMF are used for all systems
- ❑ The achievable power margin decreases with increasing tap spacing
- ❑ There is trade off between achievable power margin and Rx signal oversampling required

- ❑ FFE tap spacing of T/2 is considered here and MZMs with 2 km SMF are used for all systems
- ❑ There is an optimum FFE tap count beyond which the optical power budget does not improve

Estimated Power Dissipation for Systems using MZMs



	PAM-4	PAM-8	CAP-16	CAP-64	QAM-16-OFDM
DAC/ADC (GS/s)	100	66.7	75*	50*	55

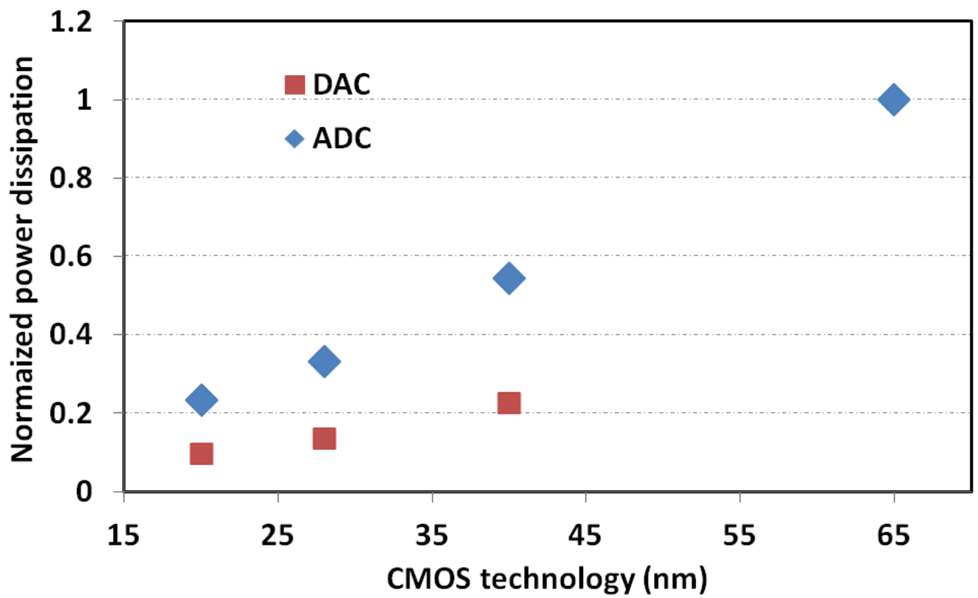
* The Nyquist sampling rate given by 2*(1+roll_off_factor)*symbol_rate, with roll_off_factor being 0.5

- Power dissipation estimation is based on 65 nm CMOS technology
- The power dissipations of PAM, CAP and OFDM transceivers are dominated by the DAC/ADC
  - ✓ For example, for CAP-16 (16-QAM-OFDM) with a single-channel configuration, the DAC/ADC power consumption accounts for 55% (48%) of that for the overall transceiver
- DAC/ADC power dissipation is extrapolated from Fujitsu 55G-65G DAC and 56G ADC product sheets[1], and the assumption is made that its power consumption is linearly dependent on the sampling rate
- CAP implemented without DAC/ADC consumes less power than a 4×25 Gb/s NRZ 100 Gigabit Ethernet system, indicating great potential for high power-efficiency

[1] Fujitsu factsheet, http://chais.info

Potential Lower Power Dissipation for DAC/ADC

Extrapolated ADC/DAC power dissipation based on Fujitsu CMOS design



Source: Kenn Liu, Hui, "Enable 100G- Key Technology for 100G Transport Network ASIC" , ICCAD2010. available at http://www.slideshare.net/kennliu/fujitsu-iccad-presentationenable-100g?from=share_email

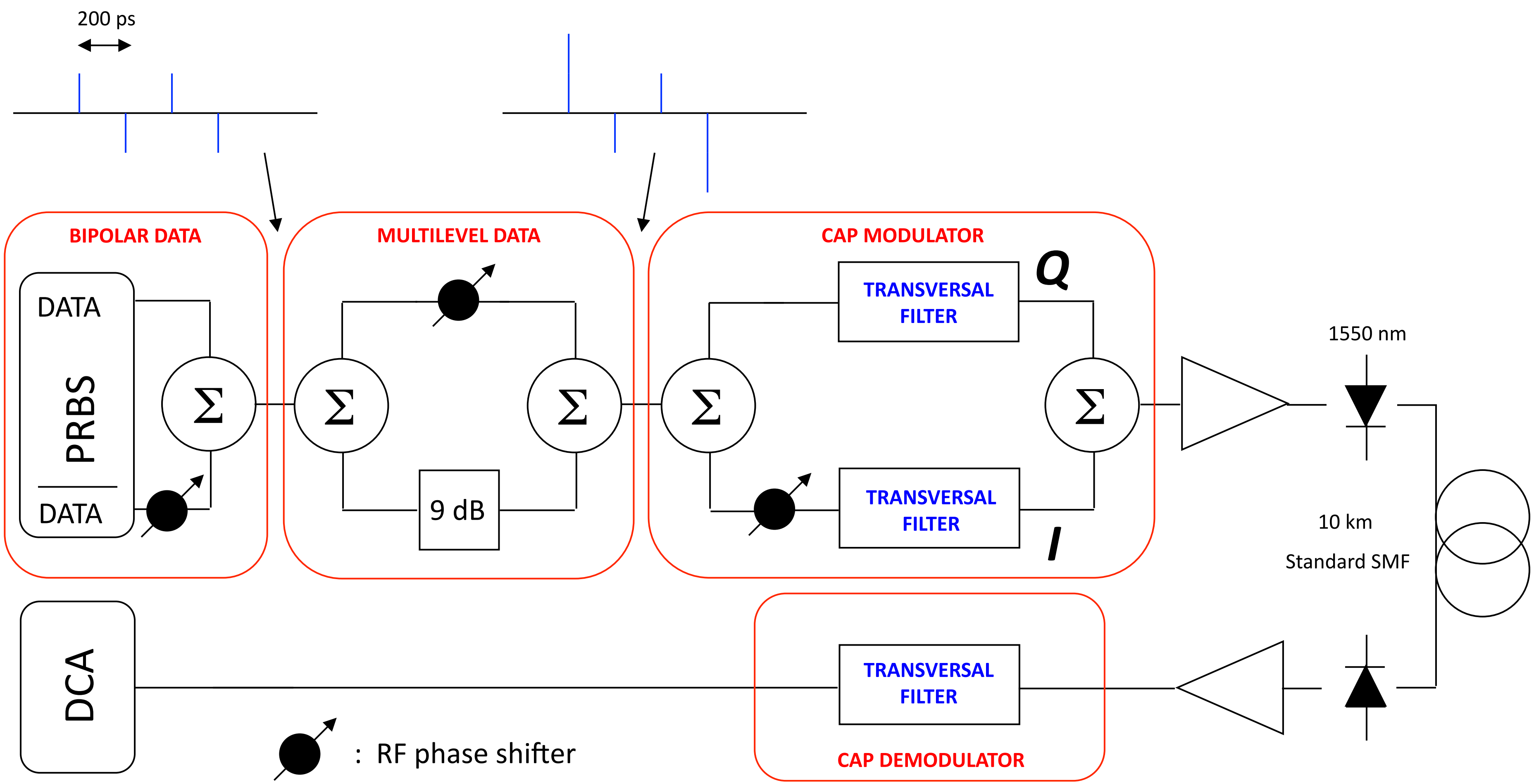
- The power consumption for ADC is almost halved using 40 nm CMOS technology compared to 65 nm CMOS
- Further reduction of power dissipation of the proposed systems is predictable
  - For example, when 20 nm CMOS technology is used, the power dissipation for a CAP-16 transceiver is close to that of a 4 × 25Gb/s NRZ 100 Gigabit Ethernet system

Experimental Studies of CAP-16

Two approaches considered:

- 40 Gb/s CAP-16 using integrated transversal filters for encoding and decoding
- 50 Gb/s CAP-16 using integrated XOR gate for encoding and discrete transversal filter for decoding

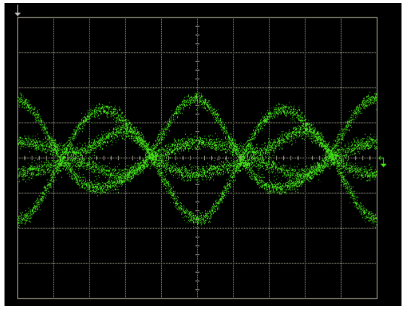
40 Gb/s CAP-16 – Experimental Arrangement



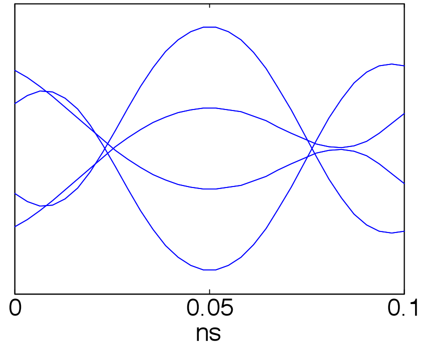
40 Gb/s CAP-16 - Encoding

Integrated transversal filter with tap spacing ≈ 25 ps (≈ 5 taps required)

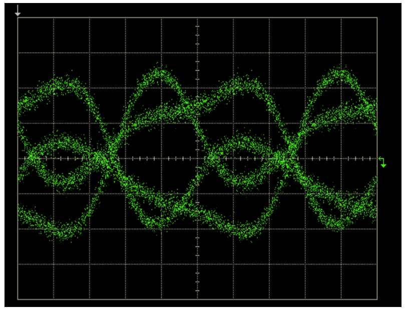
In-phase channel



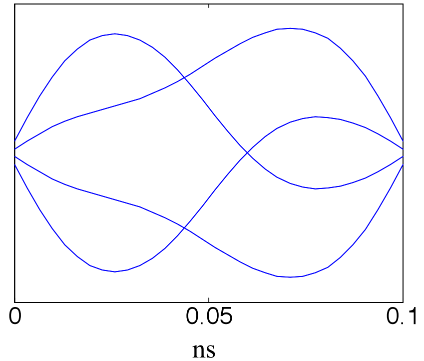
20 ps/div



Quadrature channel



20 ps/div

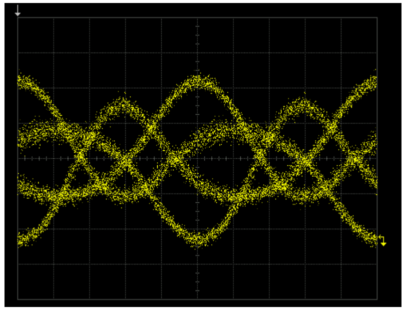


Good agreement with simulated pulse shapes

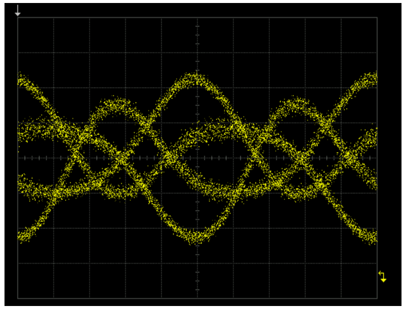
40 Gb/s CAP-16 - Decoding

Back to back | 10 km SMF

In-phase channel

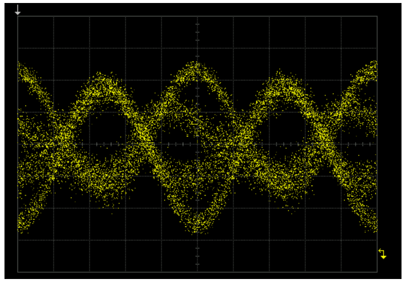


20 ps/div

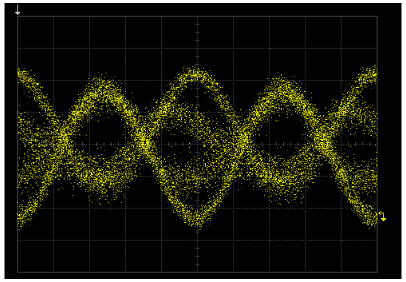


20 ps/div

Quadrature channel



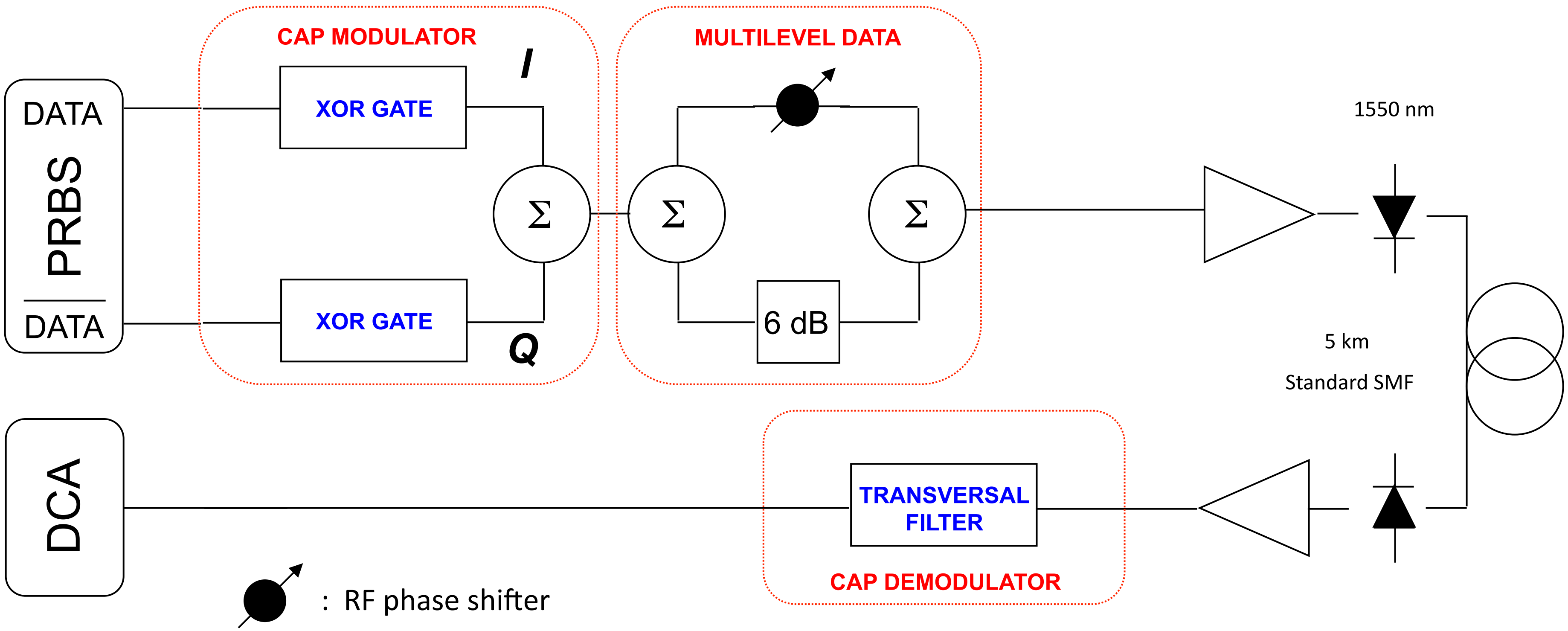
20 ps/div



20 ps/div

After 10 km SMF transmission, the 4-level decoded eye diagrams have *Q* factors:
6.2, 6.1 and 6.4 (in-phase channel)
3.0, 4.1 and 3.5 (quadrature channel)

50 Gb/s CAP-16 – Experimental Arrangement



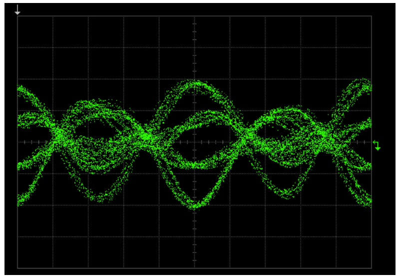
Discrete transversal filter (3 taps) constructed for decoding

12.5 GHz clocks applied to XOR gates with 90° phase shift between *I* and *Q* clocks

50 Gb/s CAP-16 - Encoding

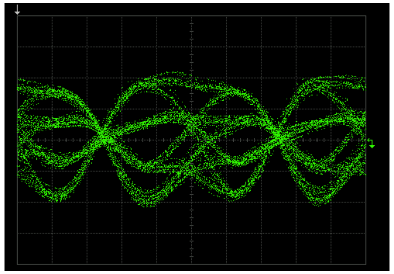
XOR gate used for encoding of $2^7 - 1$ PRBS

In-phase channel



16 ps/div

Quadrature channel

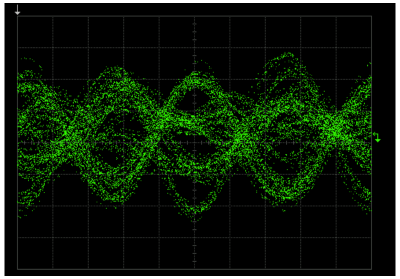


16 ps/div

50 Gb/s CAP-16 - Decoding

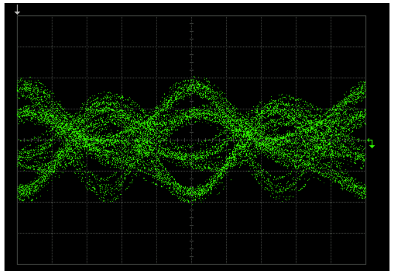
5 km SMF

In phase channel



16 ps/div

Quadrature channel



16 ps/div

After 5 km SMF transmission, the 4-level decoded eye diagrams have *Q* factors:
4.0, 3.9 and 4.3 (in-phase channel)
3.8, 4.0 and 4.0 (quadrature channel)

Conclusions

- ❑ We have established a full simulation tool to evaluate the performance of various 100 Gigabit Ethernet coding schemes

- ❑ We have theoretically demonstrated the feasibility of 100 Gigabit Ethernet PMDs enabled by NRZ, PAM-4, PAM-8, CAP-16, CAP-64 and QAM-16-OFDM over a single optical channel using MZM and FEC. The feasibility of using DML for FEC-aided CAP-16 and QAM-16-OFDM has also been explored

- ❑ Energy consumption aspects have also been considered

- ❑ We have also experimentally demonstrated CAP systems at data rates up to 50 Gb/s using both transversal-filter encoding and XOR encoding

Issues to Be Investigated in Future

- The system power penalties due to the following mechanisms have not been considered, but will be in future studies
  - Baseline wander
  - Reflection-induced interferometric noise
  - The dependence of jitter penalty on modulation format