PAM-16 Implementation Update

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IEEE 802.3 NG100GE Optics Study Group

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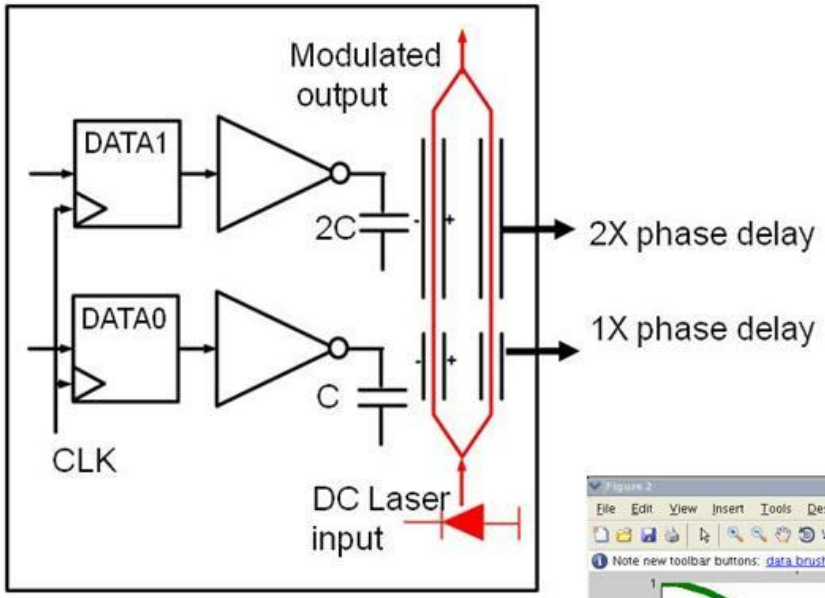
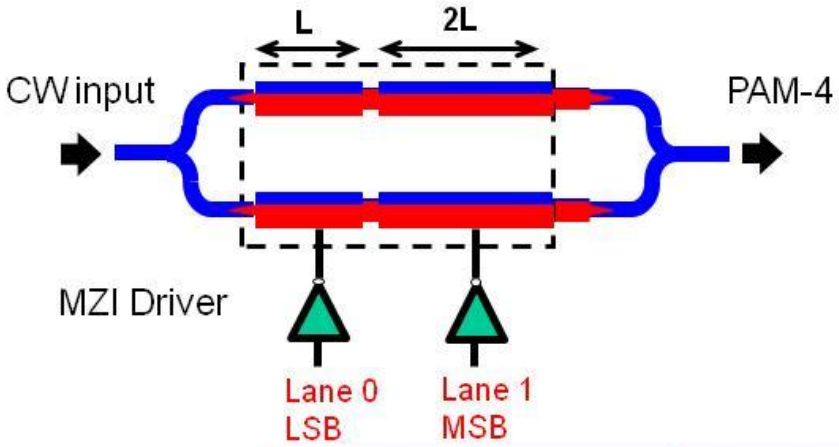
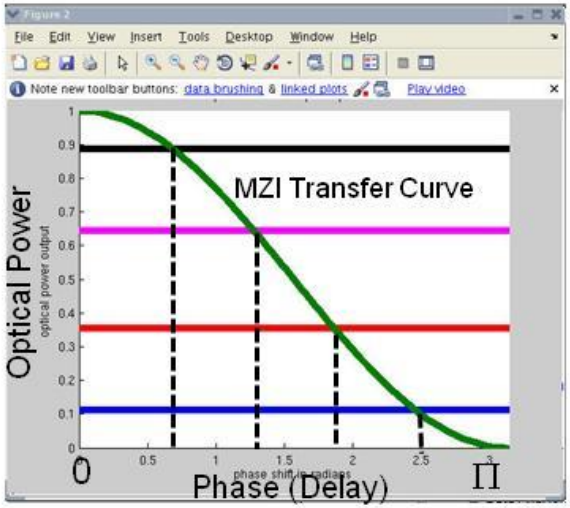
Overview

- Recap of PAM-n signaling implementation using SiP MZI
  - See dama_01_0312_NG100GOPTX.pdf
- Status update on Cisco PAM-16 10GBaud test chip

Achieving PAM Signaling with MZI (i.e.PAM-4)



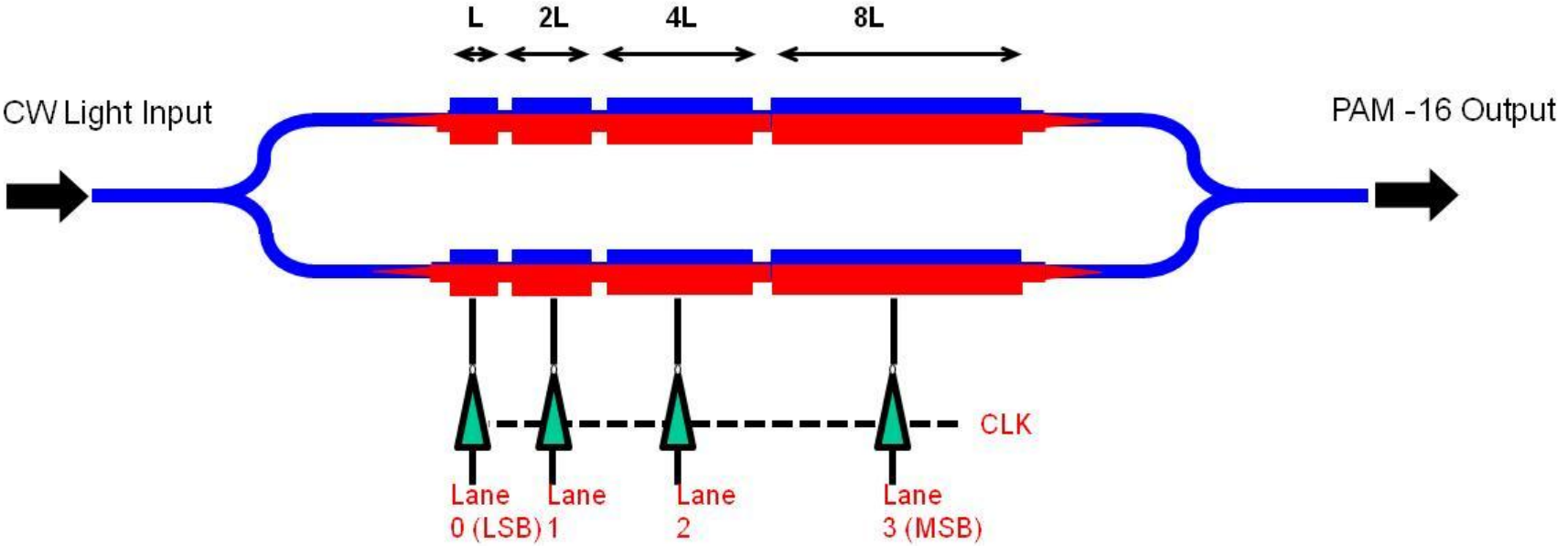




Lane 1 – Electrical MSB 0.66 ϕ	Lane 0 – Electrical LSB 0.33 ϕ	Optical Out
0	0	0
0	1	1
1	0	2
1	1	3

Segmented MZI + Simple Digital Driver > DAC function for PAM

Segmented MZI Extended to PAM-16

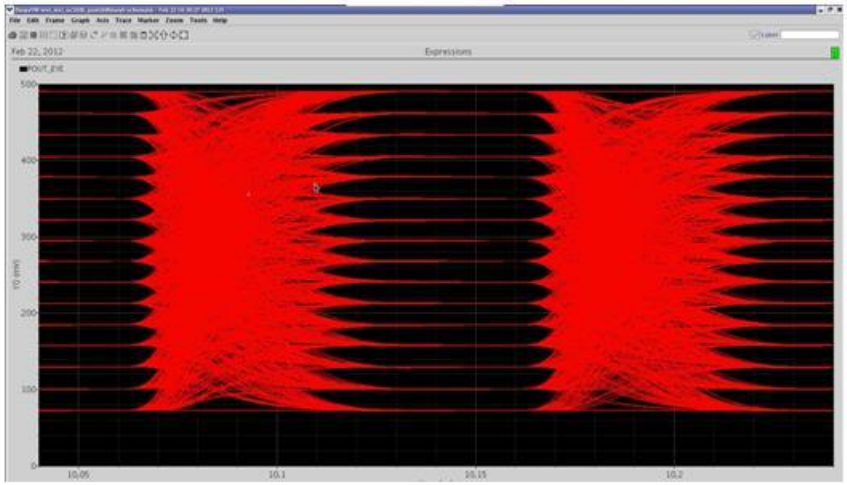


Lane 3 MSB	Lane 2	Lane 1	Lane 0 LSB	Optical Out
0	0	0	0	0
0	0	0	1	1
-	-	-	-	-
1	1	1	1	15

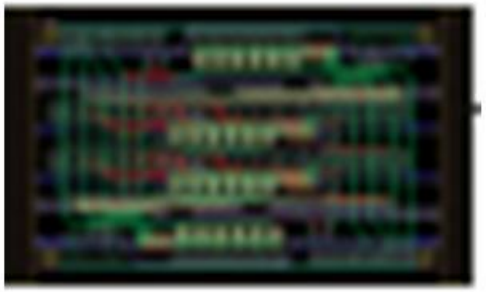
- Electrically: 4 CMOS inverters driving 4 capacitors
- Optically: Continuous waveguide, where 4 segments contribute phase shift proportional to their length
- Need to line-up electrical transitions across all 4 lanes (i.e. re-timed driver)

Tx Optical PAM-16 Realization

PAM16 @10 Gbaud (40Gbps) **



- 10G TX Optical Simulations
- Design completed
- ICs in fabrication

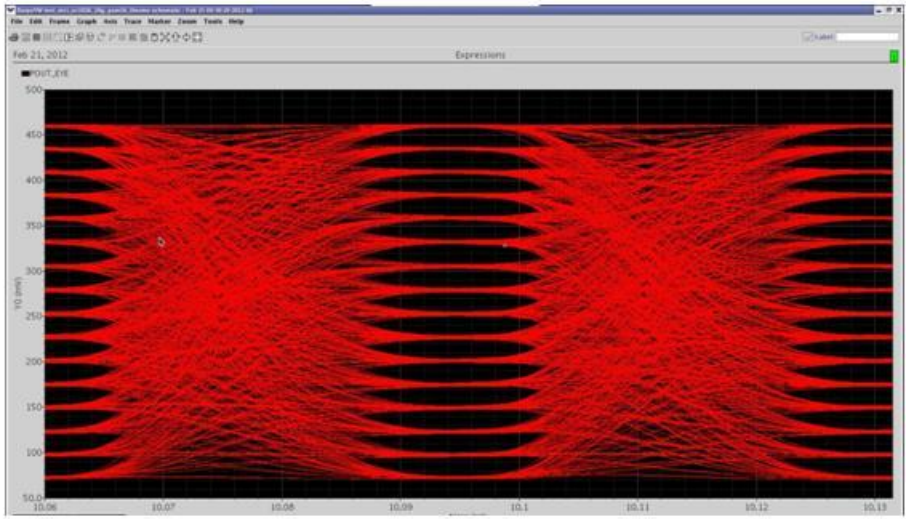


IC Size:

~2mm x ~1mm

- IC includes PAM-16 MZI + more structures

PAM 16 @ 28 Gbaud (112 Gbps)



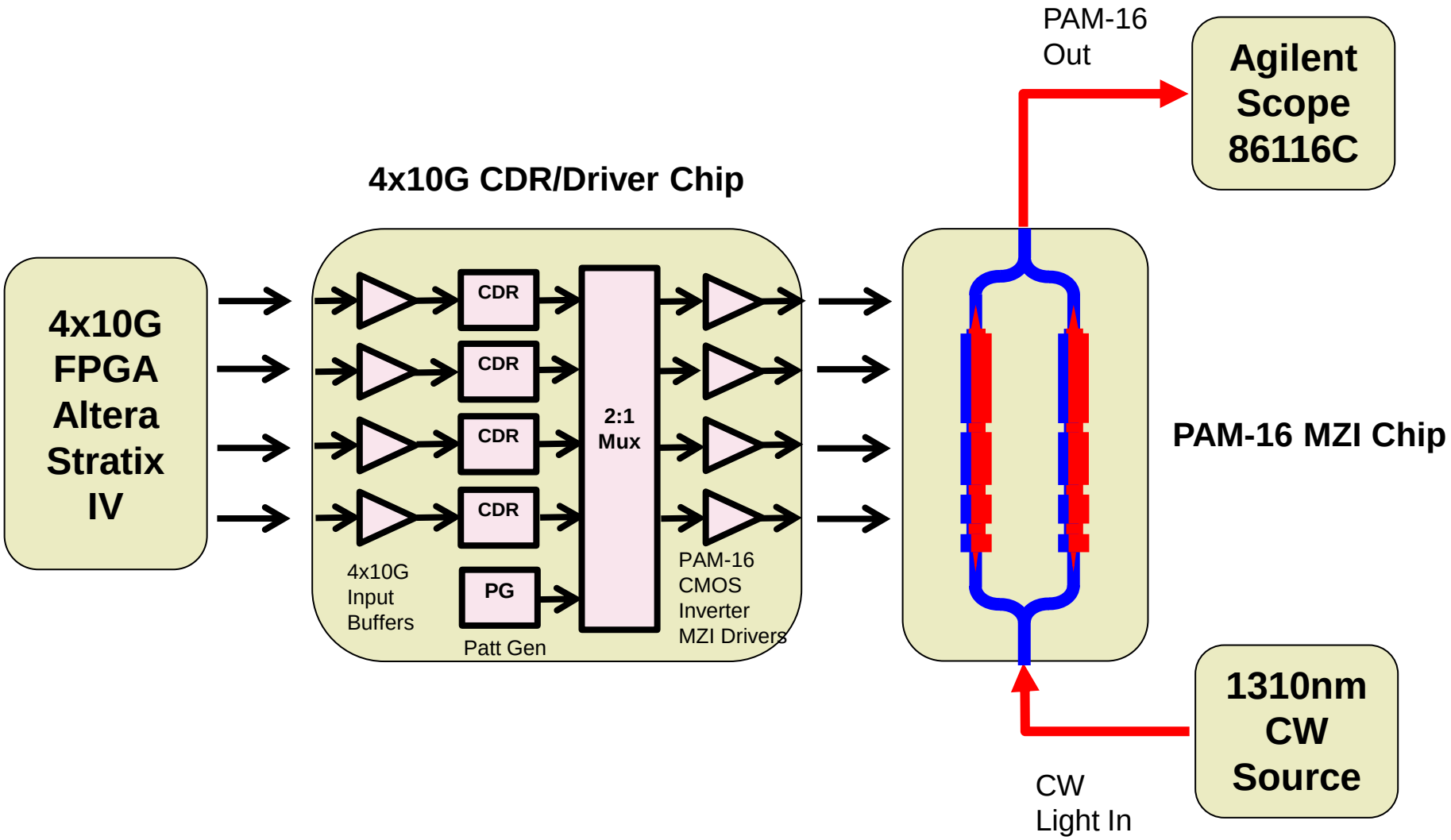
- 28G Simulations
- Further design optimization possible

** Darpa Contract

Cisco PAM-16 10GBaud Test Chip - Update

- Test chips received from Fab
  - 4x10G CDR/Driver IC (40nm CMOS)
  - PAM-16 MZI IC (SiPhotonics)
- Test chips mounted onto Eval board
- Test station in the process of being assembled
- Will have initial results to share in July

Test Setup


PAM-16
Out
Agilent
Scope
86116C
4x10G CDR/Driver Chip
4x10G
FPGA
Altera
Stratix
IV
CDR
CDR
CDR
CDR
PG
2:1
Mux
4x10G
Input
Buffers
Patt Gen
PAM-16
CMOS
Inverter
MZI Drivers
PAM-16 MZI Chip
1310nm
CW
Source
CW
Light In

PAM-16 Eval Board

Eval Board