# Application Space of CAUI-4/ OIF-VSR and cPPI-4

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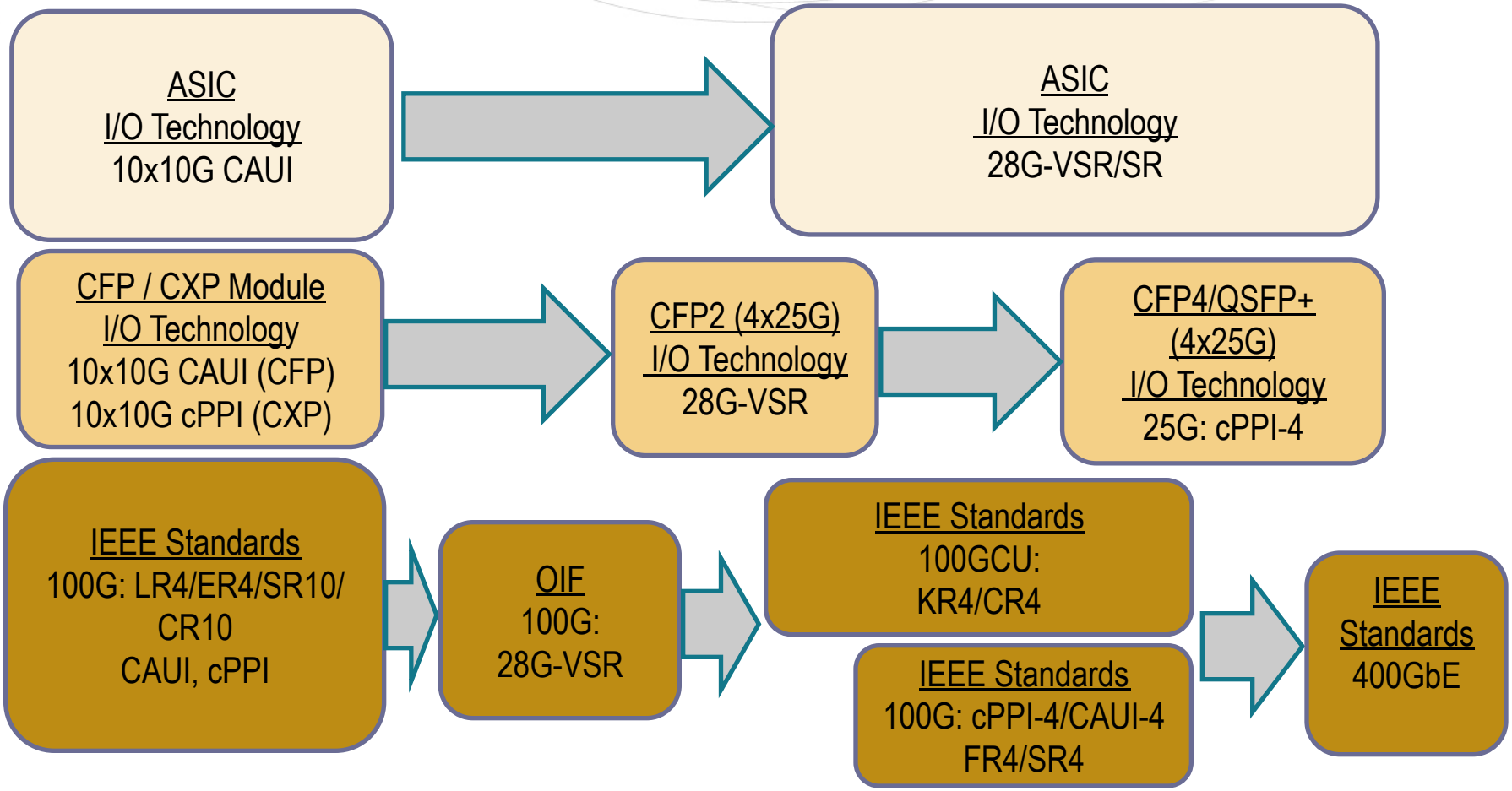
# Overview

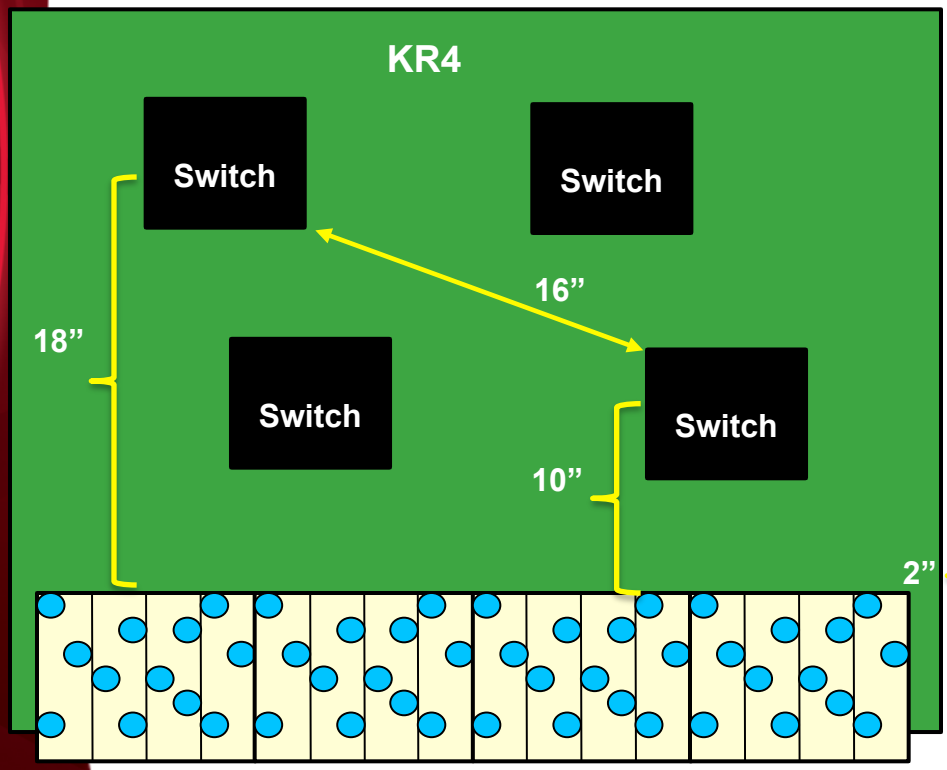
- I/O Trend
- Line card implementations
- VSR/CAUI-4 application model
- cPPI-4 application model
- VSR loss budget
- Possible CAUI-4 loss budget
- cPPI-4 simulations and measurements
- Measurements result of 100G-LR4 link operating unretime
- Credits
  - TE formally known (Tyco Electronics) for providing test board and connector models
  - Finisar corporation for joint 100Gbase-LR4 testing but Finisar corporation has no specific position on the content of this presentation.

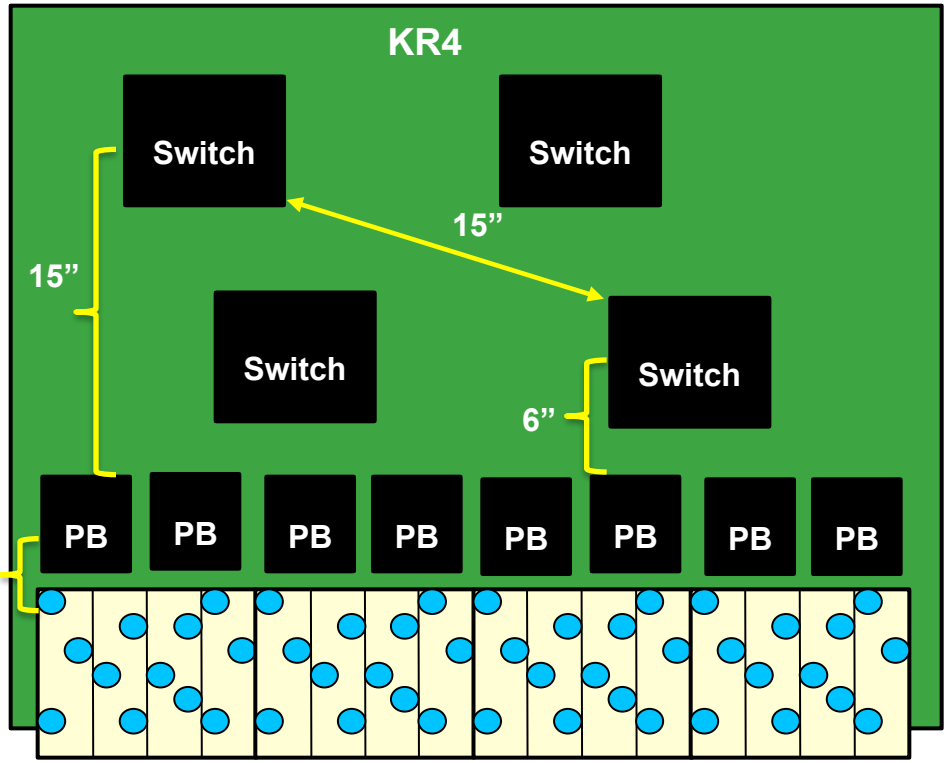
# 100GbE I/O Trends



# Typical Line Card on a Scalable System

- Requirement to simultaneously drive the backplane increases the distance to front panel ports
- Line card chip to chip application require at least 15” of PCB with one connector which is inline with OIF-28G-SR

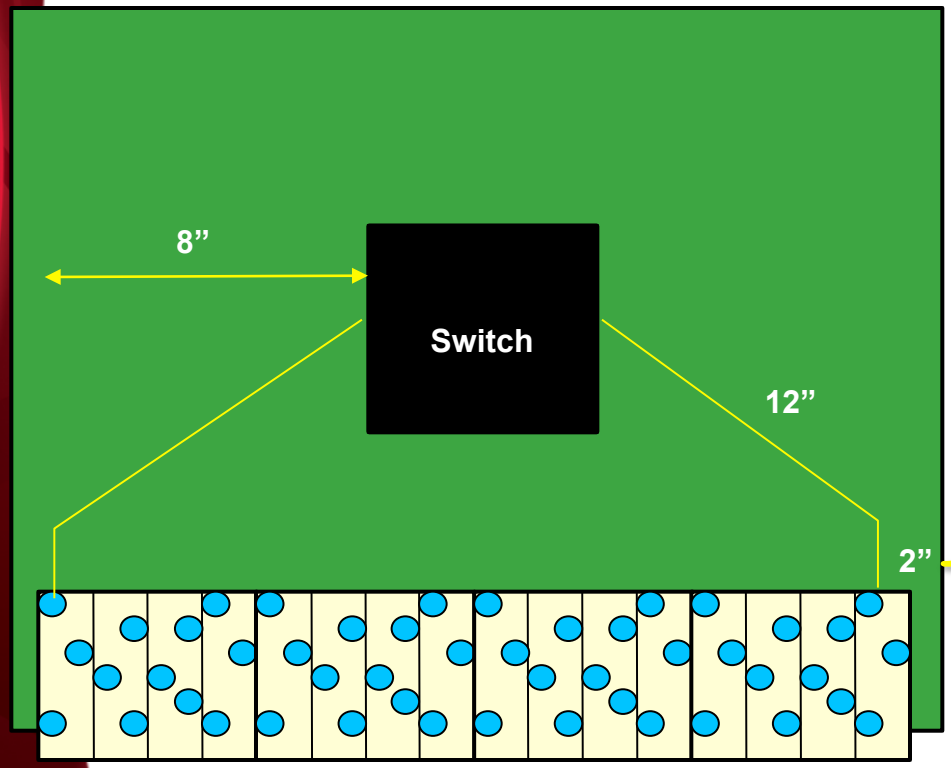


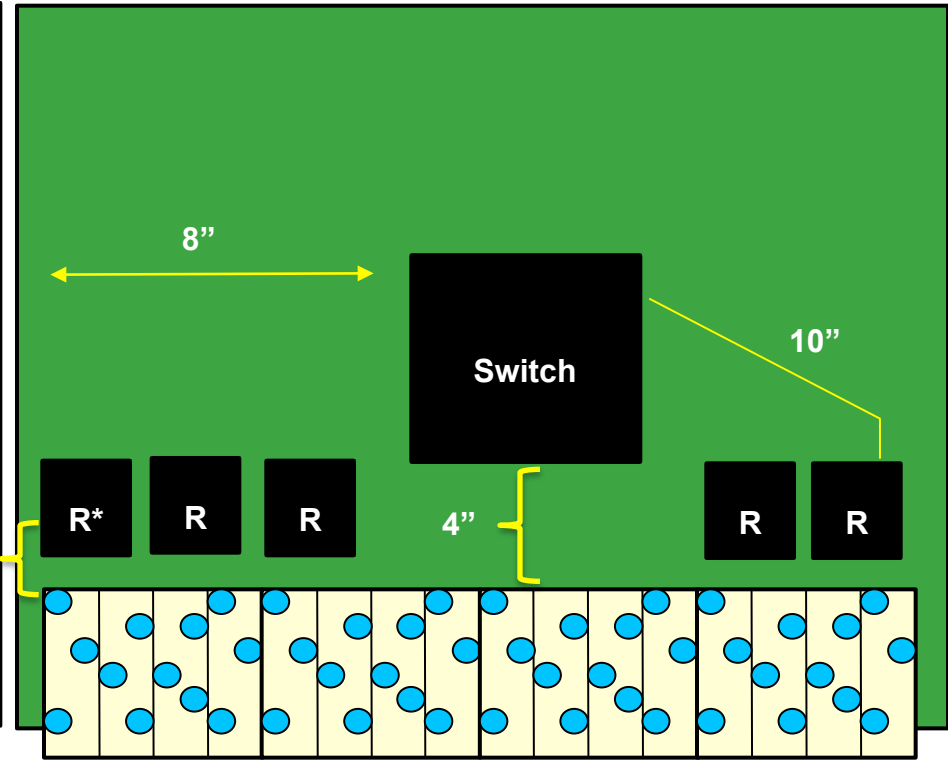




* PB is port buffer and may contain one or more of the following memory, MACSec, Time stamp, etc.

# Typical Top of the Rack Switch

- Top of the rack switch aggregate server uplinks operating at 100G
- If single ASIC was driving all front panel ports 12” host PCB is required and roles out Cu cabling
  - Alternative approach is to use external retimer when needed at external retimers and support 40G/100G Cu cabling

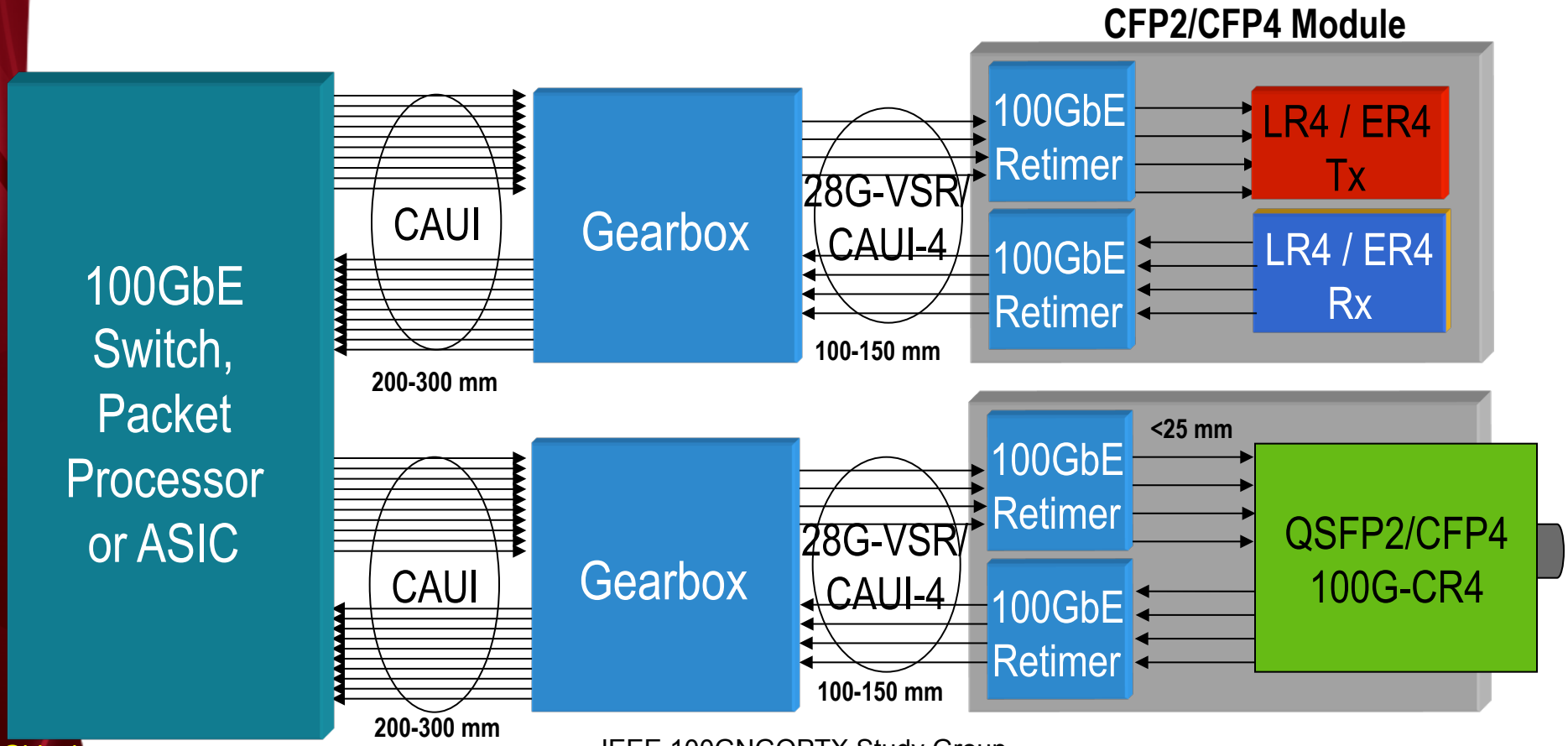



* R is retimer

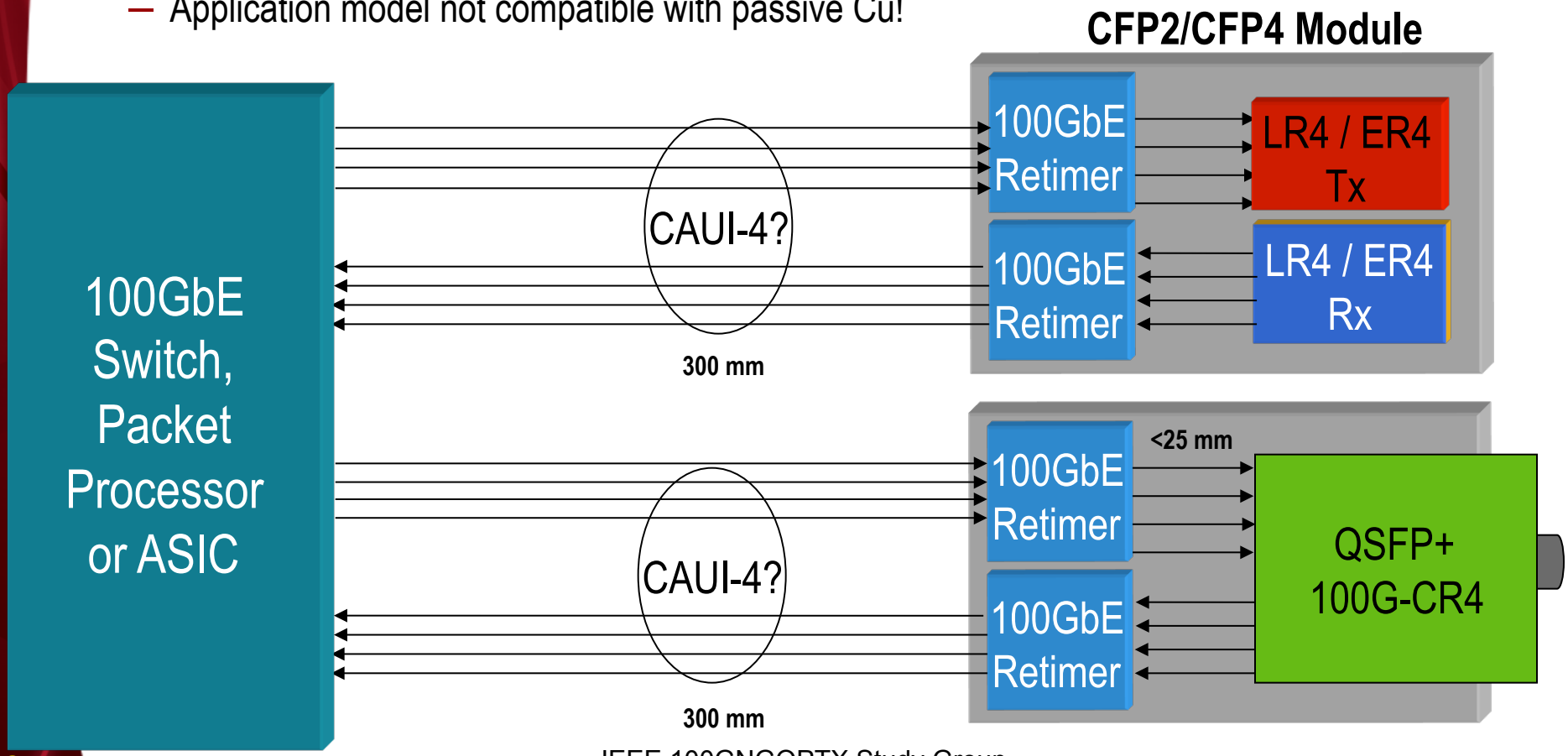
# Current Retimed Applications with "CFP2"

- CFP2 is retimed interfaced designed for LR4/ER4 but could be retrofitted to support 100G-CR4/SR4 as well
- OIF 28G-VSR only supports 4-6" of PCB and not sufficient for general CAUI chip to chip application where OIF 28G-SR is currently targeted



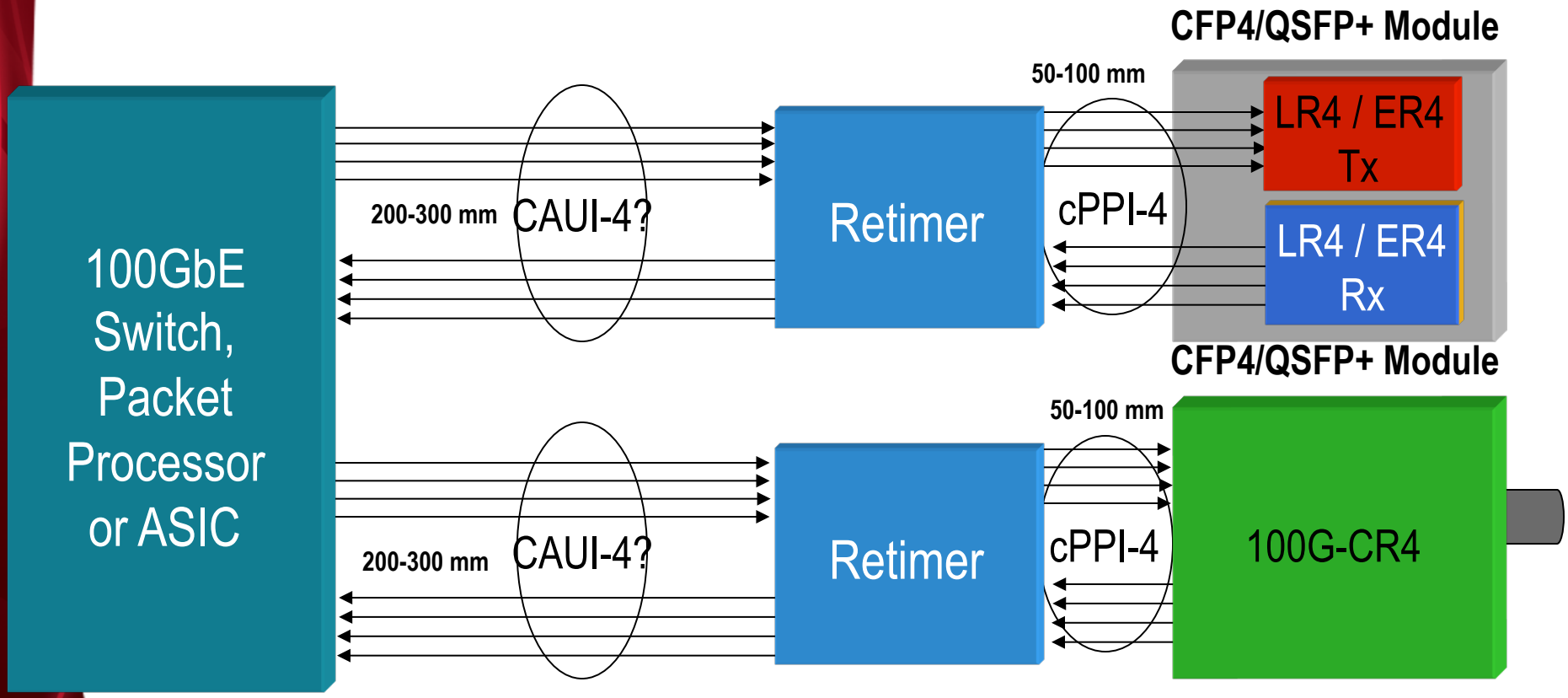
# Possible Applications of CFP2

- **The 200-300 mm host PCB with one connector would be required**
  - Can VSR 10 loss budget enhanced without substantial power increase
  - A retime module to ASIC interface need to support 300 mm of host and would not be compatible with current retime interface OIF-28G-VSR
  - Application model not compatible with passive Cu!



# Next Generation Implementation Based on cPPI-4

- cPPI-4 is unretimed interfaced will be designed to support LR4/ER4 as well as new PMD's in development 100G-CR4/SR4
- The 200-300 mm is more inline with OIF 28G-SR, can we retrofit OIF VSR to meet CAUI-4 chip to chip application as well?



# The Crystal Ball is not so clear!

- **VSR already has defined a retiemd 10 dB interfaced**
  - VSR could be enhanced to about 12 dB and still be compatible
- **To support retime back to one large ASIC or chip to chip applications an OIF 28G-SR loss budget (15.4 dB) is needed**
  - For a pluggable non-engineered link CTLE receiver is not sufficient!
- **OIF VSR was created because OIF-SR was too high a power**

| Host Trace Length * | Total Loss (dB) | Host Loss(dB) | FR4-6 | N4000-13 | N4000-13SI | Megtron 6 |
|---|---|---|---|---|---|---|
| Nominal PCB Loss at 28G/in | N/A | N/A | 2.0 | 1.5 | 1.2 | 0.9 |
| OIF 28G-LR with two connector | 25.5 | 23.1 | 11.6 | 15.4 | 19.3 | 25.7 |
| OIF 28G-SR with one connector & HCB | 15.4 | 12.5 | 6.3 | 8.3 | 10.4 | 13.9 |
| OIF 28G-VSR with one connector & HCB | 10 | 7.1 | 3.6 | 4.7 | 5.9 | 7.9 |
| cPPI-4 with one connector & HCB | 7 | 4.1 | 2.1 | 2.7 | 3.4 | 4.6 |

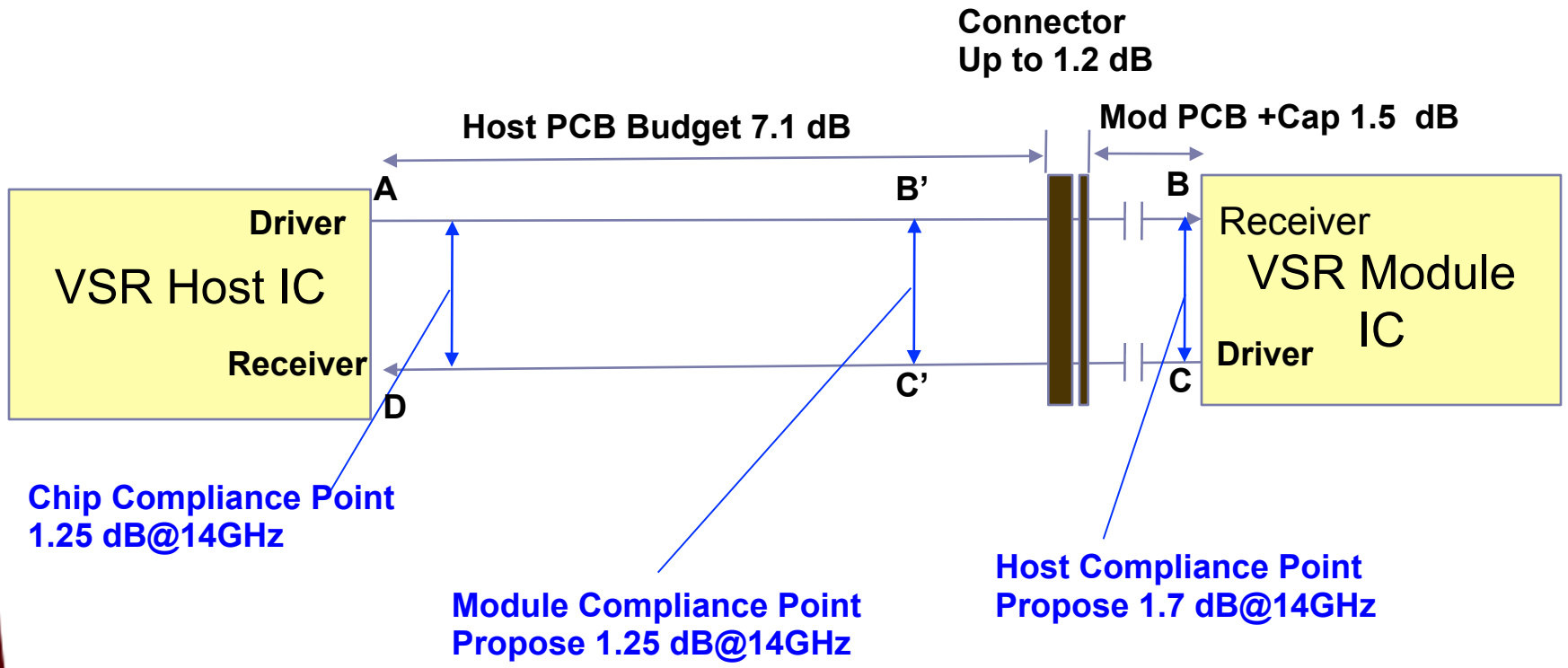
* Assumes connector loss is 1.2 dB and HCB loss is 1.7 dB.

# Highlight of OIF 28G-VSR

- Host transmitter assumes 3 tap FFE with pre and post
- Transmit amplitude of 600 mV
- Host output measured at HCB output with reference CTLE and must meet certain vertical and horizontal opening
- Module transmitter assumes it will deliver certain vertical and horizontal opening at MCB output
- Assume sensitivity at chip ball is 100 mV when measured with software CTLE
- There is no back channel
  - Host will optimize far end eye through reference CTLE by adjusting pre and post
  - The module will utilize its pre/post or peaking filter and faster rise time to deliver min vertical and horizontal opening at TP4 (MCB Output)
- Specification assumes MCB and HCB similar to 802.3ba
- Good starting point for CAUI-4 and it can be tweaked to better fit Ethernet applications.

# OIF 28G-VSR Architecture and Reference Points

- Follows 802.3 CL83B (CAUI)



# VSR Channel Loss Budget Table

- Assumes 10 dB loss from host IC balls to module IC balls
- If the CPPI-4 loss budget is in the 12 dB range a level of compatibility with VSR could be achieved
  - With 12 loss budget 9" host PCB is possible on Meg 6

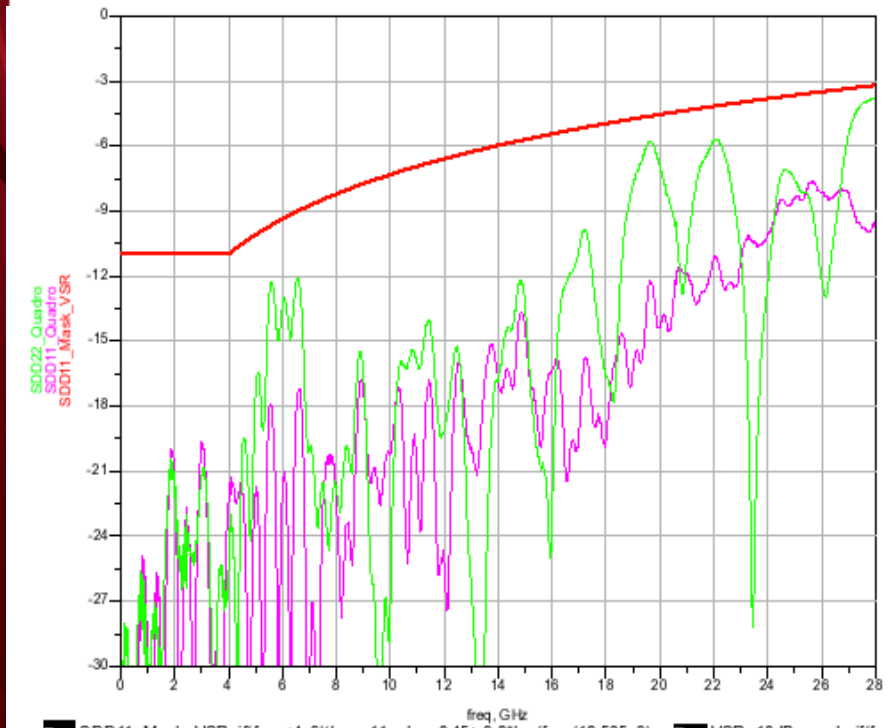
| Traces | FR4-6 | N4000-13 | N4000-13SI | Megtron 6 |
|---|---|---|---|---|
| Loss at 14 GHz /in | 2.0 | 1.5 | 1.2 | 0.9 |
| Worst Case Connector loss at 14 GHz | 1.2 | | | |
| Loss allocation for 2 Vias in the channel | 0.5 | | | |
| DC Block | 0.5 | | | |
| Max Module PCB Loss | 1.7 | | | |
| Host PCB Trace Length Assuming 10 dB Loss Budget | 3.0500 | 4.0667 | 5.0833 | 6.7778 |
| Host PCB Trace Length Assuming 12 dB Loss Budget | 4.0500 | 5.4000 | 6.7500 | 9.0000 |

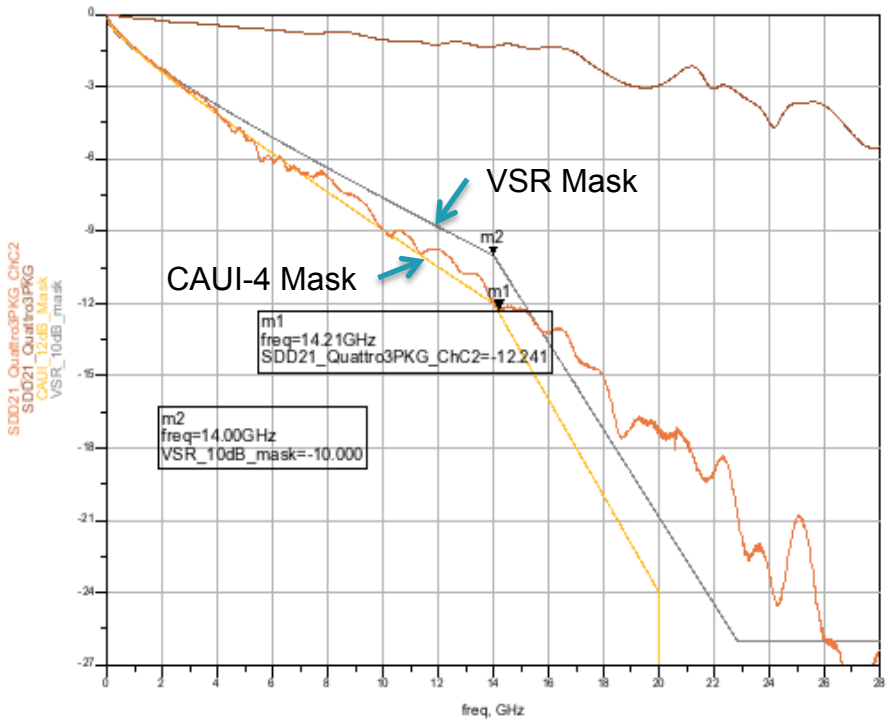
# How To Increase OIF VSR Loss Budget

- **Transmitter TP1a (Host Output)**
  - Transmit output is measured with 0-8 dB CTLE requiring 100 mV post EQ eye height
  - Minimum transmit amplitude is 600 mV
  - Increasing transmit amplitude, reducing jitter, or reducing rise time can deliver the same eye opening across 12 dB channel
  - Further increase would require adding more equalization to the module or possibly increasing sensitivity from 100 mV to 75 mV which will result incompatible interface
- **Receive TP4a (Module Output)**
  - Current OIF test method only require near end testing with small value of CTLE gain 1 or 2 dB
  - There is trivial option to extend the VSR reach assuming just compliant module
  - The most straight forward way would be design the host PCB based on the capability of the receiver, since this is done at design phase it will be interoperable with all VSR modules

# Target CAUI-4 Channel

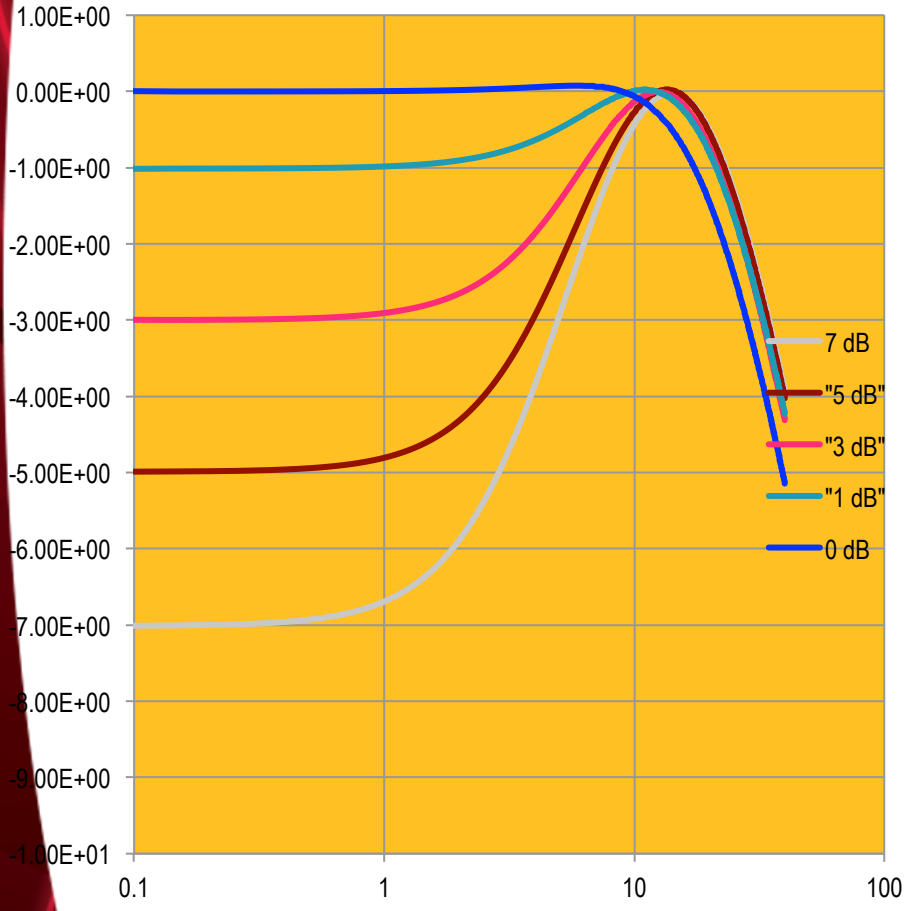
- **VSR loss can be extended for CAUI-4 to 12 dB and have a level of compatibility**
  - Channel was based on measured 5” of FR4 370-HR stripline, with two vias, Quattro connector, and HCB
  - VSR RL mask shown on the left diagram does not include host IC where the VSR mask include the host IC

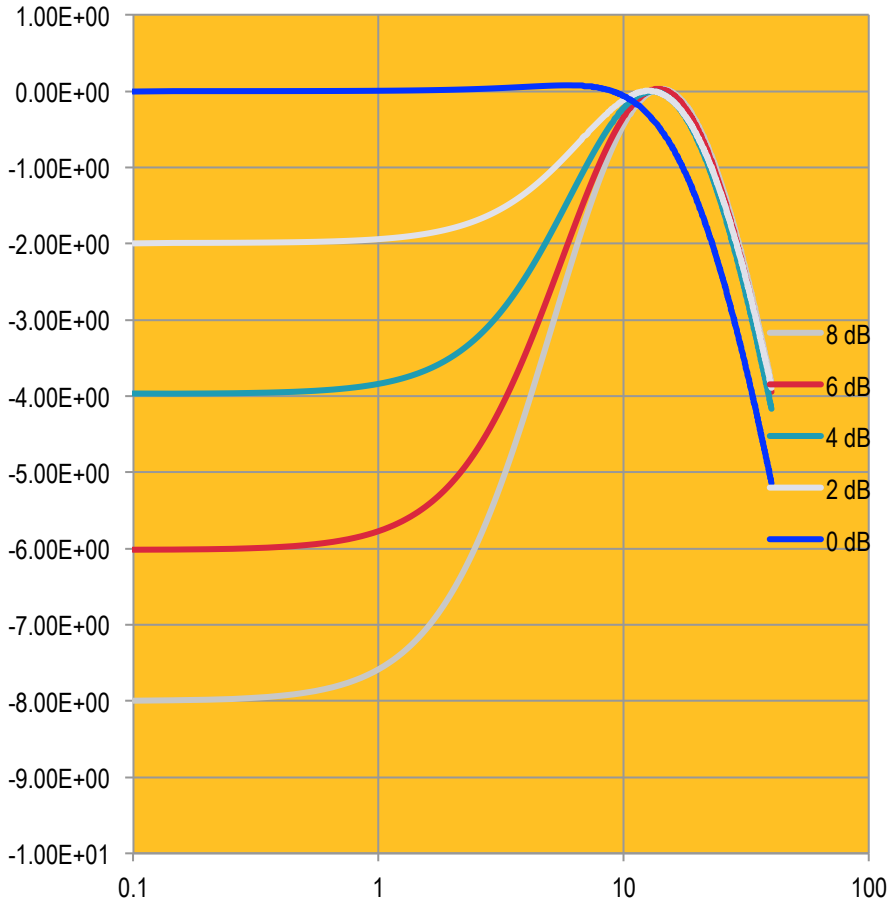


# OIF VSR Reference Receiver

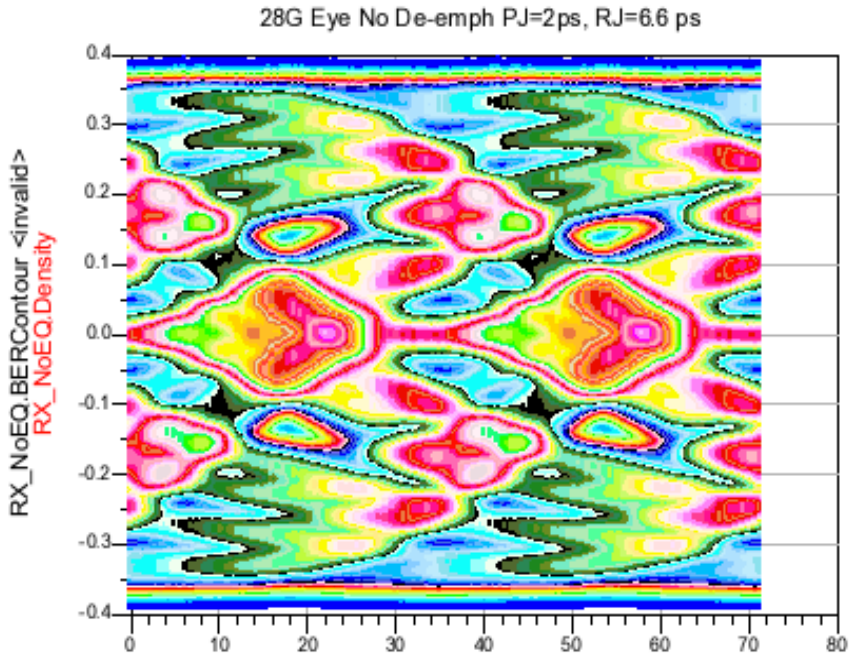
- **Is based on a family of 0-8 dB CTLE having two poles and one zero**
  - Will also submit the same model to be posted under model/channel area



# Far End Eye 12 dB CAUI-4 Channel

- **Just increasing TX amplitude to 800 mV with standard VSR near end jitter would fail the far end**
  - Far end equalized eye measured with OIF VSR CTLE

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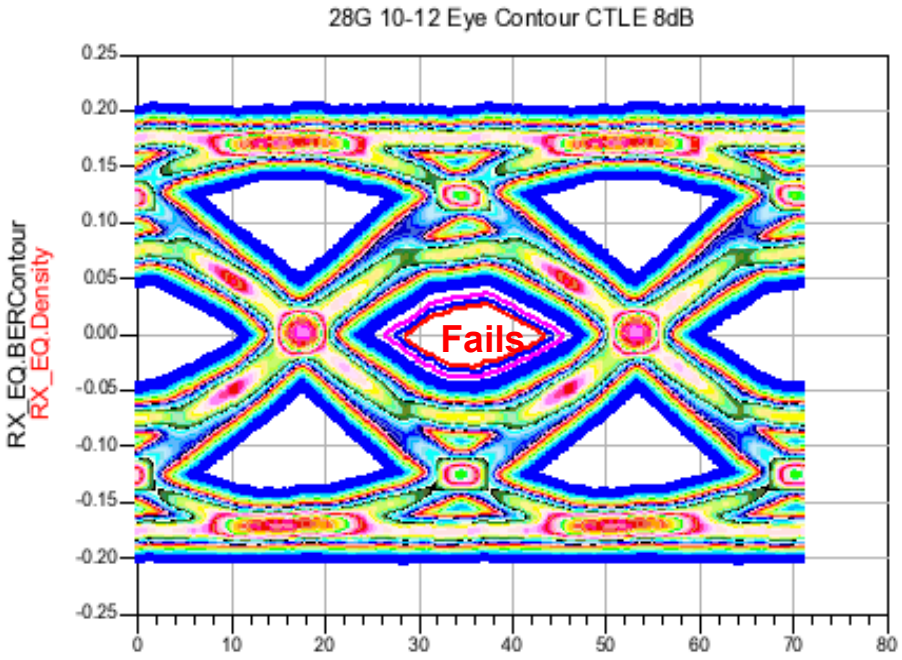


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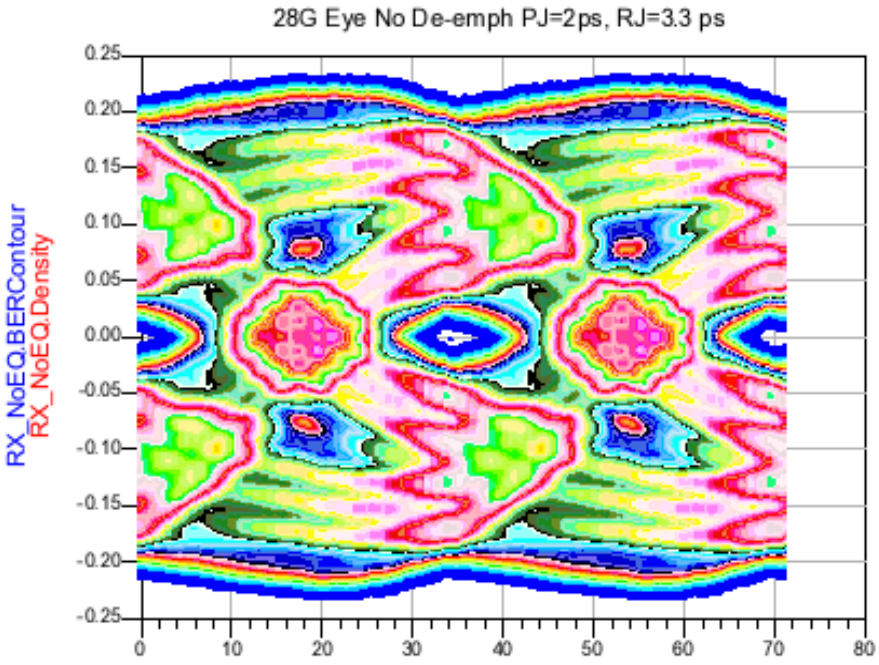
|---|---|---|
| 0.000 | 1.518E-11 | 0.055 |

# Far End Eye 12 dB CAUI-4 Channel

- **Using 2nd gen transmitter similar to cPPI with 600 mV**
  - Alternatively a combination better transmitter and amplitude can be used
  - Far end equalized measured with OIF VSR CTLE

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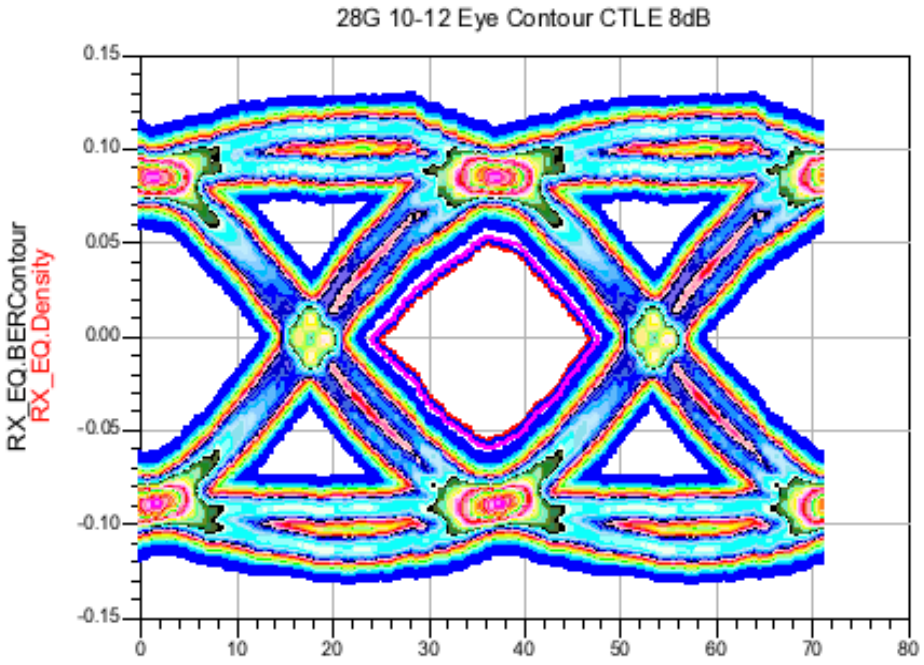


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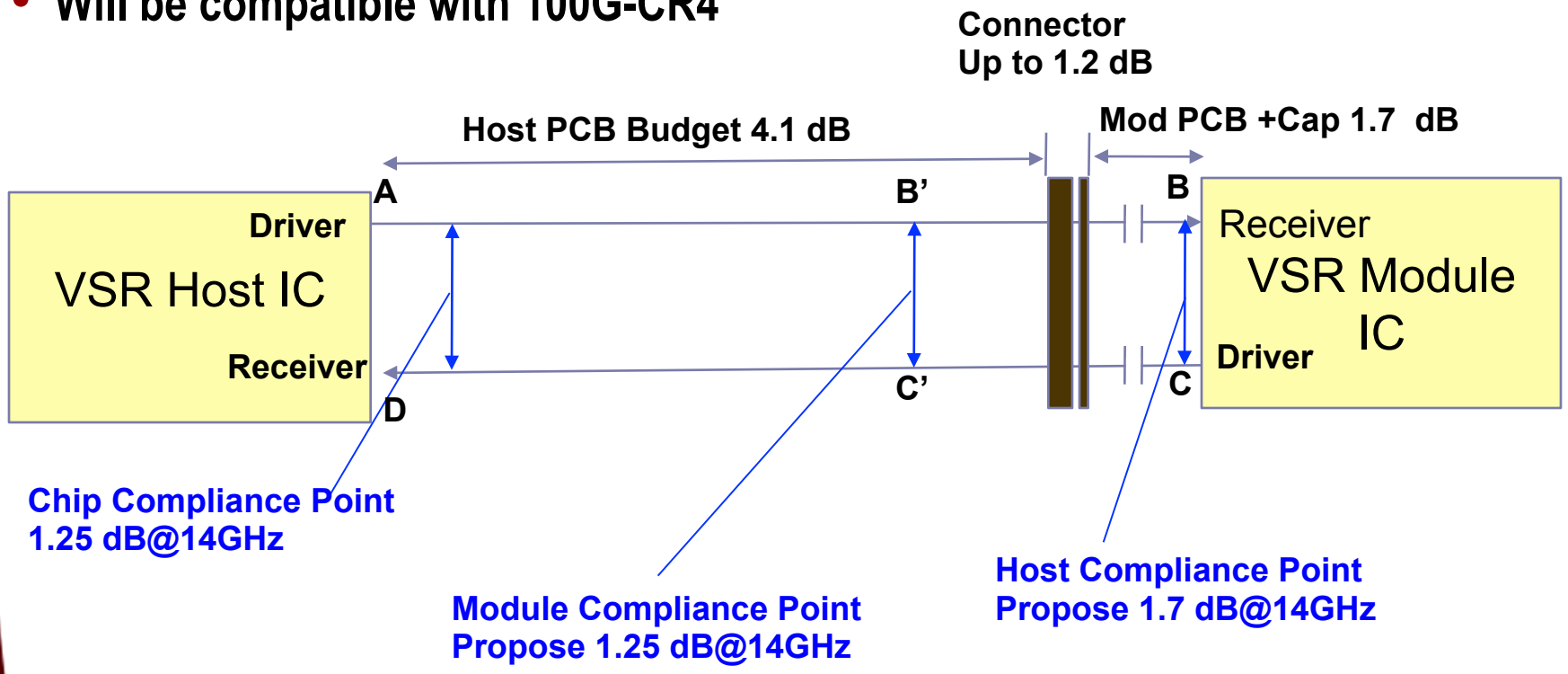
# cPPI-4 Architecture and Reference Points

- Follows 802.3 CL86(nPPI) and CL85
- Will be compatible with 100G-CR4



# cPPI-4 Proposed Channel Loss Budget

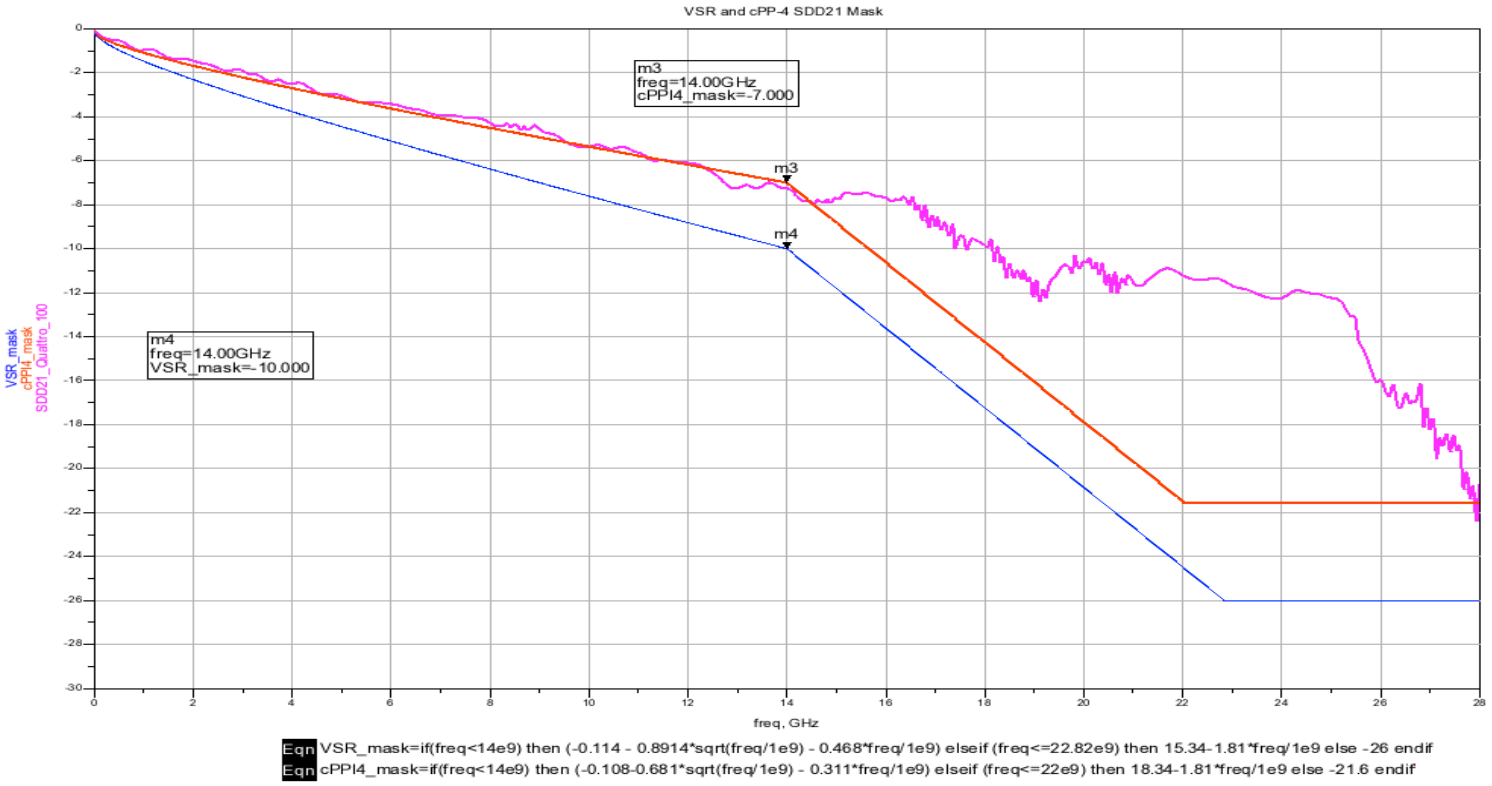
- Attach cPPI-4 with 7 dB loss budget can support unretimed optical PMDs as well as100GCU copper cables

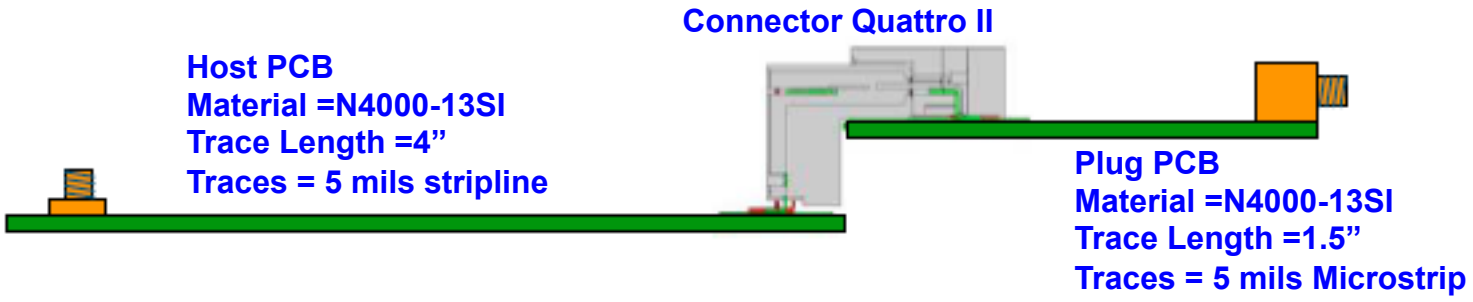
| Traces | FR4-6 | N4000-13 | N4000-13SI | Megtron 6 |
|---|---|---|---|---|
| Nominal Loss at 14 GHz /in | 2 | 1.5 | 1.2 | 0.9 |
| Connector loss at 14 GHz* | 1.2 | | | |
| Loss allocation for 2 Vias in the channel | 0.5 | | | |
| Max Module PCB Loss/DC Blocks at 14GHz* | 1.7 | | | |
| PCB Trace Length Assuming 7 dB Loss Budget | 1.8000 | 2.4000 | 3.0000 | 4.0000 |

* For 100 GbE operation since the HCB and connector are specified for operation up to 28GBd there will be 0.2-0.3 dB unallocated margin.

# cPPI-4 Channel Based on TE Quattro II

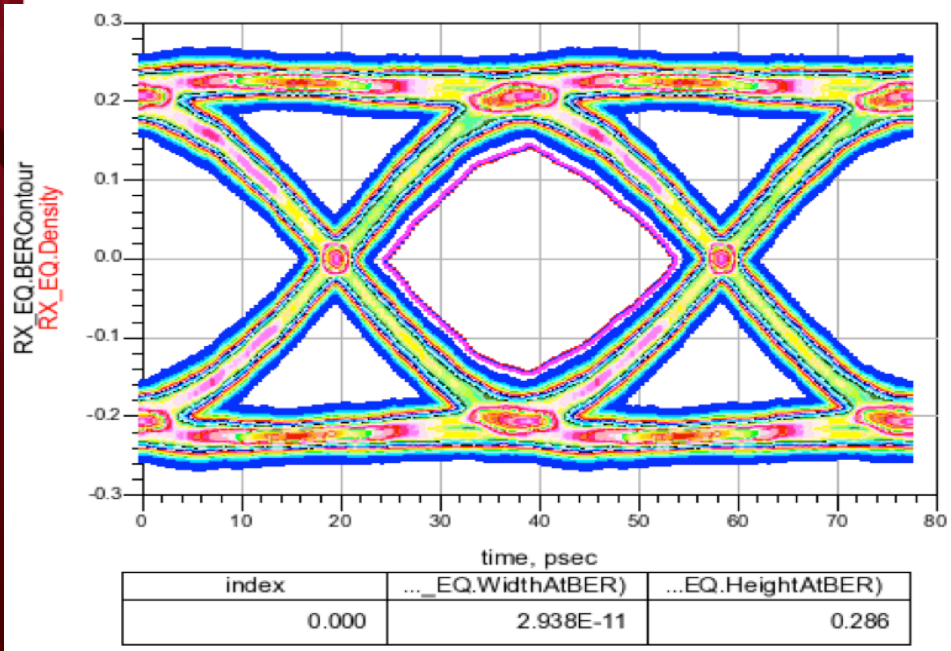
- VSR mask also shown



# Far End Transmitter Eye

- **Simulated and measured eye for 4” Quattro II Channel at 25.7 GBd**
  - Channel loss 7.1 dB @14 GHz

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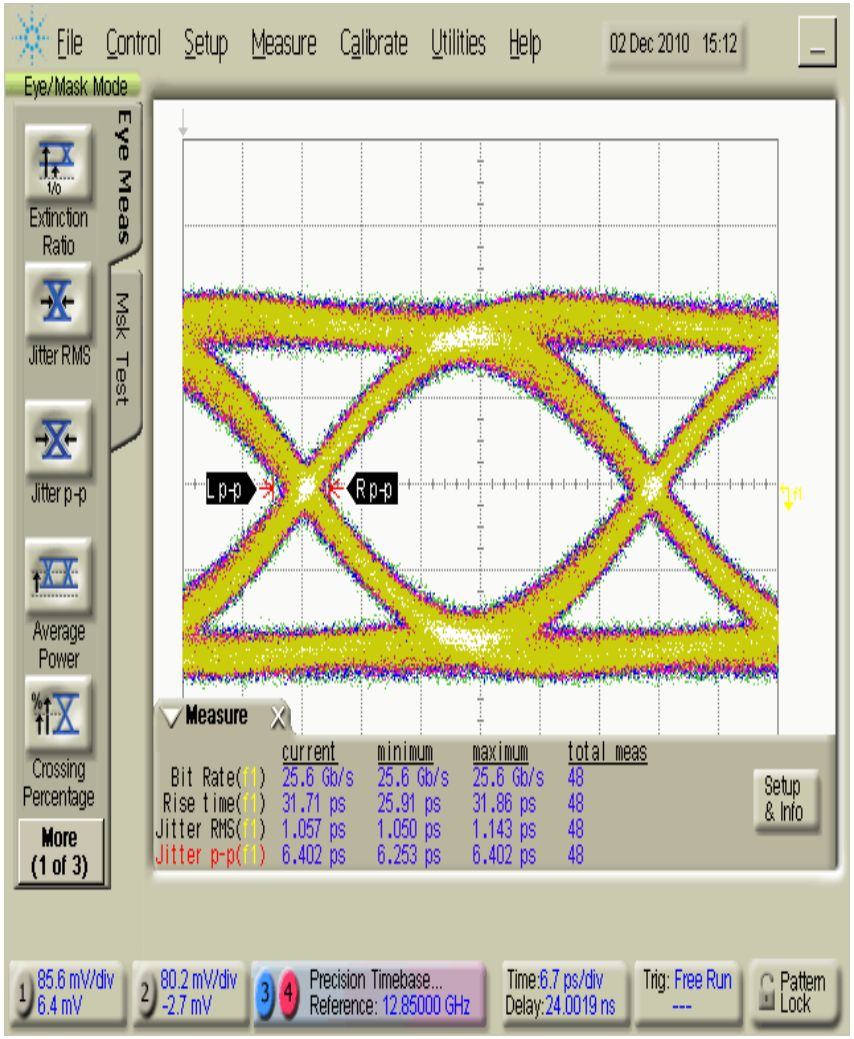
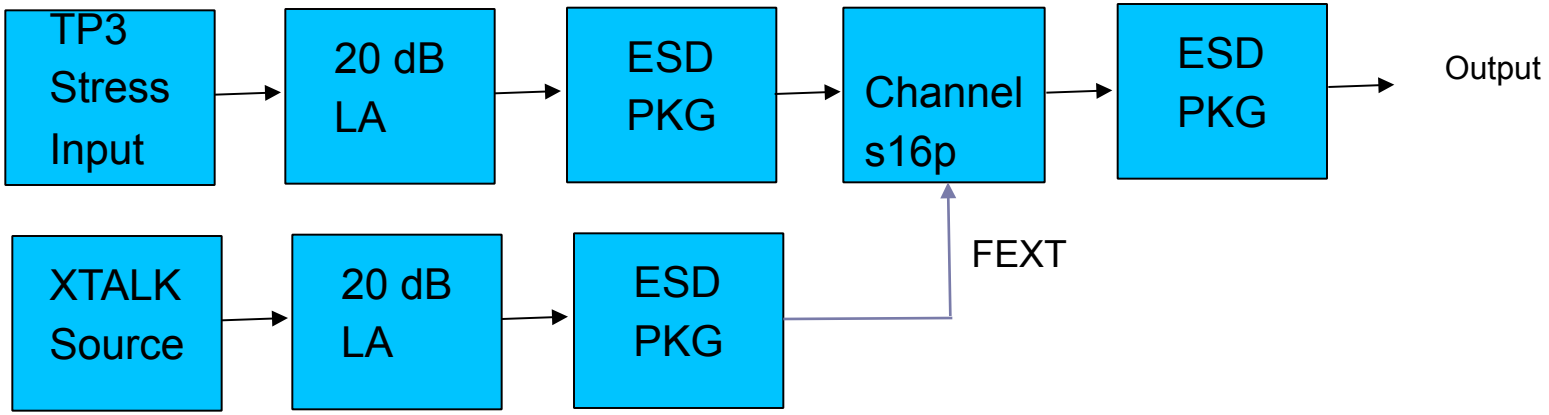


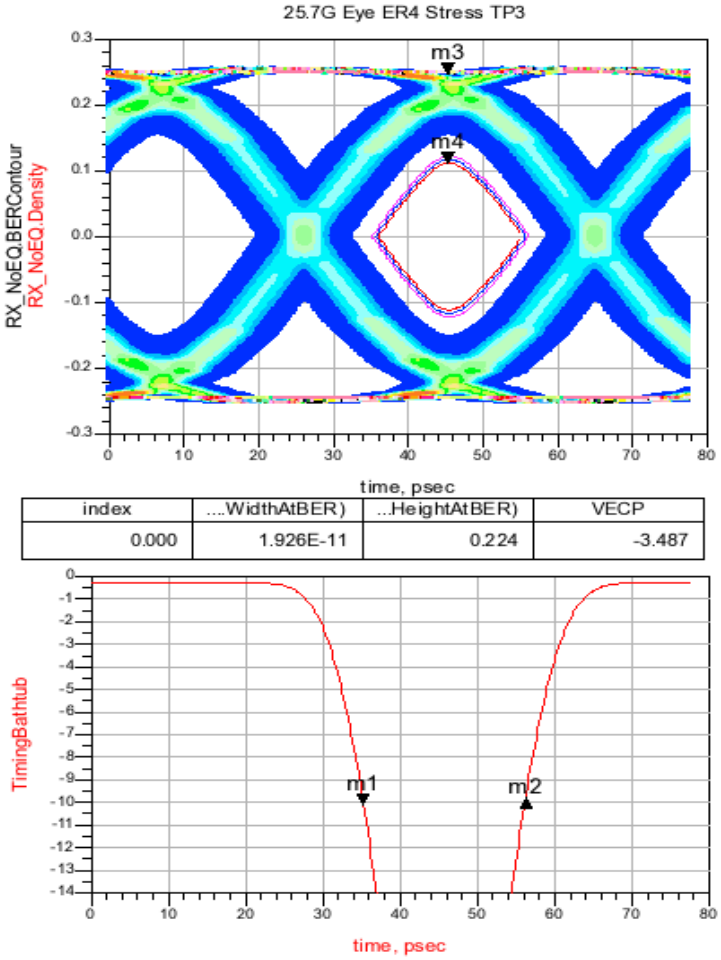
# Simulation Block Diagram Host Module to Host

- **Channel based on s16p and includes worst case FEXT in the simulation**
- **100Gbase-ER4 TP3 stress input with 3.5 dB VECP**
  - VECP for 1310 nm FR4 PMD expected to be 1.5-2.5 dB
  - VECP for 850 nm SR4 PMD could be 3.5 dB
- **TP5 sensitivity with minimum optical receiver sensitivity 0.7 UI TJ at slicer and one with 0.65 UI at slicer**
  - A linear interface will relax the requirement of 0.7/0.65 UI jitter at 25G



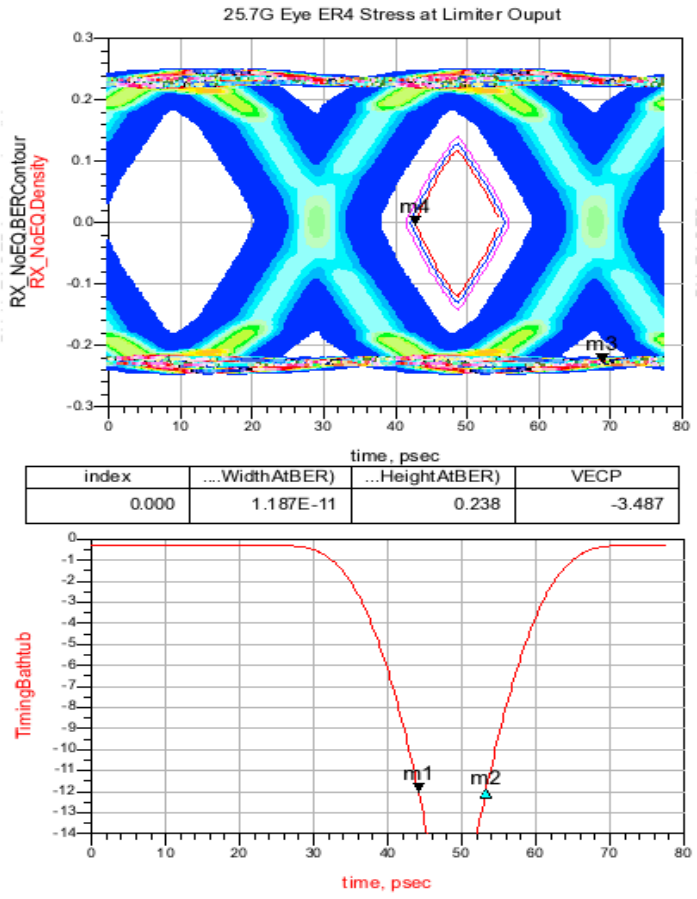
# TP3 Stress Input

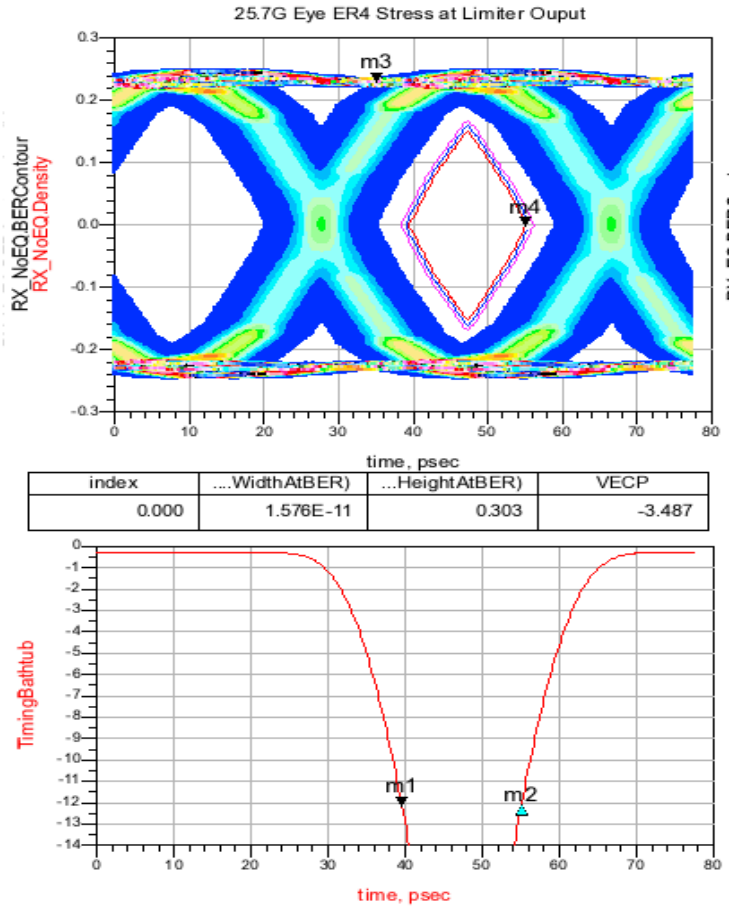
- **Based on 100Gbase-ER4 definition which has higher 3.5 dB VECP, J2=0.3 UI, J9=0.47 UI**



# Limiter Output

- For minimum required sensitivity and slightly better receiver with 0.4 UI opening at sampling point instead of 0.3 UI

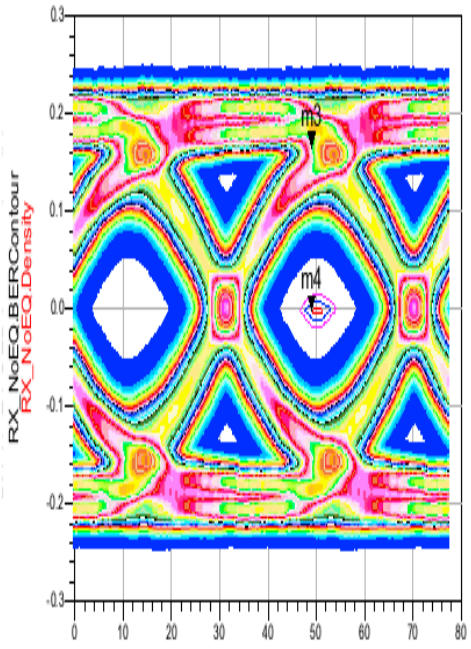


# 75 mm cPPI Like Channel

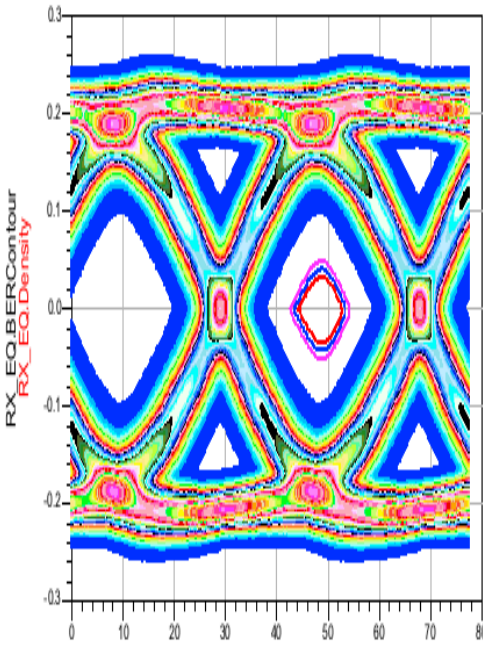
- **Results at TP5 with 0.3 and 0.4 UI at sampling point**
  - Increasing sampling point by 0.1 dB equates to ~2 dB sensitivity increase

25.7G Eye ER4 at TP5




| index | ...WidthAtBER) | ...HeightAtBER) | VECP |
|---|---|---|---|
| 0.000 | 2.335E-12 | 0.004 | -3.487 |

25.7G 10-12 Eye Contour 2 Tap FFE+1 Tap DFE

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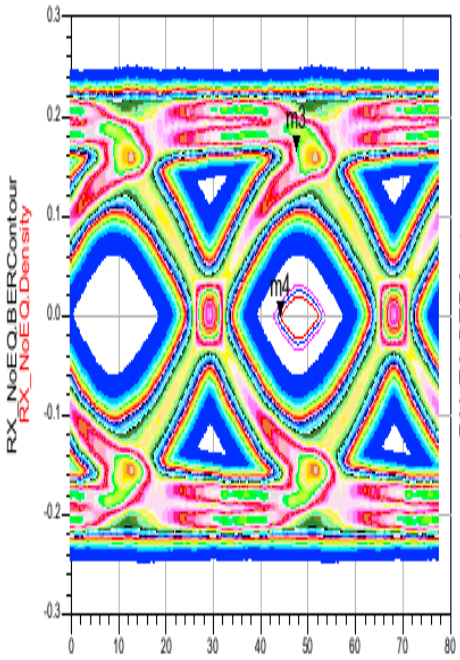
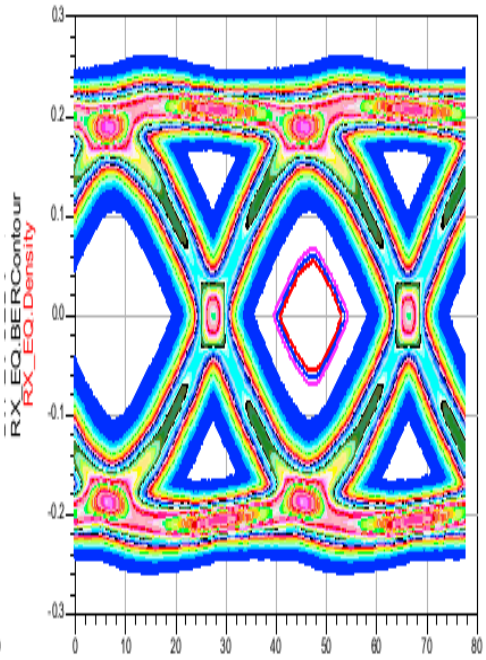
| 0.000 | 8.949E-12 | 0.067 |

25.7G Eye ER4 at TP5




| index | ...WidthAtBER) | ...HeightAtBER) | VECP |
|---|---|---|---|
| 0.000 | 8.171E-12 | 0.041 | -3.487 |

25.7G 10-12 Eye Contour 2 Tap FFE+1 Tap DFE

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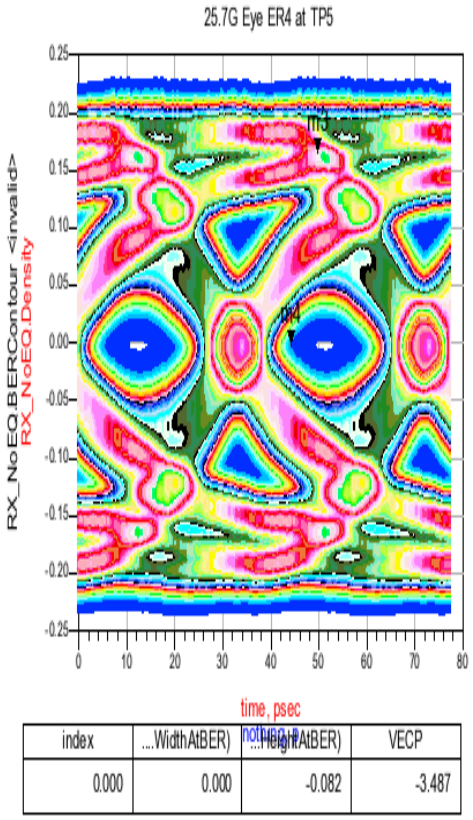
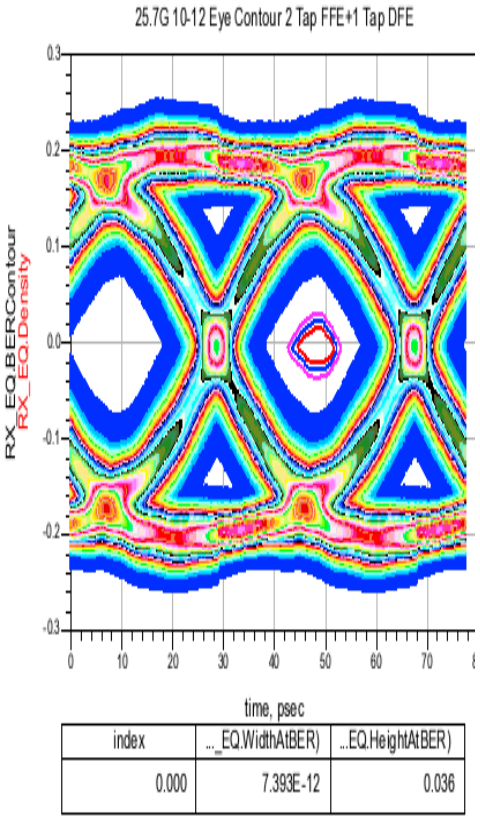
|---|---|---|
| 0.000 | 1.265E-11 | 0.109 |

# 175 mm Channel Unretimed

- 175 mm channel with 0.3 and 0.4 UI at sampling point




| index | ...WidthAtBER) | ...HeightAtBER) | VECP |
|---|---|---|---|
| 0.000 | 0.000 | -0.082 | -3.487 |

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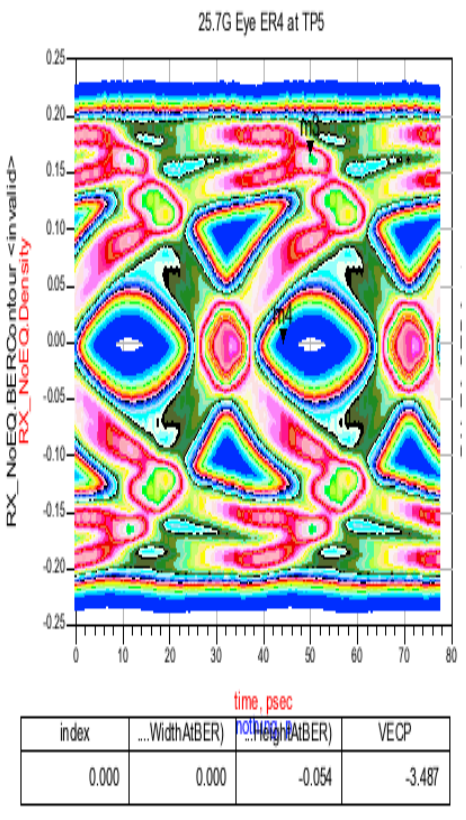
| 0.000 | 7.393E-12 | 0.036 |

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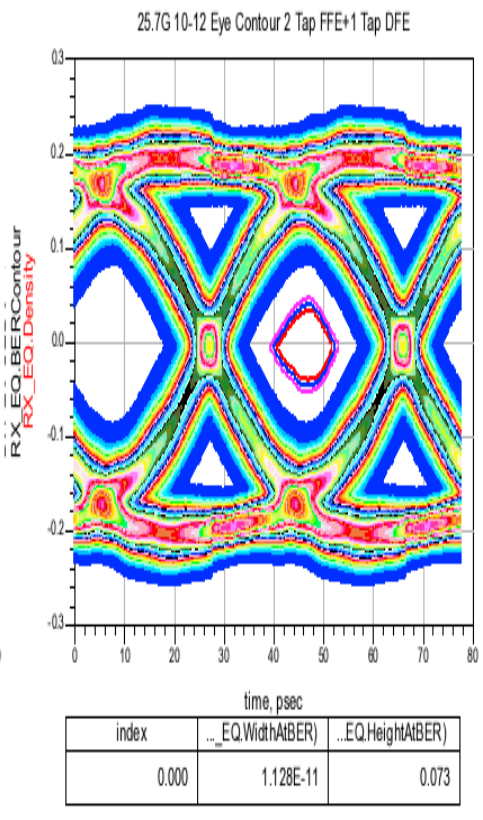
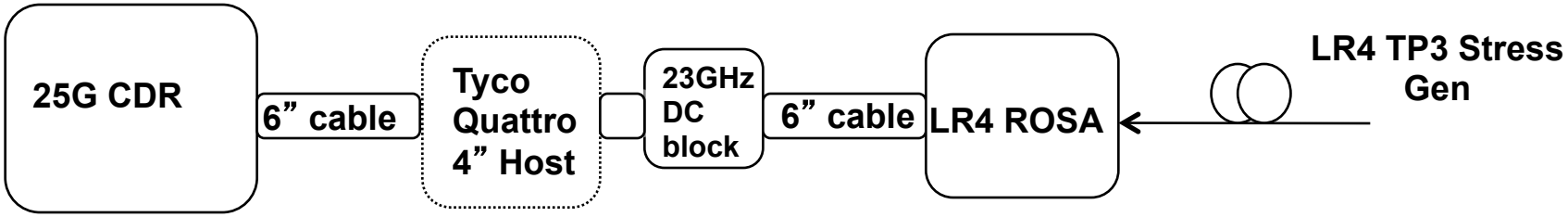
|---|---|---|---|
| 0.000 | 0.000 | -0.054 | -3.487 |




| index | ...EQ.WidthAtBER) | ...EQ.HeightAtBER) |
|---|---|---|
| 0.000 | 1.128E-11 | 0.073 |

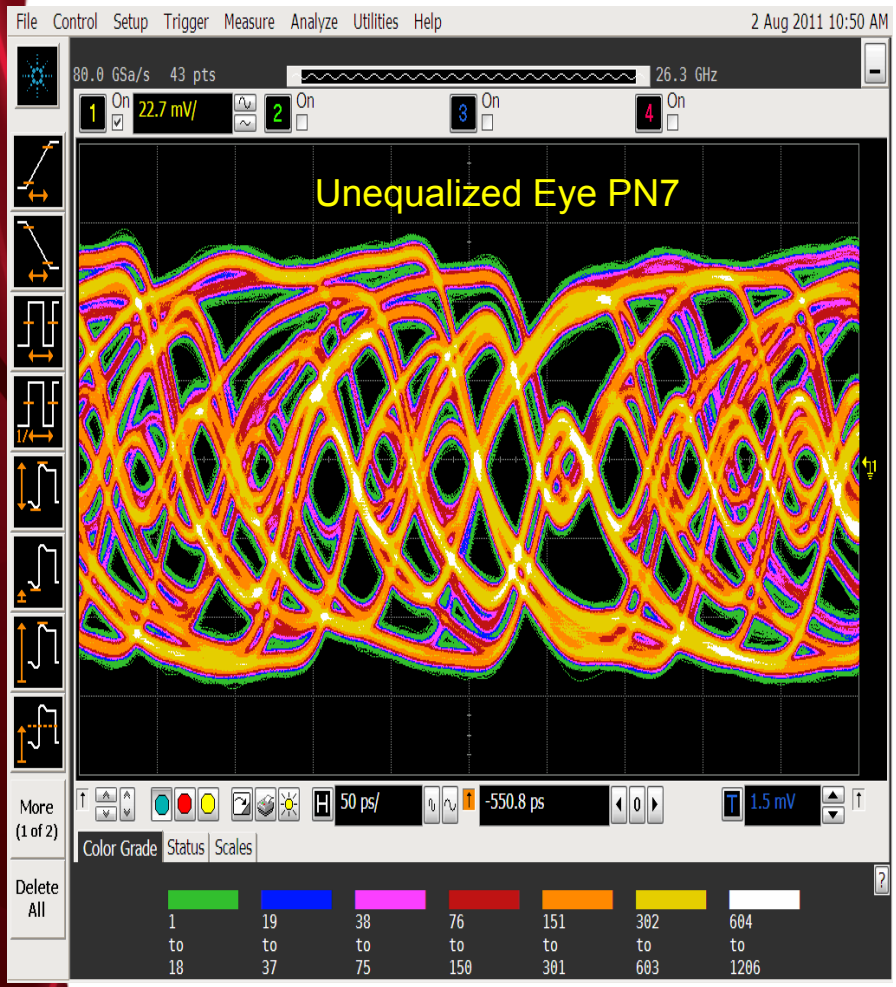
# 100GBase-LR4 Stress Sensitivity Test

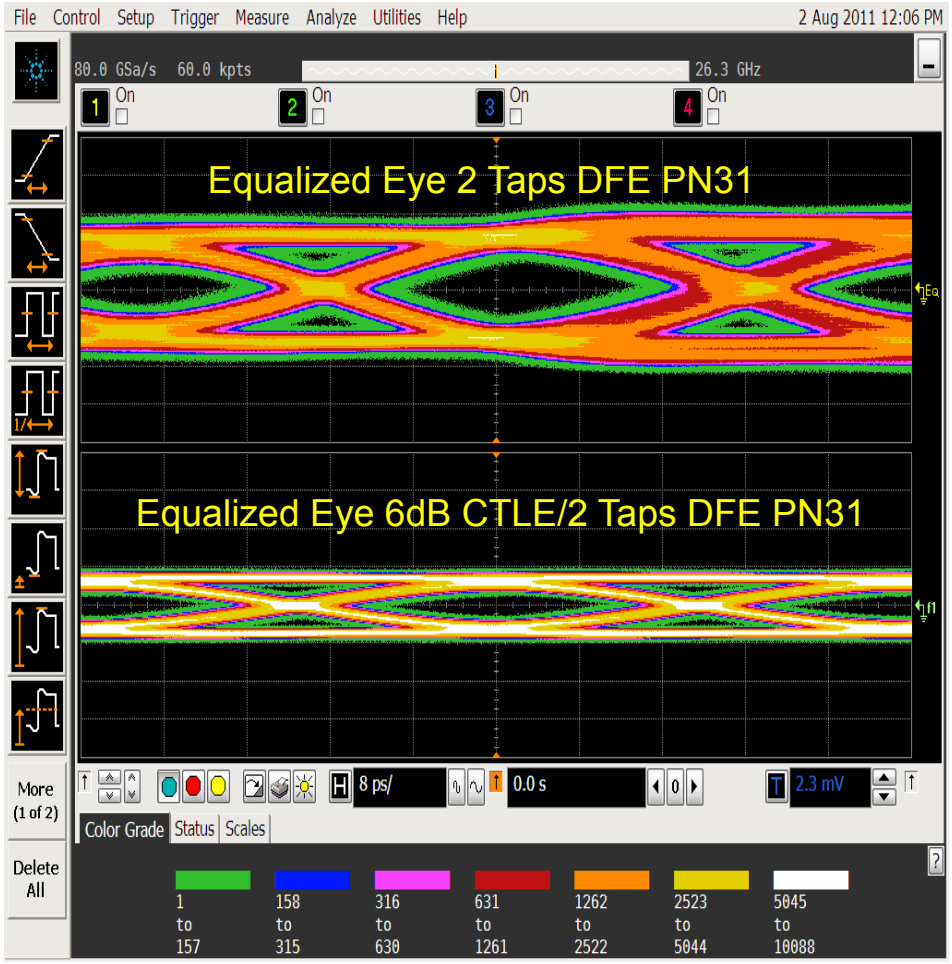
- Tested @25.78GHz
- Tyco HCB + Quattro-II connector + 4 Host" PCB channel (IL 7dB @14G)
- BER tested with PRBS31



# LR4 ROSA Driving 4” TE Channel

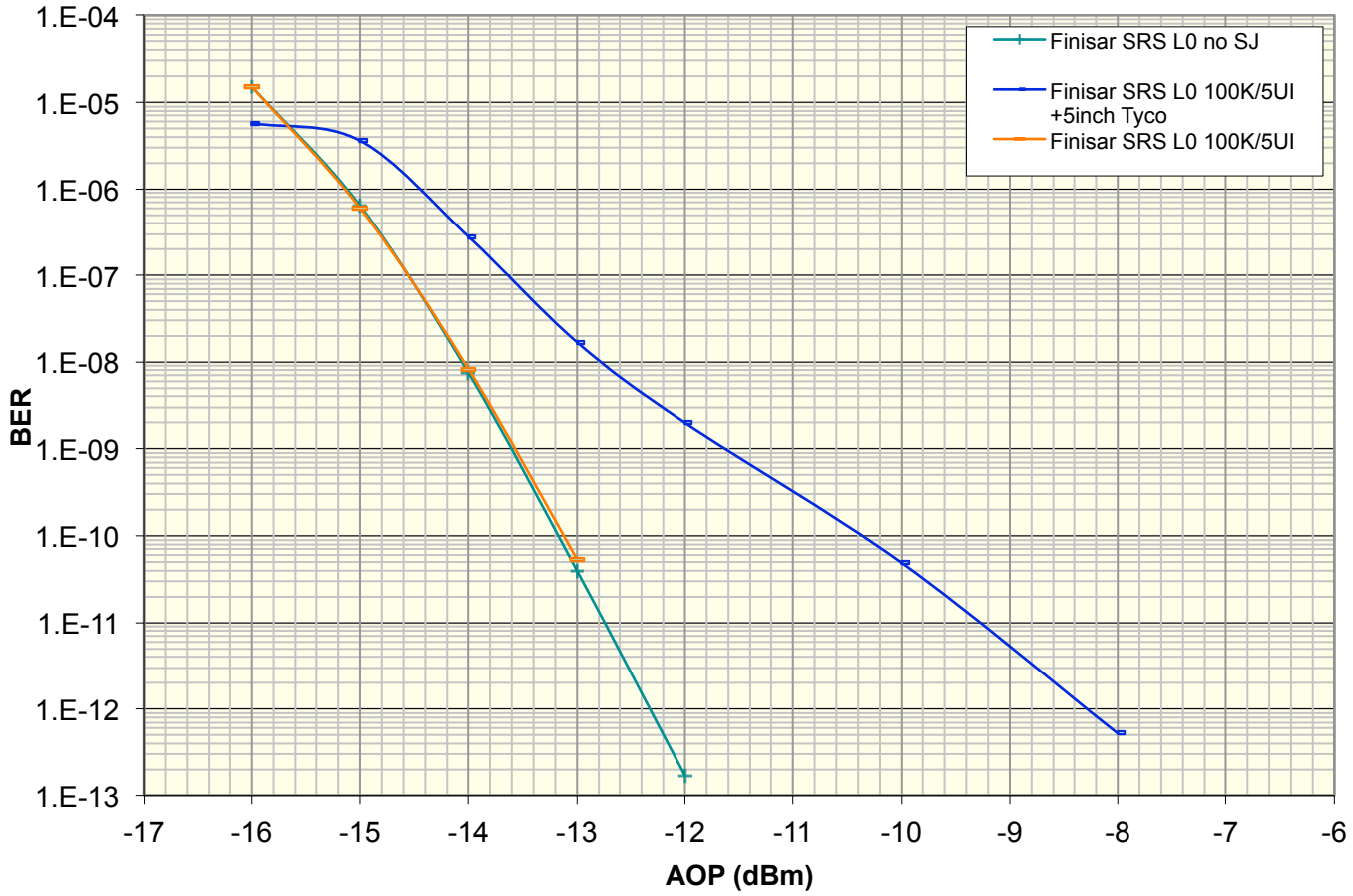
- Real time scope results at -6 dBm AOP



# cPPI-4 BER Measurements

- **Test chip with CTLE shows about 4 dB of optical penalty which is high**
  - Real time scope result with just 2 tap DFE looks promising and expect the penalty could be reduced to more reasonable level like 1-2 dBo



# Summary

- **After investigating line card application space a retime space meeting majority of applications is in line with OIF 28G-SR with loss of 15.4 dB**
  - OIF VSR was specifically created to lower the module PD with agreed loss of 10 dB
  - As identified here OIF VSR loss budget can be increased to 12 dB for CAUI-4 and still maintain a level of compatibility
  - Alternatively we can define a 10 dB and 15.4 dB chip to chip/module interface
- **CAUI-4 must operate with BER 1E-12 or better without FEC as it must support existing PMDs such as LR4/ER4**
  - FEC option must be combine with new PMDs such as 100G-SR4/nR4
- **100GNGTOPTX project needs to define retiemd interface as well as an investigate unretimed interface which is in sync with 100GCU project**
  - In 802.3ba retimed interfaces was defined in CL83A/83B and unretimed interfaces CL85 (CR4/CR10) and CL86 (nPPI) were defined
- **Simulation and measurements shown here indicate feasibility of unretime interface specially in case of new PMDs and with FEC**
  - But we have also shown feasibility of unretime with LR4.