

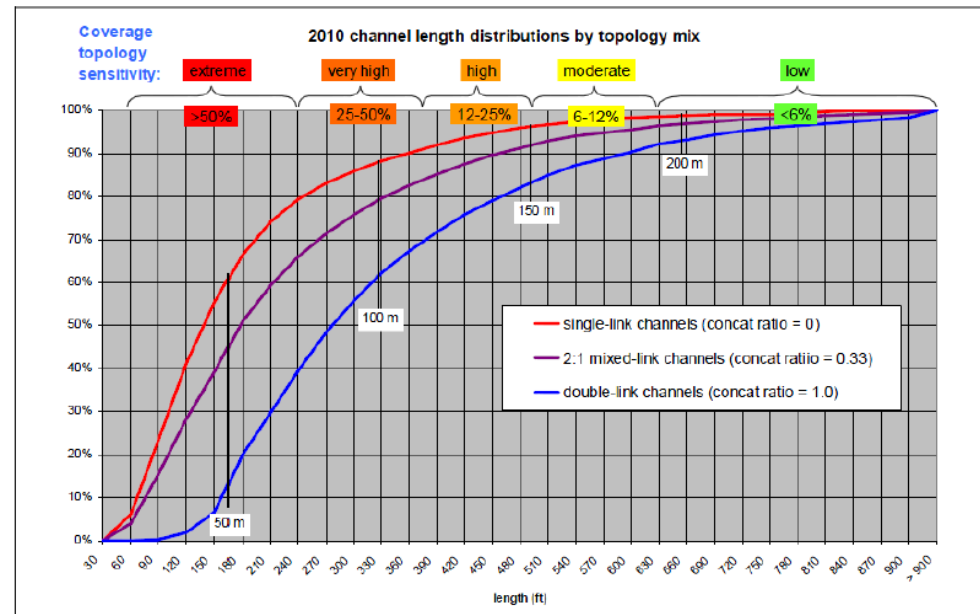


Next Gen 100G Interconnect

Technical Feasibility Using Silicon Photonics

Data Center Needs at 100Gbps

- Low cost transceivers
 - Very low cost at ~150m
 - Low cost at ~2,000m
- Low power consumption
- Small form-factors
 - High front panel density
- Multi-sourcing
 - Multi-vendor interoperable



Coverage topology sensitivity = (single-link coverage - double-link coverage) / single-link coverage

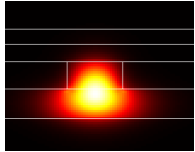
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- IEEE needs to respond with standardization activities that enable:
 - Application of new technologies that can meet cost-performance objectives
 - Existing and new technologies interoperable solutions
 - Support for distances needed in emerging large data centers

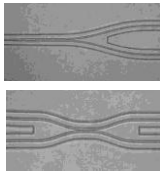
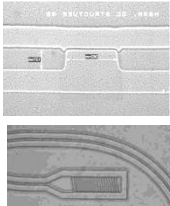
What are the Potential New Technologies

Silicon Photonics – Electro Photonic Integrated Circuit

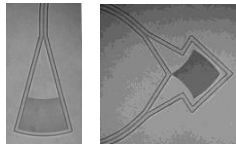
CMOS Photonic Circuits



Waveguides



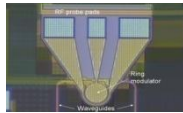
Waveguide Structures



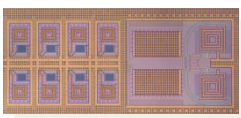
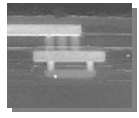
Vertical Couplers



High/Low Speed Modulators

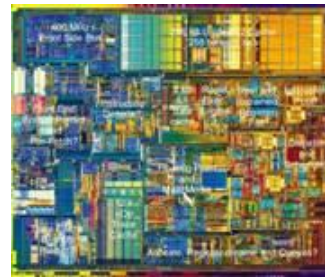


Waveguide Photo-detectors



Integrated PD & TIA/LA

CMOS Analog & Digital Circuits

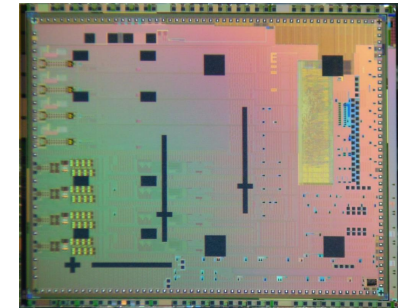


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Integrated CMOS

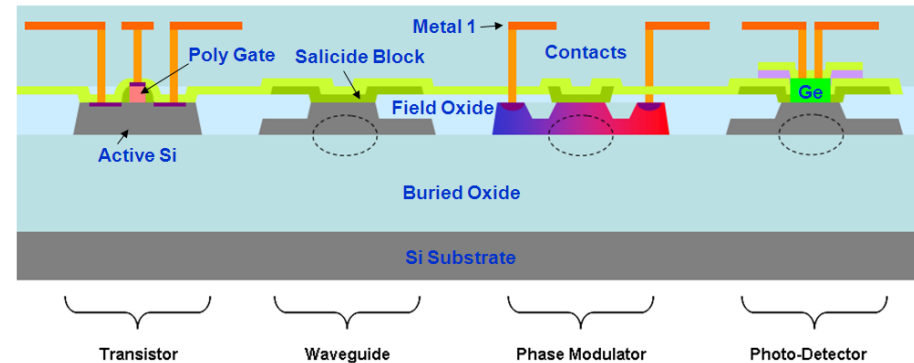
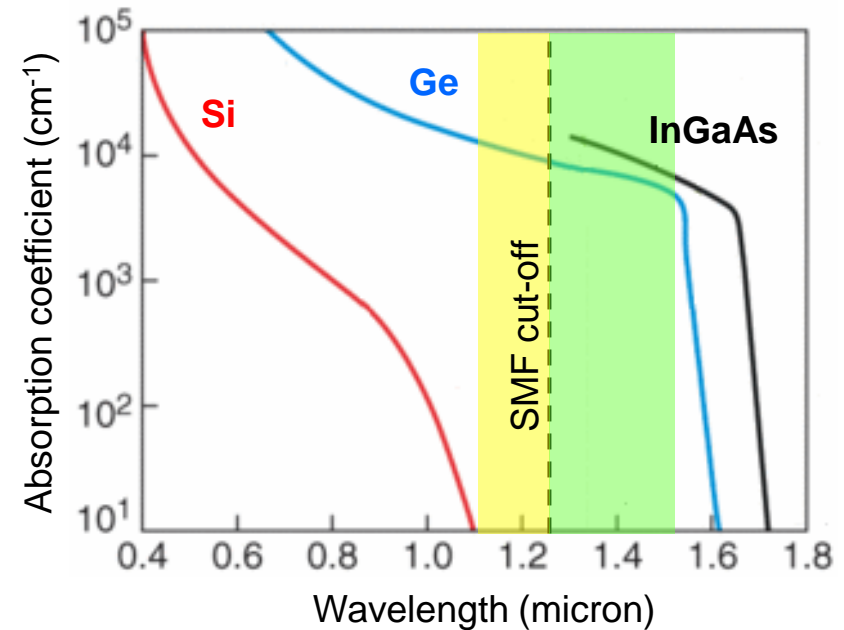
Photonic, Analog & Digital Circuits



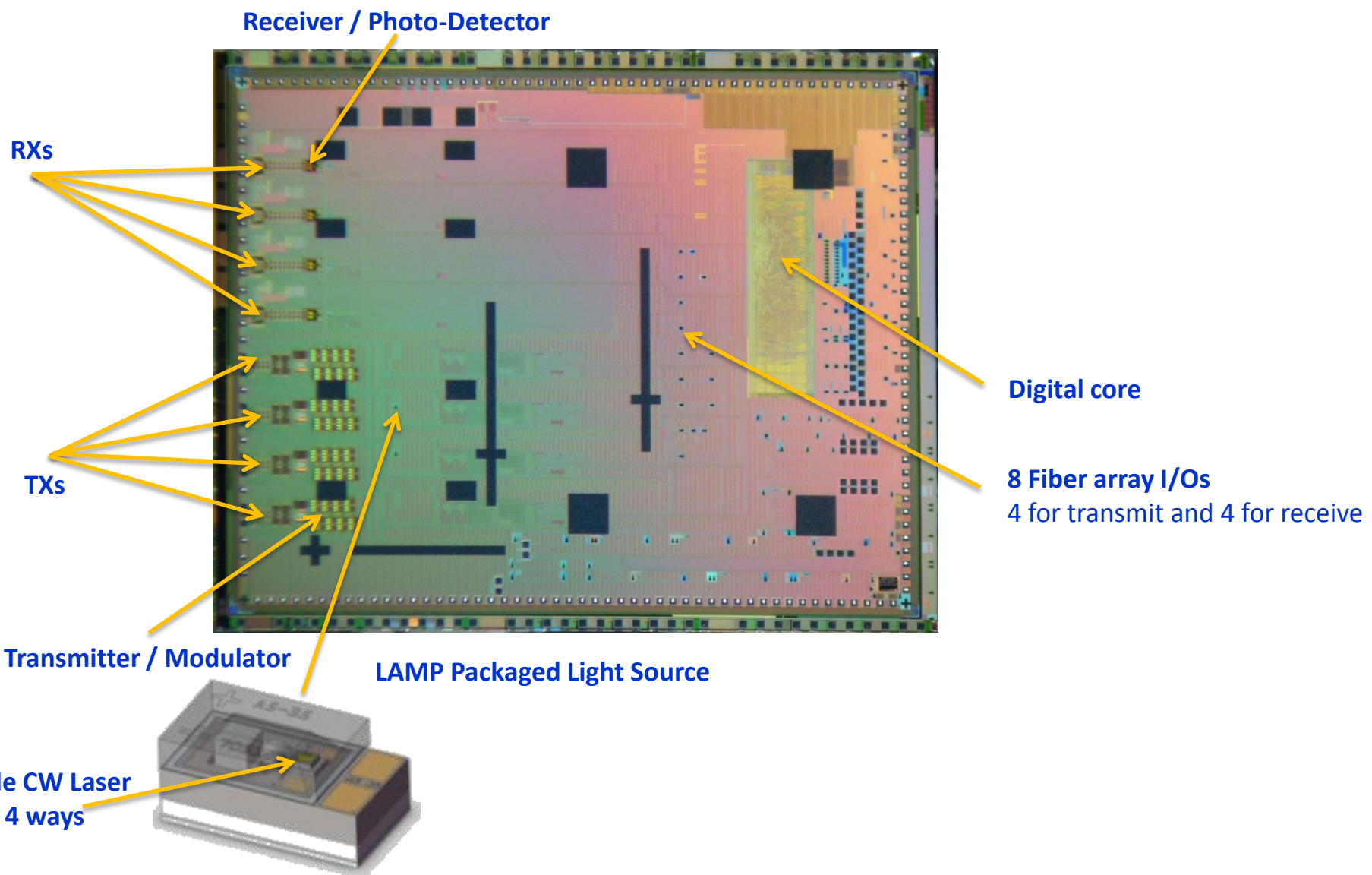
- A number of companies are working on this technology, including:
 - Luxtera, Intel, IBM, Lightwire, Kotura, and other new startups

Key Technical Characteristics of Silicon Photonics

- Silicon is transparent to light at wavelengths longer than 1100nm
 - Need transparency to build a waveguide
- Germanium efficiently absorbs light up to 1560nm
 - Need absorption to build an efficient photo-detector
 - Germanium enables monolithic Photo-detector
- Light from a waveguide couples most efficiently to a single mode fiber
 - Low loss due to small diameter of SMF core
- **RESULT:** to enable a low-cost, low-power and small form factors of silicon photonics the following are needed:
 - Wavelength between 1100nm and 1560nm
 - Single Mode Fiber transmission media



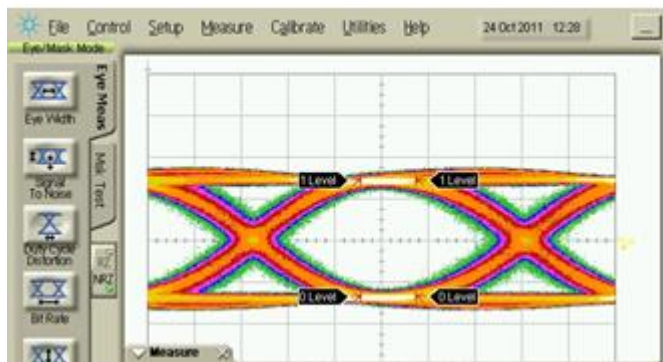
Example of a 4x28Gbps SP Optical Transceiver



Enables Performance Needed at 26G and 28Gbps

Applications: 100GE Ethernet and EDR InfiniBand

26 Gbps Electrical Output Eye with PRBS 31

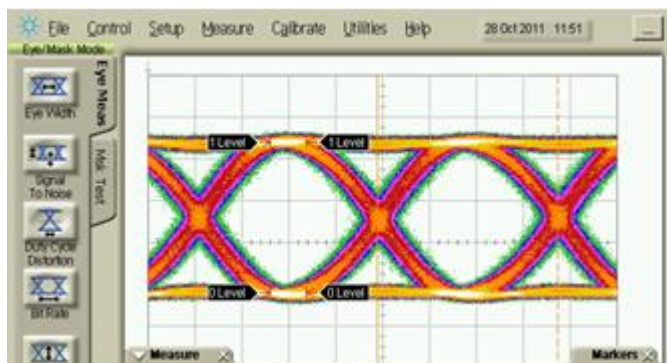


Applications: 28G VSR and 28G Fibre Channel

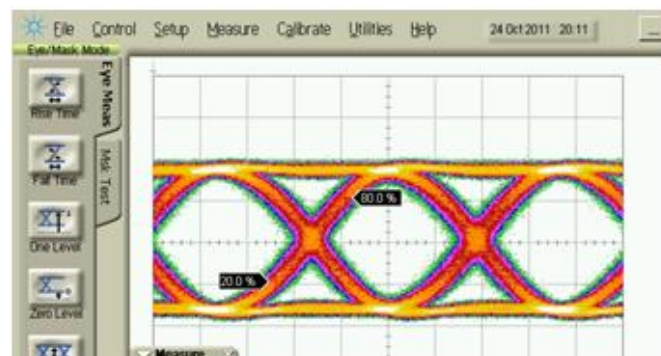
28 Gbps Electrical Output Eye with PRBS 31



26 Gbps Optical Output Eye with PRBS 31

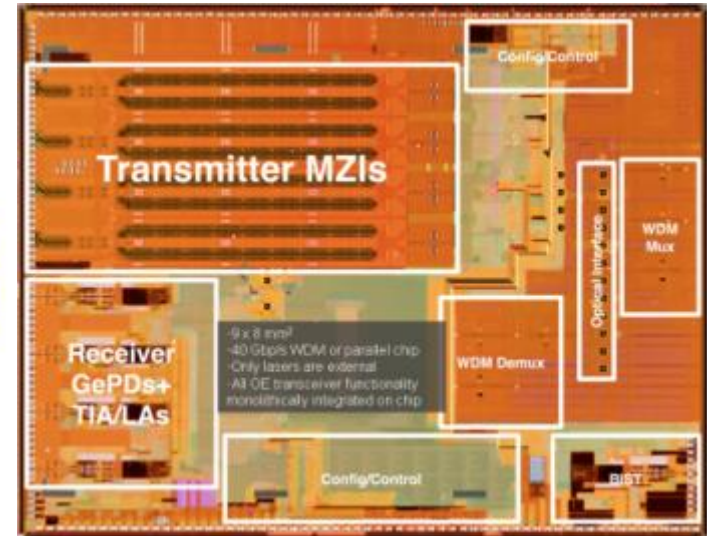
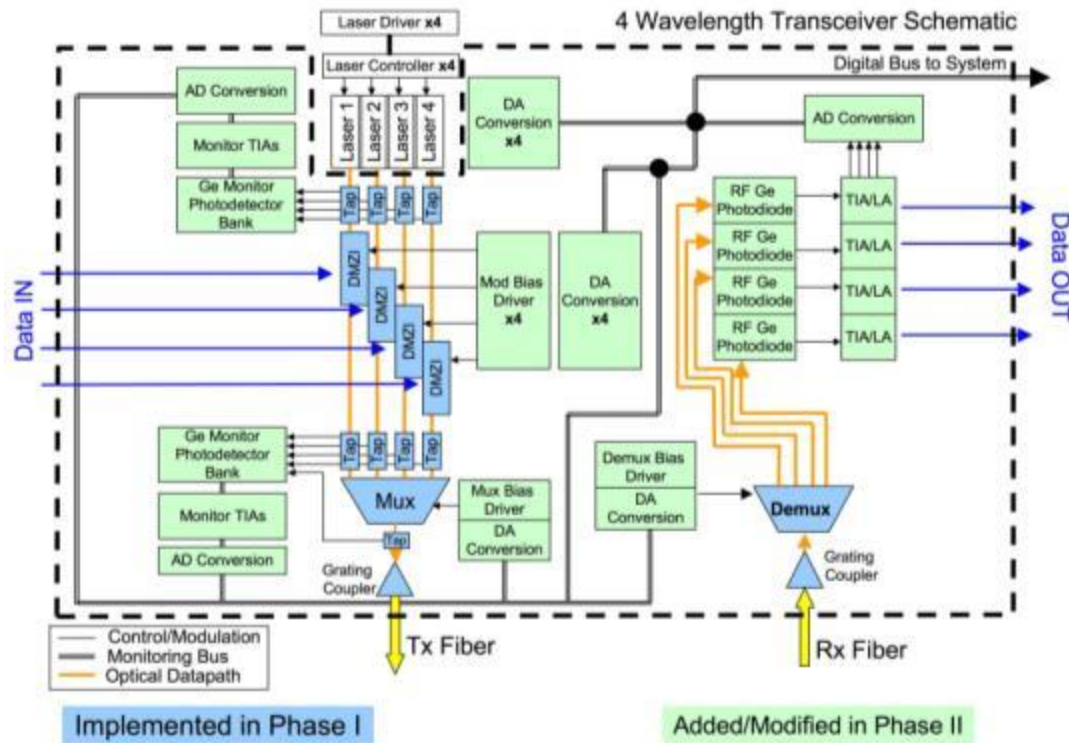


28 Gbps Optical Output Eye with PRBS 31



4 λ WDM SP Demonstrator For DARPA

Within DARPA-EPIC program developed and demonstrated a fully integrated WDM transceiver IC operating error free at 4x10 Gb/s bi-directional traffic (module-to-module).



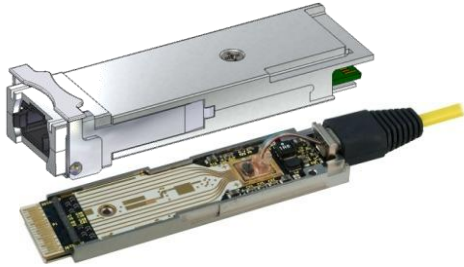
Various WDM MUX/DEMUX structures (AWG, Interleaver, Ring) have been tested and demonstrated on system die:

- Channel spacing = 1.6 nm = 200 GHz
- Combined with control circuitry: phase tuners shift spectral response for:
 - Temperature compensation
 - Process compensation
 - Agile wavelength plan



100G Form-Factor Options

100G QSFP Module with Silicon Photonics



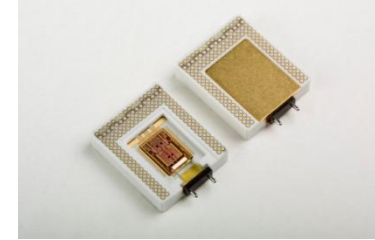
- Dual Retimed Interface
 - One CMOS Chip
- Power per 100G
 - Parallel: < 20 pJ/bit
 - WDM: < 30pJ/bit
- Cost for 100G Transceiver
 - ~25% lower than conventional
- Mechanically backward-compatible

100G Embedded Optics with Silicon Photonics



- Non-retimed interface
 - <2 inch electrical traces
- Power per 100G
 - Parallel: < 7.5 pJ/bit
 - WDM: < 17 pJ/bit
- Cost for 100G Transceiver
 - ~60% lower than conventional
- Optically compatible to modules

100G Silicon Photonics Integration with ASICs

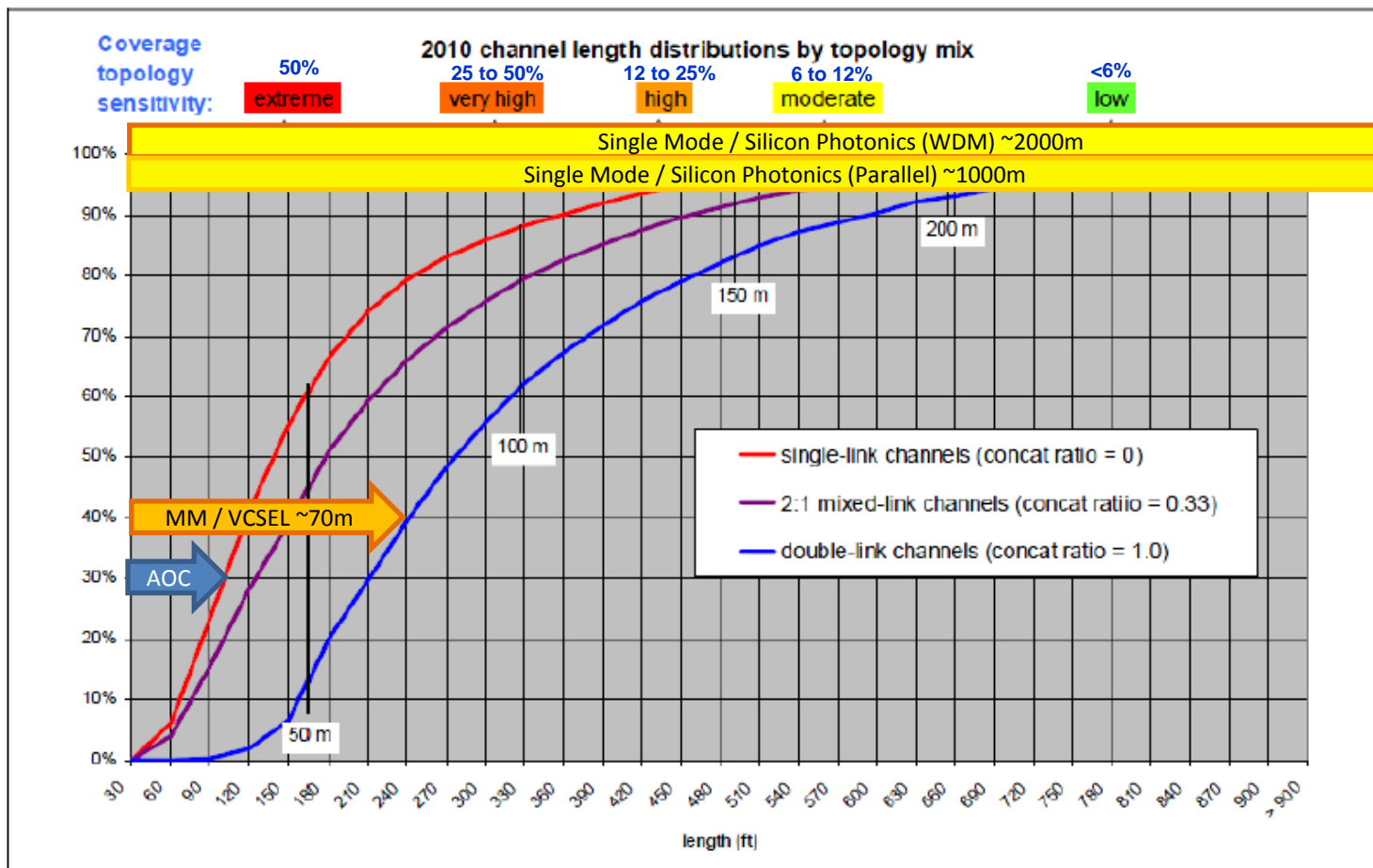


- No chip-to-chip I/O
 - No electrical traces
- Power per 100G
 - Parallel: < 3pJ/bit
 - WDM: < 10pJ/bit
- Cost for 100G Transceiver
 - ~90% lower than conventional
- Optically compatible to modules and embedded optics

All form-factors interoperable at 1310nm over single mode fiber and reaches from 0 to 10KM

Data Center Needs Low Cost, >100m Interconnect

**Multi-Mode VCSEL Serves ~ 50% of Links, Single Mode Silicon Photonics Serves 100% of Links
Two Solutions Provide 100% Data Center Coverage with Low Cost Parallel Transceivers**



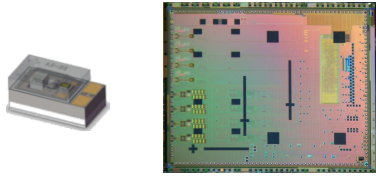
Coverage topology sensitivity = (single-link coverage - double-link coverage) / single-link coverage

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Proposed Solutions for All Reaches

1310nm Parallel Solution

- 1 Laser
- 1 Chip
- Lowest cost at short reach
- Lowest power
- Ideal for short reach



**0 to 30m: Active Optical Cable – Wavelength Agnostic
4x25G QSFP**



Reach limited by deployment practicality of AOC, not by the optical transceiver

**0 to 70m: Parallel Multi-Mode Fiber – 850nm to 1060nm
4x25G QSFP with MPO**



**0 to 1000m: Parallel Single Mode Fiber – 1310nm
4x25G QSFP with MPO** **Embedded Optics with MPO**



Longer Reach Possible



**0 to 2000m: WDM Single Mode Fiber – 1310nm
4x25G QSFP with LC** **Embedded Optics with LC**

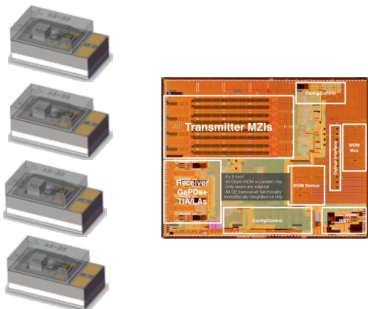


Longer Reach Possible



1310 nm WDM Solution

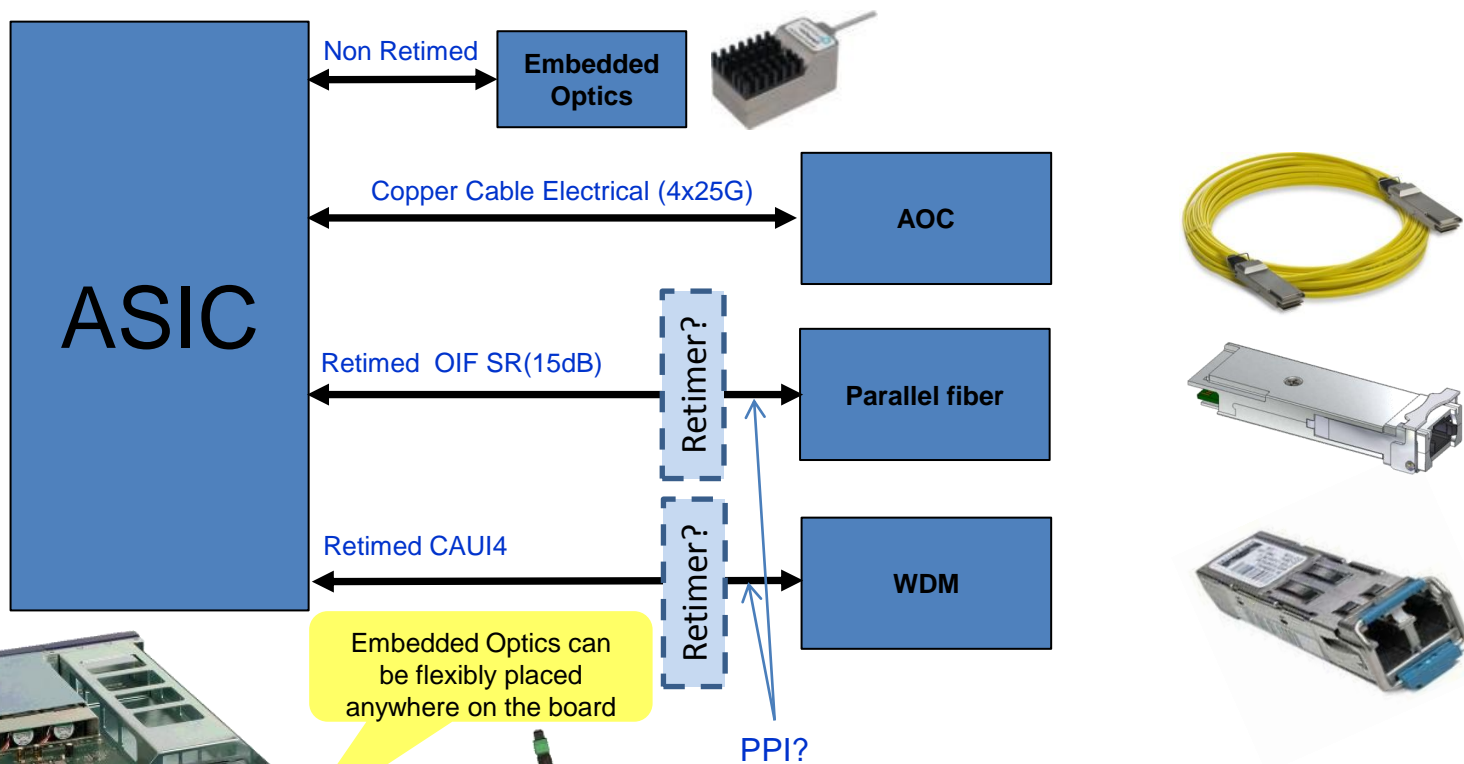
- 4 Lasers
- 1 Chip
- Lowest cost at long reach
- Reuse fiber plant
- Ideal for long reach



**0 to 10,000m: WDM Single Mode Fiber – 1310nm
4x25G QSFP with LC** **Embedded Optics with LC**



Electrical Interfaces



Embedded Optics can be flexibly placed anywhere on the board

Drive electrical 4x25G/4x28G ASIC to Module interface to a common specification where a single ASIC can be serviced by any type of transceiver

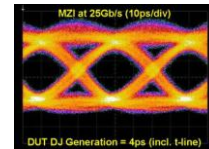
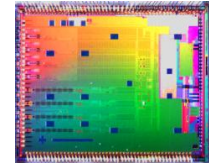
- Retimed module for 10 inch electrical traces
- Non-retimed embedded optics for 4 inch or shorter traces

Front Panel QSFP

Summary

- Silicon Photonics provides technical feasibility for Next Gen 100G interconnects:

- Low cost/power
- Small form-factor
- Meets possible reach objective of 300m for data center
- Meets possible reach objective of 1-2km (10KM possible)
- Demonstrated 25Gbps data rates and WDM
 - Interoperable with traditional EML, hybrid solutions at 1310nm
- Parallel fiber solutions are viable and are in production at 4x10G.



- Multiple Form-Factors supported

- Parallel and WDM QSFP modules or Embedded Optics
 - *End users will have flexibility to select the most optimal solution for their application*
 - *Cost / power consumption / ease of deployment trade-offs*
 - *common electrical interface to ASICs and a common mechanical form-factor (QSFP)*

