100G-SR4 Link Modeling

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Next Generation Optics Study Group

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Objective & Methodology

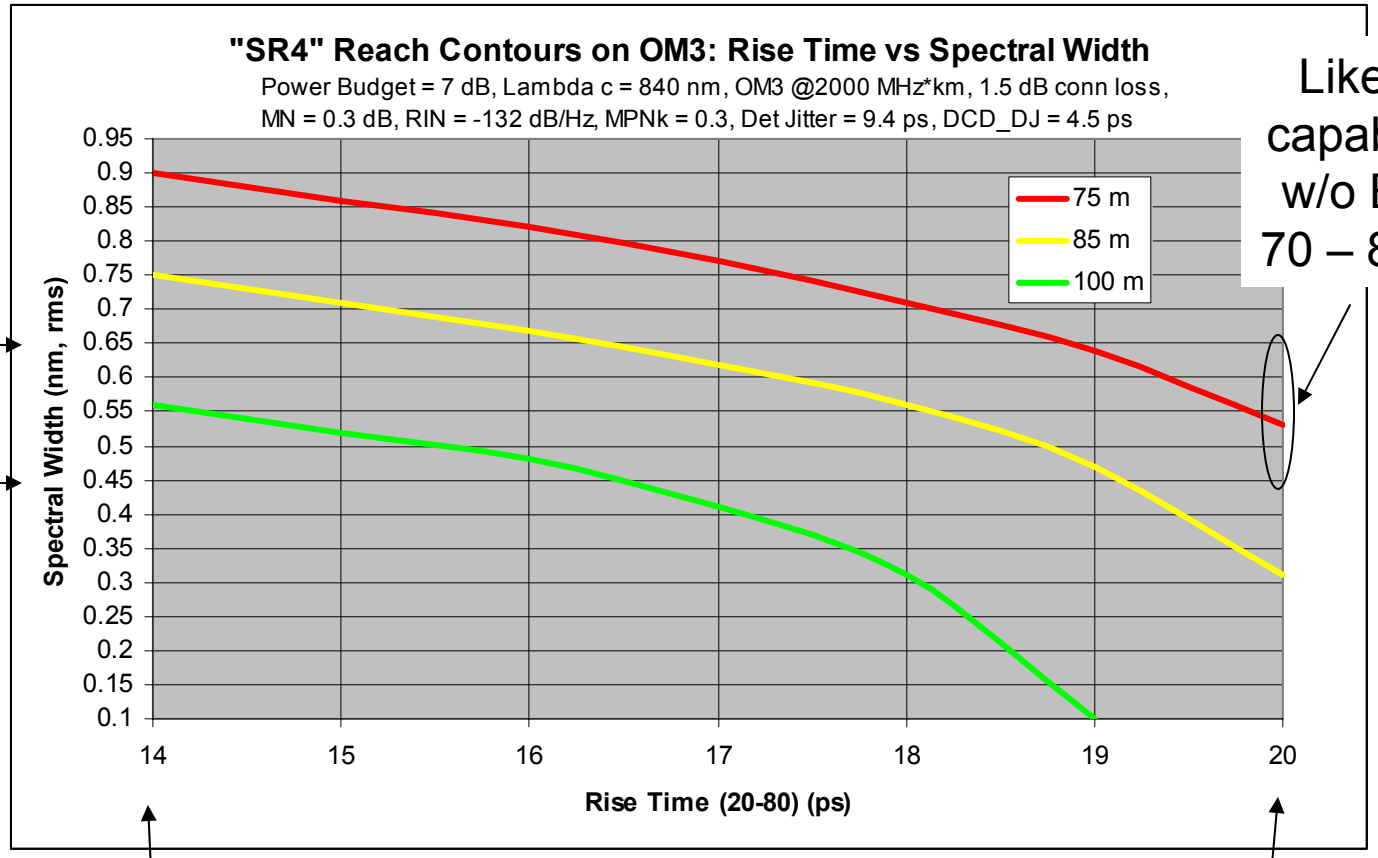
- Explore parameter space to establish possible solutions for supporting various reach targets for 850 nm systems at 25.8 Gbaud

- Exercise IEEE link model under certain assumptions

Assumptions

- Clock recovery required (at this time)
  - Jitter budget is biggest impairment for 100G-SR10
- VCSEL speed and spectral width are key performance concerns
  - Reported speeds not scaling proportionally to 25G
  - Spectral width relaxed by >40% for 100G-SR10

OM3 Reach Contours



100G-SR10

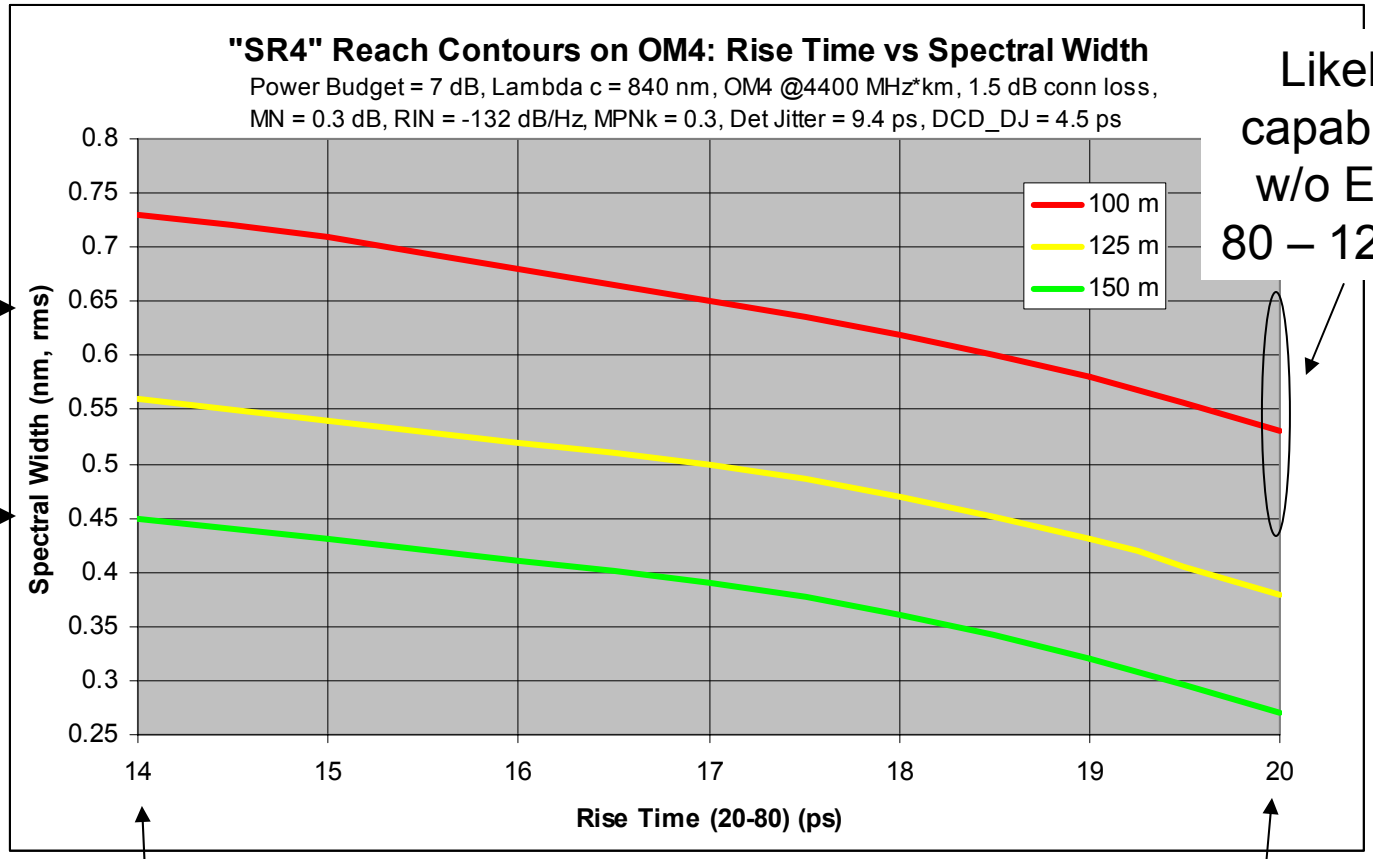
10G-SR

Likely capability w/o EQ. 70 – 80 m

Speed scaled to 25 Gbaud

Speed reported as likely

OM4 Reach Contours



100G-SR10

10G-SR

Likely capability w/o EQ. 80 – 120 m

Speed scaled to 25 Gbaud

Speed reported as likely

Equalization

- Modest equalization would compensate slow VCSELs
  - Explore fixed-coefficient 1- and 2-tap DFE
- With clock recovery employed, fixed DFE is incremental
- Modest EQ would allow seamless upgrade path
  - 40GBASE-SR4 to 100GBASE-SR4
  - Without change to cabling
  - Without reconfiguration of data center

Thank You