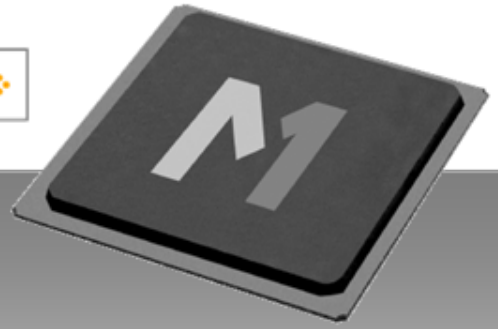
Considerations for Electrical Objectives



Sept 2011
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Agenda

- Background
  - CFI electrical material
  - Areas of study in relation to CSMA/CD model
  - Chip-to-module background
- Questions to be answered
  - CAUI-4: What host/medium reach is supported at required power consumption
  - CPPI-4: What host/medium reach is supported, what are the thermal / cost benefits
  - Enhanced CAUI-4: Is there benefit to adding capability to the CAUI interface which in turn increases host or medium reach extension
- Potential Electrical Objective

Technology Used for 802.3ba (from CFI)

- Electrical interfaces based on 10 Gb/s
  - 10x10G electrical channels, differential -> **40 high speed pins** just for data
  - ASIC/FPGA I/O challenged to achieve high enough density
    - 32 CXP connectors possible on a faceplate would require 320 - 10G channels
  - 25Gb/s signaling too challenging at the time
  - Connector technology for 25Gb/s not available at the time
  - Low power 25Gb/s I/O not available at the time

CAUI Interface Loss Summary

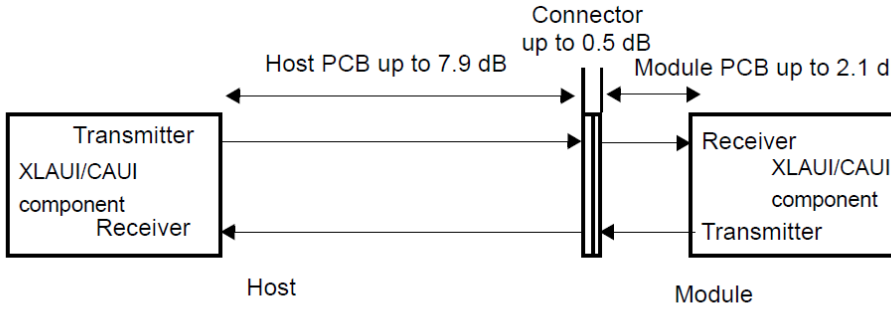


Figure 83B–2—Chip-module loss budget at 5.15625 GHz

CPPI Interface Loss

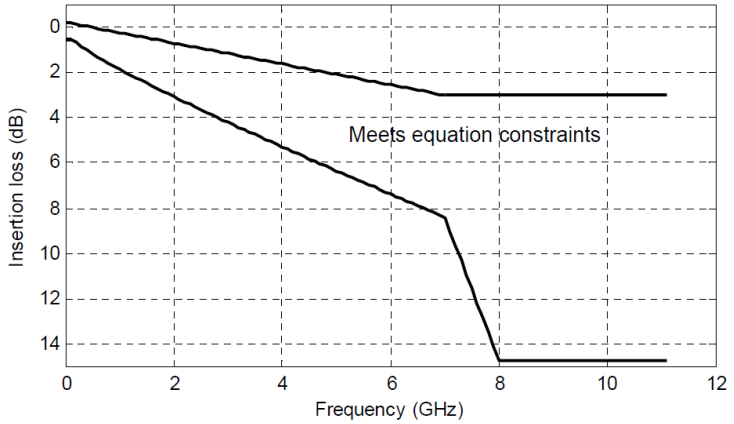
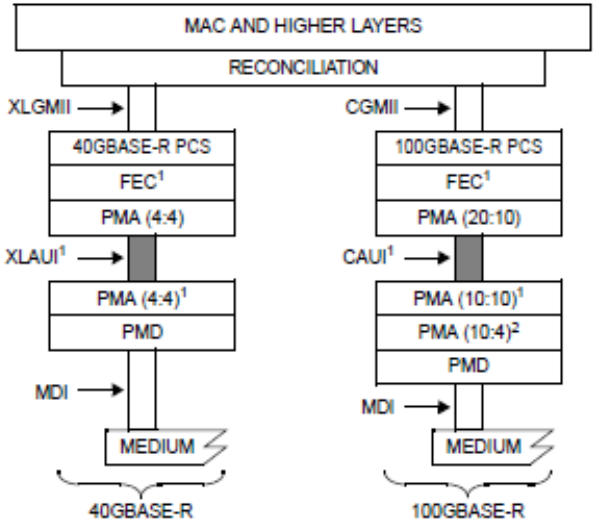


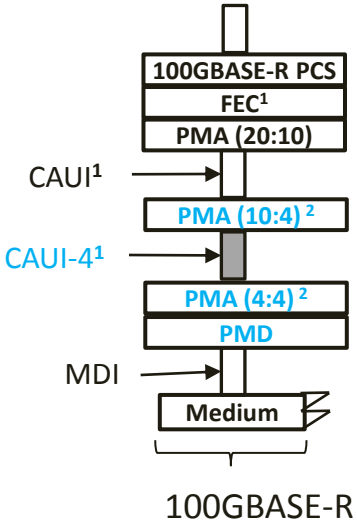
Figure 86A–11—Recommended insertion loss limits of host PCB, connector and HCB

Potential areas for Cu study (from CFI)

- 4 x 25 GBd
- NRZ modulation format
- CAUI-4 (retimed 4 lane)
- CPPI-4 (un-retimed or equivalent 4 lane)
  - Impact upon optical transmitter and receiver performance
- Performance of 4 x 25 GBd electrical connector and channel
- Equalization & de-emphasis requirements
- Electrical interface jitter budget, amplitude requirements

Areas for Study Relative to CSMA/CD LAN Model



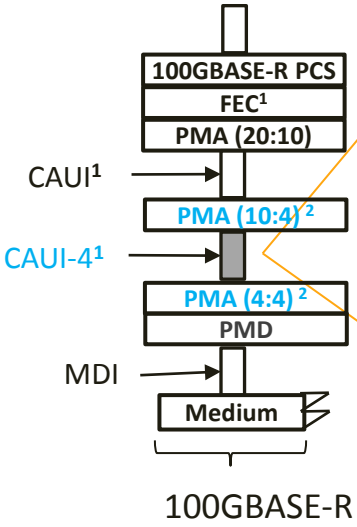


CAUI = 100 Gb/s ATTACHMENT UNIT INTERFACE
CGMII = 100 Gb/s MEDIA INDEPENDENT INTERFACE
FEC = FORWARD ERROR CORRECTION
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
XLAUI = 40 Gb/s ATTACHMENT UNIT INTERFACE
XLGMII = 40 Gb/s MEDIA INDEPENDENT INTERFACE

NOTE 1—OPTIONAL OR OMITTED DEPENDING ON PHY TYPE
NOTE 2—CONDITIONAL BASED ON PMD TYPE

Figure 83A–1—Example relationship of XLAUI and CAUI to IEEE 802.3 CSMA/CD LAN model

CAUI-4



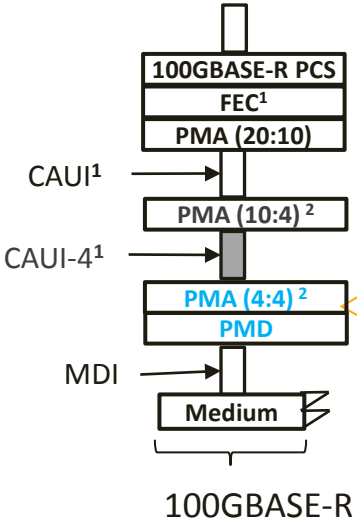
Balancing Act:

- PMA 10:4 performance, power, cost
- Host channel length requirements, connector performance (and other impairments)
- PMA 4:4 performance, power, cost

Desired Result

- Definition of a 4 lane 100G chip to module interface
  - Electrical I/O, Evaluation methodology

PMA (4:4) & PMD



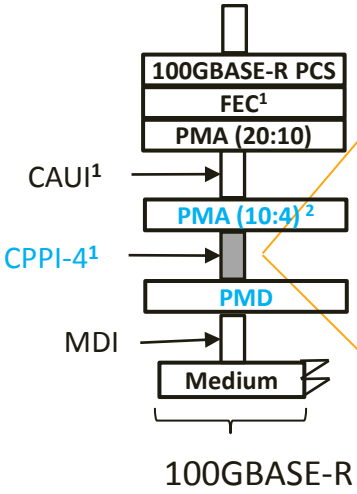
Balancing Act:

- PMA 4:4 performance, power, cost
- Required I/O for PMD – not exposed
  - In conjunction with optical tracks

Desired Result

- Closed jitter / power budget for specified link reach

CPPI-4



Balancing Act:

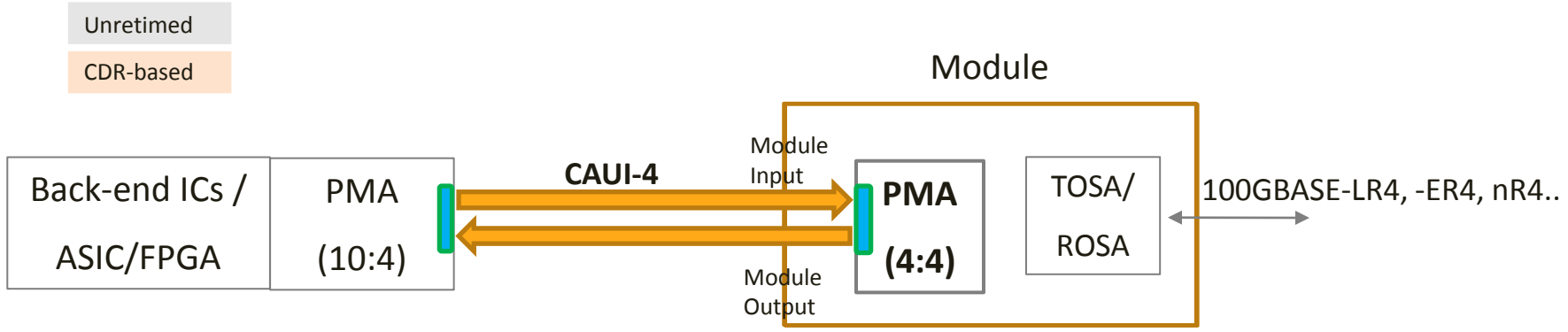
- PMA 10:4 or PMA 4:4 performance, power, cost
- Host channel length requirements, connector performance and other impairments
- Required I/O for PMD
  - In conjunction with optical tracks

Desired Result

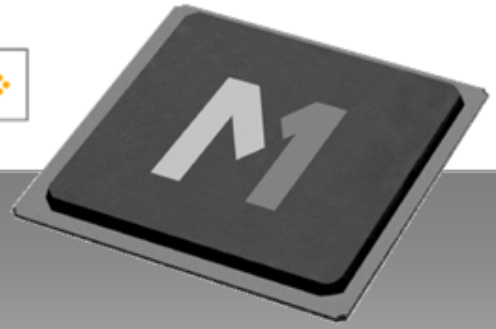
- Closed jitter / power budget
- Definition of a 4 lane 100G unretimed chip to module interface
  - Electrical I/O, Evaluation methodology

Optical Chip-Module Background

Interface	Data Rate	Module Output (TJ UIpp)	Approx Channel Loss at Nyquist (dB)	Module Input (TJ Uipp)
XFI	11.1G	0.34	9.6	0.61
SFI	11.1G	0.7	9	0.28
16GFC	14.025G	0.36	12	0.45
PPI	10.3125G	J9 = 0.65	6.9	J9 = 0.29
CAUI	10.3125G	0.4	10.5	0.62
OIF-28G VSR	28G		10	
32GFC	28G		20	



Questions to be answered



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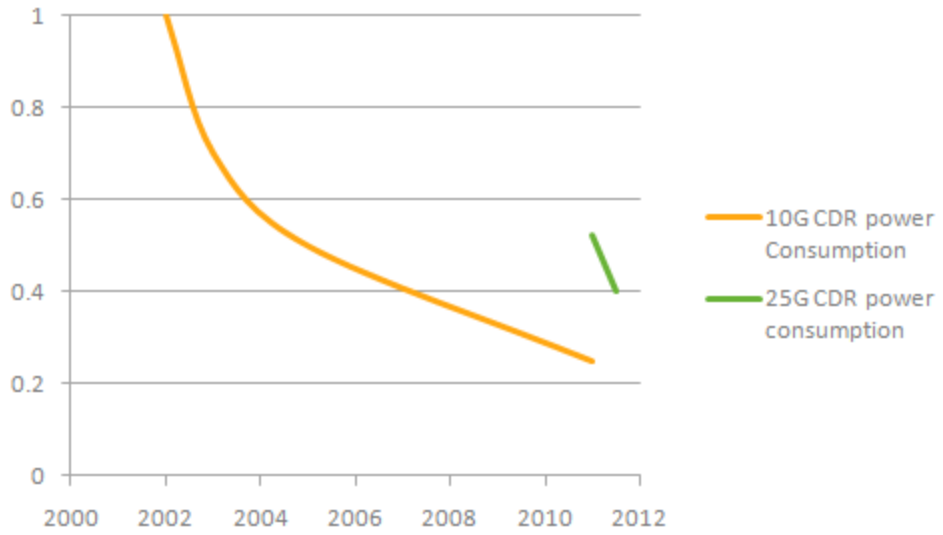
CAUI-4: What host/medium reach is supported…

- Reach for host:
  - OIF VSR is targeting ~10dB loss at ~12.5GHz which equates to a few inches on lower cost material
  - 802.3ba CAUI targets ~10 inches interconnect distance
  - Higher reach = increased flexibility for power/cost optimizations
    - What loss enables highest level of integration on the host?
- Reach for the medium
  - Retimed interface provides for highest jitter budget for channel
  - 32GFC (~28Gb/s) goal of 100m on OM4

CAUI-4:… at required power consumption

PMA (4:4) Benefits	PMA (4:4) Costs
Largest jitter budget for host, module, and media	Power & area Consider thermal and area budgets
PMD performance is isolated from host design, host design is isolated from PMD	

Normalized Per Lane PMA CDR Power Consumption over time



25G CDRs are starting at less power than the first generation 10G CDRs and are on the steep part of their power reduction curve

CPPI-4: What host/medium reach is supported, what are the thermal / cost benefits

Table 86A–3—nPPI module electrical output specifications at TP4

Parameter description	Min	Max	Units	Conditions
Single ended output voltage tolerance	–0.3	4	V	Referred to signal common
AC common-mode output voltage (RMS)	—	7.5	mV	
Termination mismatch at 1 MHz	—	5	%	
Differential output return loss	See 86A.4.2.1	—	dB	10 MHz to 11.1 GHz
Common-mode output return loss	See 86A.4.2.2	—	dB	10 MHz to 11.1 GHz
Output transition time, 20% to 80%	28	—	ps	
J2 Jitter output	—	0.42	UI	
J9 Jitter output	—	0.65	UI	
	Specification values			
Eye mask coordinates: X1, X2 Y1, Y2	0.29, 0.5 150, 425		UI mV	Hit ratio = 5×10^{-5}
Crosstalk source VMA, each lane	700		mV	At TP1a
Crosstalk source transition times, 20% to 80%	37		ps	At TP1a

CPPI-4

Assuming UI scaling of nPPI

	TP4 Jitter Distribution (UI)	TP4 Jitter Distribution (ps)
DDJpp	0.456	18ps
RJpp	0.40	16ps
J2	0.42	16ps
J9	0.65	25ps
TJ	0.70	27ps

http://www.ieee802.org/3/ba/public/jan10/petrilla_01_0110.pdf

Eye opening before host channel: 11.6ps

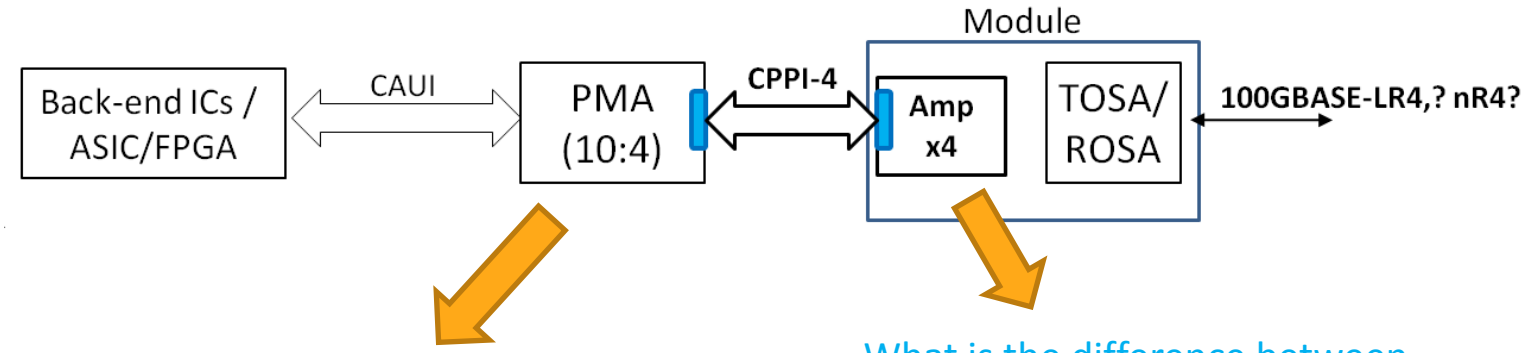
Host channel will introduce additional bandwidth impairments which will not be equalized perfectly. Extremely high bandwidth required to recover from DDPWS

Tx Jitter budget will be equally as challenging

Host length less than a few inches on low cost material

CPPI-4: What host/medium reach is supported, what are the thermal / cost benefits

PMD Interface Benefits	PMD Interface Costs
Power & area Consider thermal and area budgets	Jitter / optical budget Impacts PMD reach / channel goals Additional cost and complexity for PMD & host design
	Manufacturability Host exposed to PMD impairments and PMD exposed to host impairments



If CPPI-4 interface is very low loss, host silicon will persist

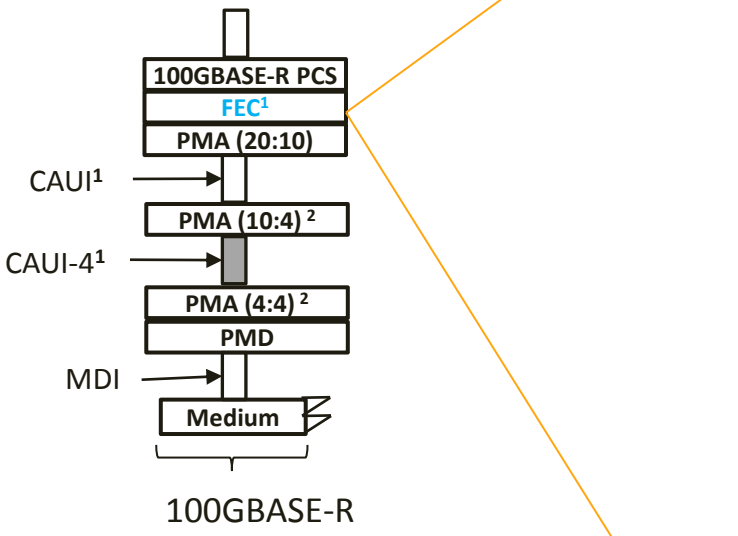
What is the difference between amplification and CDR functionality?

CAUI-4 & CPPI-4 Comparison

- CAUI-4 (CDR based interface)
  - Chip-module interface which can close jitter budget across PMD types
    - Take a forward view of delta in power & area for CDR functionality when considering thermal budget
  - Useful as a chip-to-chip interface as well as a chip-module interface
- CPPI-4 (un-retimed or equivalent 4 lane)
  - Chip-module interface with TBD jitter budget for host and medium
  - Goal to save power within the module
    - Implications for hosts & optical reach

Enhanced CAUI

- Is there an opportunity to use FEC or more powerful equalization to increase channel length



FEC currently an optional sub-layer in 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10

• Low gain FEC originally used in 10GBASE-KR to correct for single burst errors associated with DFE Error Propagation

FEC is currently not used in optical links in 802.3ba

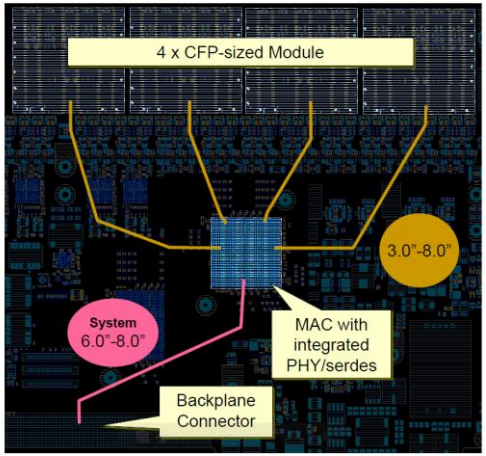
•Use would require new sublayer for optical links which could impact compatibility, bit rate, and latency

•FEC is not needed to close retimed chip-module electrical links

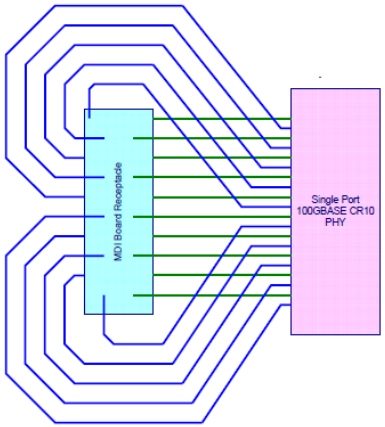
Electrical Objective

Define a 4-lane 100G chip-to-module interface

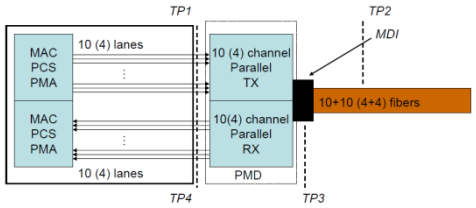
- Characteristics of the electrical interface dependent on:
  - Jitter budget & reach objective for host
  - Jitter budget & reach objective for Link
  - Other application constraints



Example Host Board for CAUI (http://www.ieee802.org/3/ba/public/jul08/nicholl_01_0708.pdf)

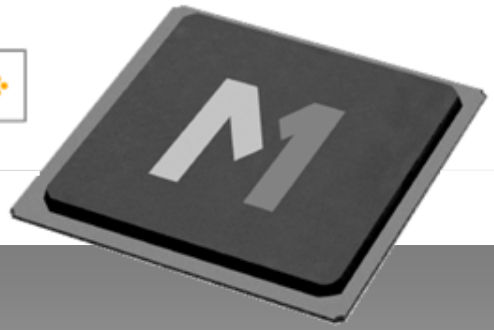


Example host board for SR10 (http://www.ieee802.org/3/ba/public/jul09/gustlin_04_0709.pdf)



SR10 Budgeting Proposal (http://grouper.ieee.org/groups/802/3/ba/public/may08/600933_01_0508.pdf)

THANK YOU!



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