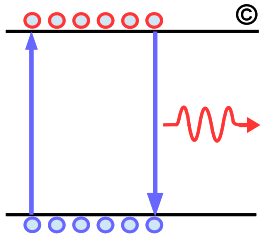

The Benefit of Matching SerDes Rate to Optical Lane Rate

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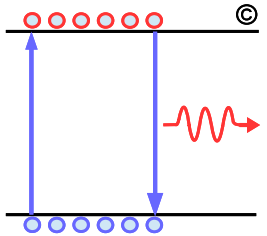
Long Beach

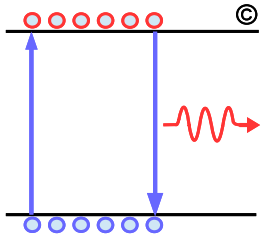
January 16, 2019

Overview

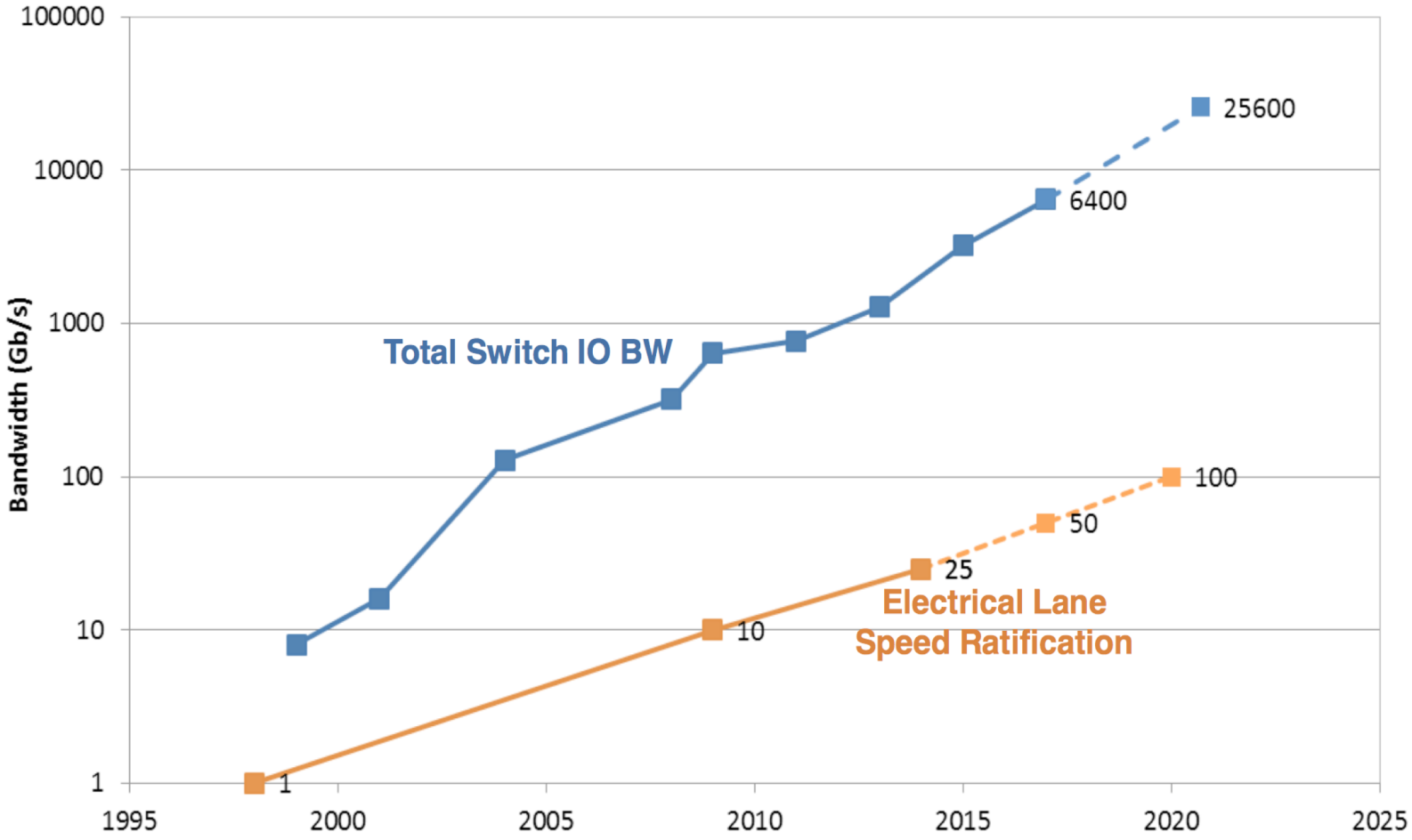


- SerDes rate and faceplate BW are doubling to enable 25.6 Tb
- 100G ASIC IO are coming
- 100G signaling enables 800G modules
- Simplest PMD implementations in support of 25.6 Tb systems

Switch BW Doubling Every ~2.5 Years

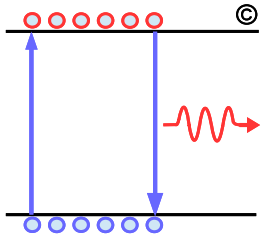


- By 2020 100G/lane ASIC IO will enable 25.6 Tb switches
- The key driver to double switch BW has been doubling of SerDes rate
- To support 25.6 Tb front panel faceplate the module IO must migrate from 50G to 100G IO
- 32 QSFP-dd or OSFP each will support an aggregate BW of 800G.

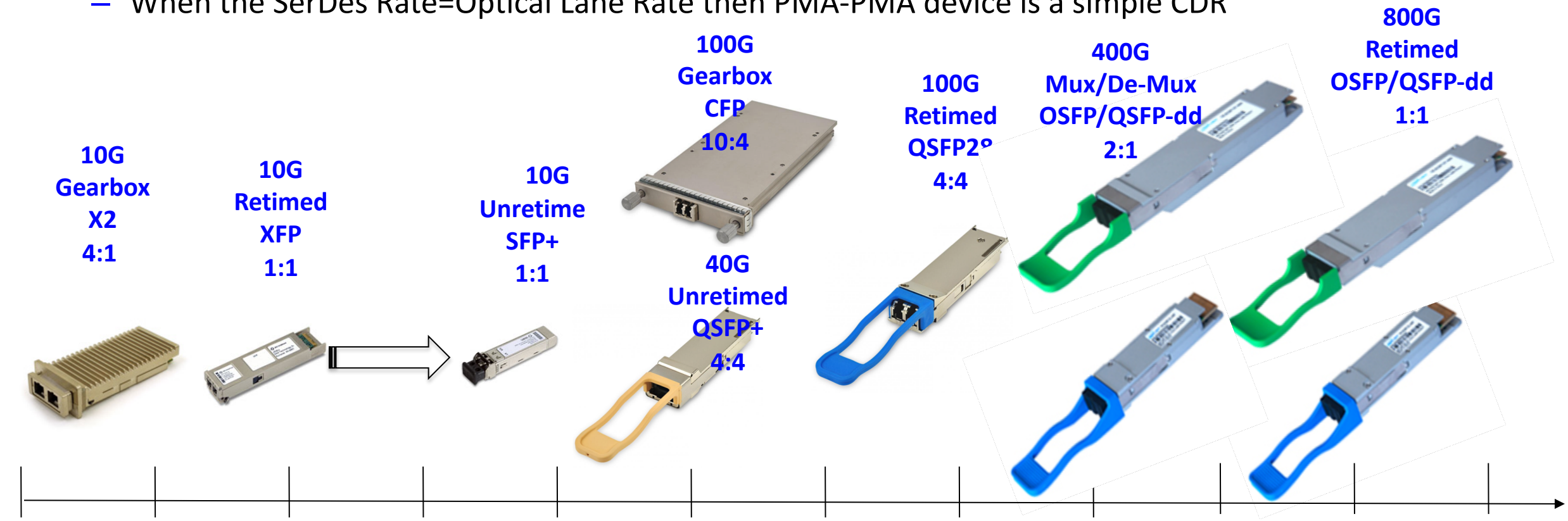


http://www.ieee802.org/3/cfi/1117_3/CFI_03_1117.pdf

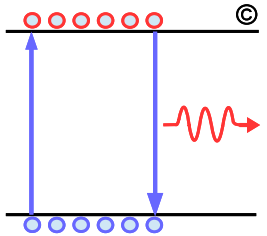
100G Signaling Enables 800G Modules/25.6 Tb Systems



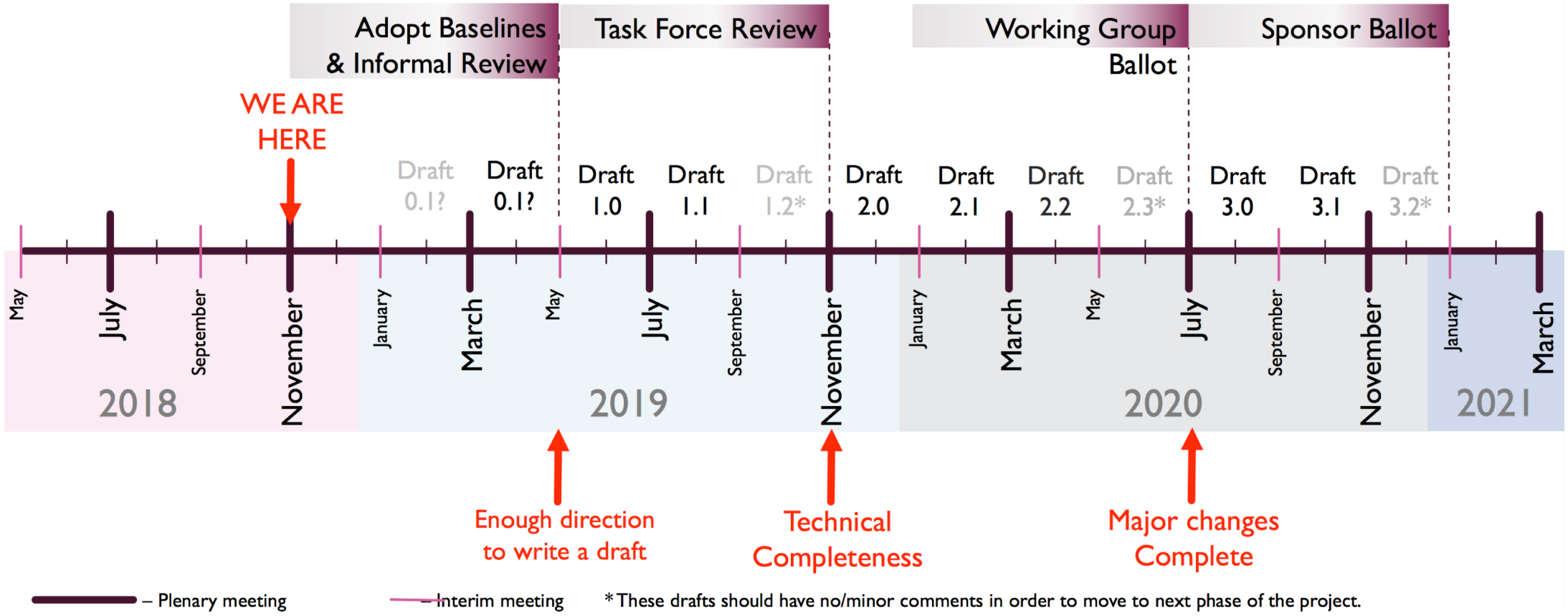
- **Over last 6+ generation of optical module the switch SerDes IO rate has always converged to optical signaling to deliver more efficient and lower cost PMD**
  - When the SerDes Rate=Optical Lane Rate then PMA-PMA device is a simple CDR



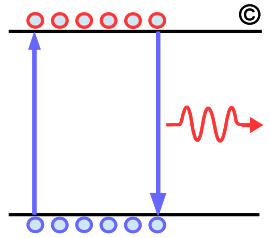
802.3ck Proposed Time Line



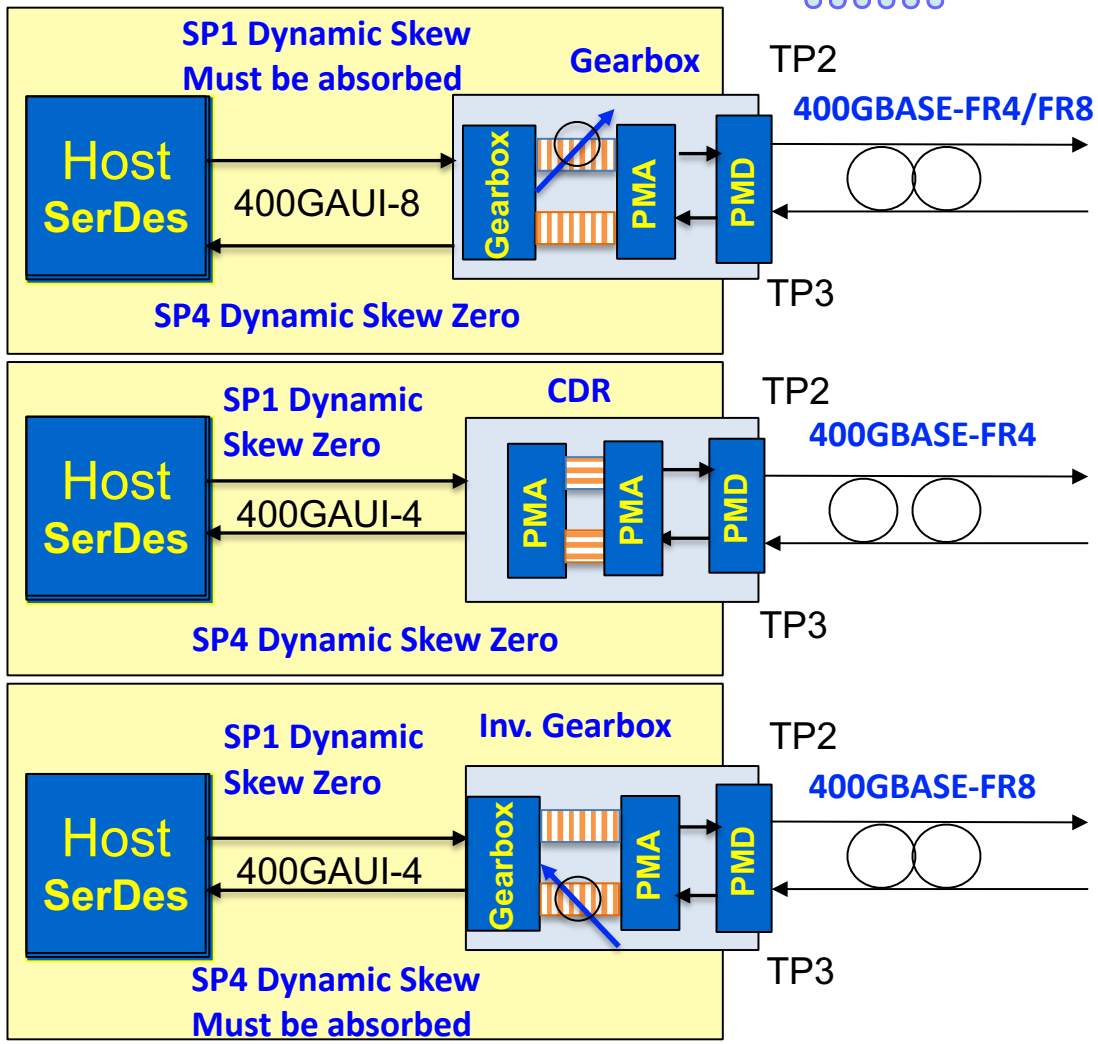
- **802.3ck project goal is developing 100G ASIC IO to enable 25.6 Tb switches**



The Benefit of Matching ASIC IO to Optics Signal Rate

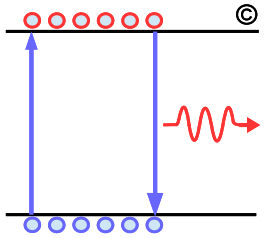


- **ASIC IO speed < Module IO speed and optics signaling**
  - Supports only 12.8 Tb faceplate
  - The module PMA-PMA is a Gearbox (FR8 PMA is a CDR)
  - 5 UI of dynamic skew at SP1 must be absorbed
  - A cleanup PLL with > 5 UI FIFO necessary to reduce impact of jitter transfer doubling since both 26.55 GBd and 53.1 GBd CDRs have corner frequency of 4 MHz
- **ASIC IO speed = Module IO speed and Optics signaling**
  - Supports 25.6 Tb faceplate
  - The module PMA-PMA is a simple pass through "CDR"
- **ASIC IO speed > Module IO speed and optics signaling**
  - Supports 25.6 Tb faceplate
  - The module PMA-PMA is a Gearbox
  - Large 90 UI at 26.55 GBd (180* UI likely at 53.1 GBd) dynamic skew at SP4 must be absorbed
  - Impact of rouge clock content should be considered.



* 802.3ck likely will set the dynamic skew at SP4 to 180 UI for 53.1 GBd.

Summary



- **Doubling SerDes rate from 50G to 100G will enable 25.6 Tb switch generation**
  - Given the timeline of 802.3ck expect to see 100G switch ASIC in next 18 month
- **100G/lane electrical signaling is necessary to support 25.6 Tb faceplate in 1 RU with 32 QSFP-dd or OSFP modules**
- **Given that modules electrical interface will operate at 100G/lane any optical PMDs not operating at 100G/lane would require a more complex and costly PMA-PMA device such as an inverse Gearbox with FIFO and dynamic skew alignment**
- **Defining 100GbE 2/10 km PMDs and 400bE 2/10 km PMDs based on 100G/lane signaling matching the ASIC IO rate will allow replacing the more complex Gearbox chips with simple CDR chips**
  - Enabling lower cost PMD implementations in support 25.6 Tb systems.