

Confirming Support for New 10km PMDs

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IEEE 100G per lane Study Group status

PMD Objectives have been adopted by the Study Group for the following:

- Define a single-wavelength 100 Gb/s PHY for operation over SMF with lengths up to at least 2 km
- **Define a single-wavelength 100 Gb/s PHY for operation over SMF with lengths up to at least 10 km**
- Define a four-wavelength 400 Gb/s PHY for operation over SMF with lengths up to at least 2 km
- **Define a four-wavelength 400 Gb/s PHY for operation over SMF with lengths up to at least 10 km**

[http://www.ieee802.org/3/100G_OPTX/Objectives Approved by SG Jan 2019.pdf](http://www.ieee802.org/3/100G_OPTX/Objectives_Approved_by_SG_Jan_2019.pdf)

Adopted by SG in Jan 2019 Y/N/A: 36:1:3

The CSD responses in support of these adopted objectives were reviewed and adopted by Study Group:

[http://www.ieee802.org/3/100G_OPTX/CSD responses Approved by SG Jan 2019.pdf](http://www.ieee802.org/3/100G_OPTX/CSD_responses_Approved_by_SG_Jan_2019.pdf)

Adopted by SG in Jan 2019 Y/N/A: 39:0:1

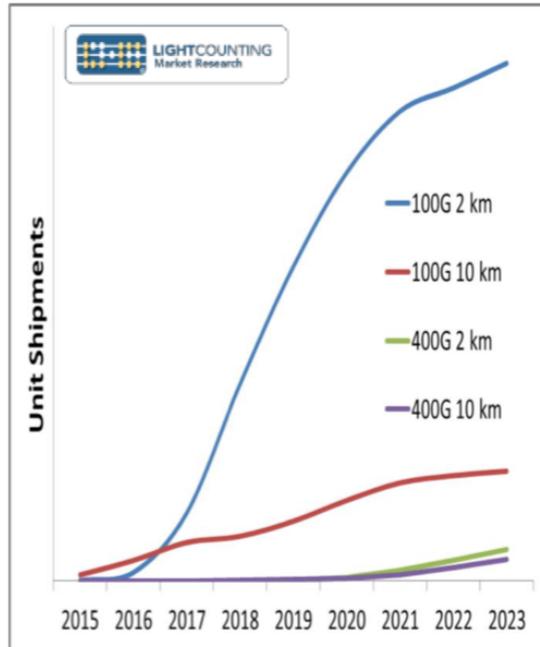
Focusing on 10km PMDs

In spite of the demonstrated broad approval of the Study Group motions, some concern was raised whether the market needed or was ready for these new 100G and 400G 10 km PMDs?

This contribution provides a double-check into the motivation behind having all these PMD objectives together.

Market View – from Jan meeting

Ethernet Market



Courtesy Dale Murray, Light Counting

IEEE 802.3 100 Gb/s per lane optical PHYs Study Group

Comments

- Strong market traction for 100G 2km and 10km
 - 2km based on 100G CWDM4 MSA
 - 10km based on IEEE LR4
- 100G 2km volume ramp coincided with the availability of x4 lane CWDM4 MSA interfaces
- Aggressive 100G cost reduction continuing as volume increases
 - Will continue as the market searches for the lowest cost solution
 - Key focus on < 2km reaches
- 400G ecosystem beginning to emerge
 - 12.8TB switch ASICs sampling
 - 32 port hardware switches demo'ing
 - 400G x4 lane 2km optical modules demo'ing
- 400G interconnects expected to surpass 4M in 2023
- Existing Ethernet standards do not cover targeted 400Gbps x4 optical interconnect

Quick Observations

1. 100G rapid growth continues
2. 2 km forecasts always higher than 10 km
3. 400G forecasts < 100G forecasts

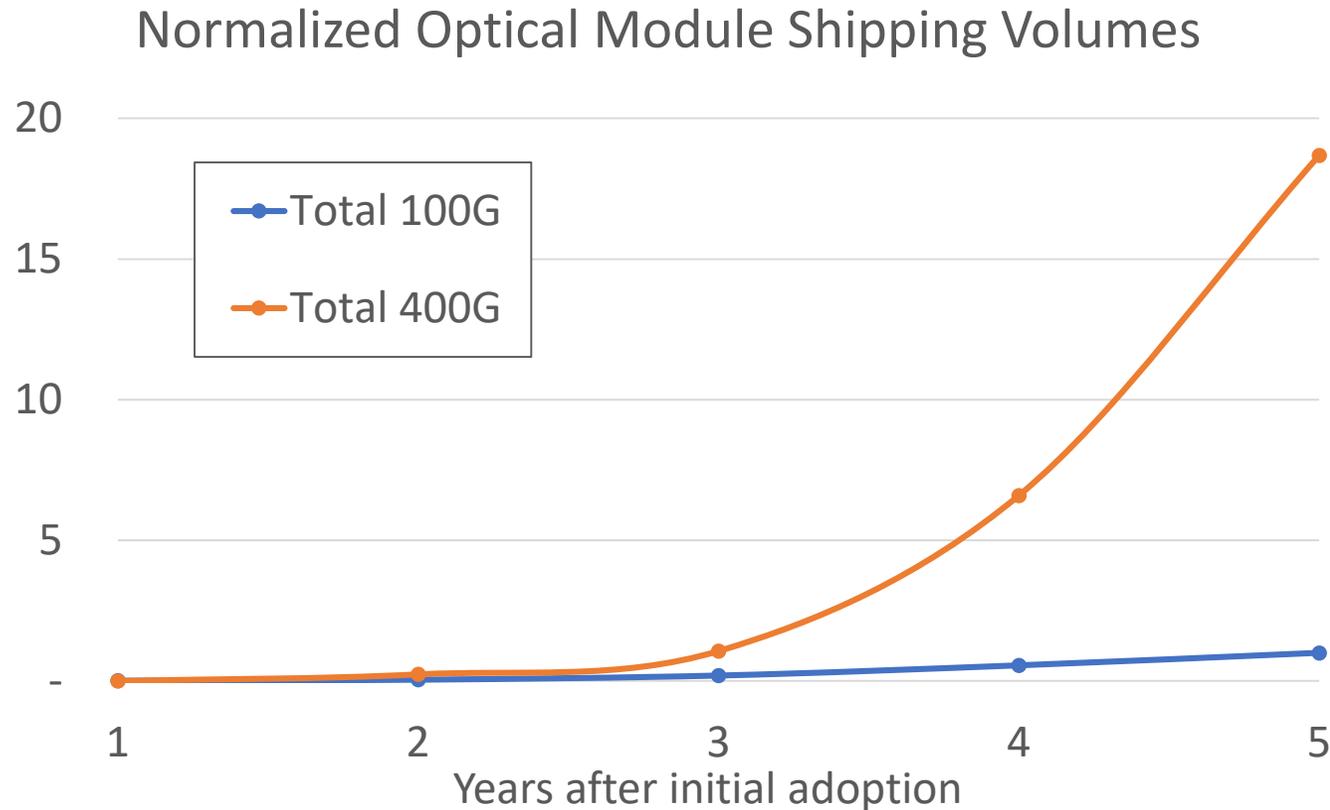
Combining 2&3 might lead to a conclusion that defining a new 400G 10km PMD now is too soon.

However, that would ignore the development and deployment synergies that are enhanced by defining both 2 km and 10 km simultaneously.

History of 100 GbE shows that both 2 km and 10 km are needed with 2 km being much higher. The same trend is expected for 400 GbE.

http://www.ieee802.org/3/100G_OPTX/public/Jan19/lewis_optx_01a_0119.pdf

400G market projections



Courtesy: LightCounting

Despite 400 GbE forecast projections looking less than 100 GbE, comparing the ramp from initial availability shows that 400 GbE will have a significantly faster ramp.

Year 5 of 400 GbE is approx. 20x larger than Year 5 of 100 GbE

Driven by multiple markets (Service Provider and Cloud DC) looking to adopt at same time.

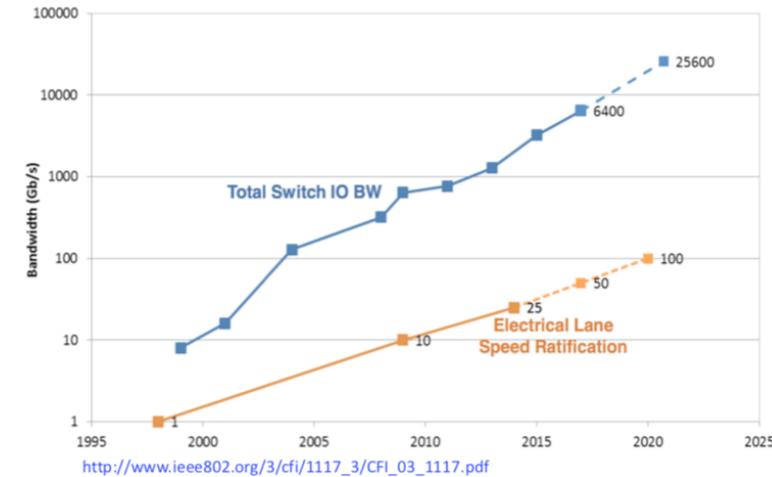
This provide an exciting challenge for equipment and component manufacturers

System equipment perspective

- Host design is complex. 12.8 Tb/s designs today

→ 25.6T & 51.2T

- High speed signaling
- High power ASICs
- Dense optical modules
- Optimized component interconnection lowers power and cost



The Benefit of Matching ASIC IO to Optics Signal Rate

- ❑ **ASIC IO speed < Module IO speed and optics signaling**
 - Supports only 12.8 Tb faceplate
 - The module PMA-PMA is a Gearbox (FR8 PMA is a CDR)
 - 5 UI of dynamic skew at SP1 must be absorbed
 - A cleanup PLL with > 5 UI FIFO necessary to reduce impact of jitter transfer doubling since both 26.55 GBd and 53.1 GBd CDRs have corner frequency of 4 MHz
- ❑ **ASIC IO speed = Module IO speed and Optics signaling**
 - Supports 25.6 Tb faceplate
 - The module PMA-PMA is a simple pass through "CDR"
- ❑ **ASIC IO speed > Module IO speed and optics signaling**
 - Supports 25.6 Tb faceplate
 - The module PMA-PMA is a Gearbox
 - Large 90 UI at 26.55 GBd (180* UI likely at 53.1 GBd) dynamic skew at SP4 must be absorbed
 - Impact of rouge clock content should be considered.

* 802.3ck likely will set the dynamic skew at SP4 to 180 UI for 53.1 GBd.
A. Ghiasi 100 Gb/s per Lane Optical PHY Study Group

The benefits of matching ASIC IO and Optical Signal rate simplifies that interconnect.

With 100 Gb/s ASIC in development, the impact on host design needs to be considered.

System Vendor Perspective on 10 km PMDs

- 400 GbE capable systems designed today around 50 Gb/s ASIC IO
- Soon to be based around 100 Gb/s ASIC IO
- A simplified host design occurs when all reaches are supportable with common design
 - 400G-DR4 and 400G-FR4 expected to be dominant PMDs
 - 400G-LR4 allows common host design
 - Current 400G-LR8 would need reverse gear box on systems with 100 Gb/s ASIC IO that is seen as burdensome in terms of size and power, and thus cost
- Anticipated synergy of technology between 2 km and 10 km attractive to help towards goal of lower costs

Module Manufacturer Perspective

- Manufacturers are ready to leverage 100G-lambda optical technology ubiquitously for 2 km and 10 km reaches based on their 500 m efforts
- Single-port modules such as QSFP28 for 100G-DR are emerging in the market, where technology is ready to support 2 km and 10 km reaches only hindered by lack of specifications for interoperability
- Module manufacturers have functioning 400G prototypes such as in QSFP-DD and OSFP form factors for 2 km and 10 km reaches via the use of four different 100G wavelengths and use of optical mux/dmux, where interoperability requires choice of
 - Wavelength grid
 - Tx and Rx per-lane specifications

Conclusions

Despite:

- The usual higher deployment of 2 km SMF PMDs vs. 10 km SMF PMDs
- The higher volumes of 100 GbE vs. 400 GbE

It still makes market and technology sense to specify both 100 GbE and 400 GbE 10 km SMF PMDs now.

- It simplifies host designs and allows a common solution for all PMDs
- It enables technology and development re-use