# Proposal for a "Working Paper" proposing an initial draft for a 10GBASE-CX4 PMD

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**NOTE:** These first set of paragraphs come from clause 53.

# 54. Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4

## 54.1 Overview

This clause specifies the 10GBASE-CX4 PMD (including MDI) and the baseband medium. In order to form a complete Physical Layer, the PMD shall be integrated with the appropriate physical sublayers (see Table 54–1) and with the management functions which are accessible through the Management Interface defined in Clause 45, all of which are hereby incorporated by reference.

**Table 54–1—CX4 PMD type and associated physical layer clauses**

| Associated Clause | 10GBASE-CX4 |
|---|---|
| 46—RS and<br>XGMII[a] | Required<br>Optional |
| 47—XGXS and XAUI | Optional |
| 48—10GBASE-X PCS/PMA | Required |
| 49—10GBASE-R PCS | n/a |
| 50—10GBASE-W WIS | n/a |

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation must behave functionally as though the RS and XGMII were present.

Figure 54–1 shows the relationship of the PMD and MDI sublayers to the ISO/IEC (IEEE) OSI reference model.

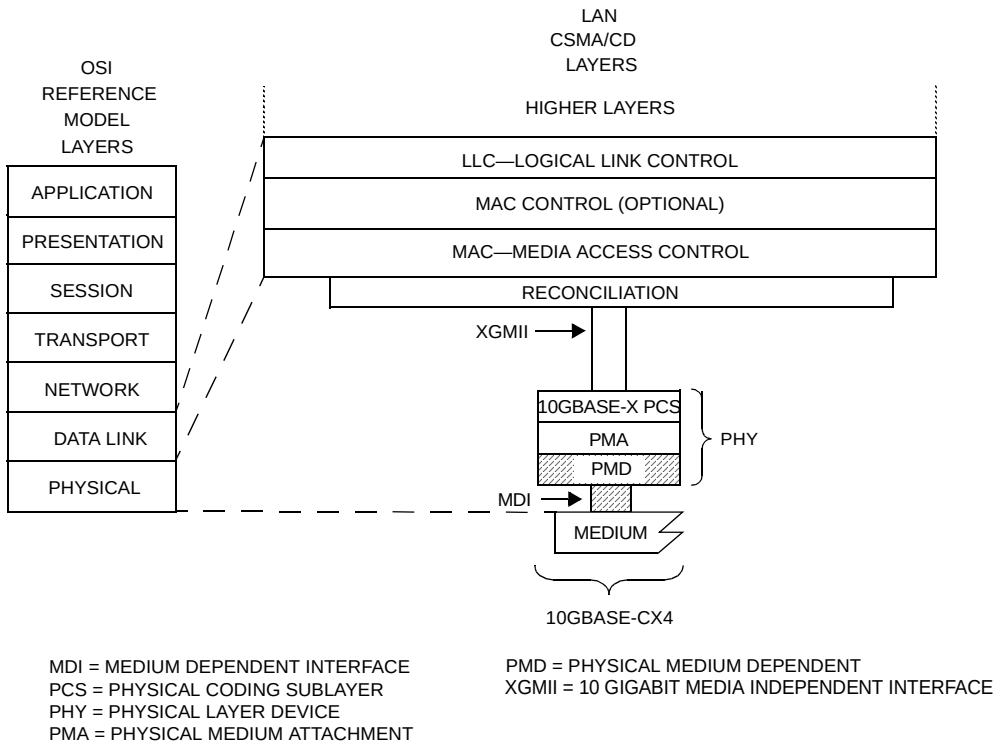



**Figure 54–1—10GBASE-CX4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model**

### 54.1.1 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 10GBASE-CX4 PMD. The service interface for this PMD is described in an abstract manner and do not imply any particular implementation. The PMD Service Interface supports the exchange of encoded data between peer PMA entities. The PMD translates the encoded data to and from signals suitable for the specified medium.

The following PMD service primitives are defined:

PMD_UNITDATA.request

PMD_UNITDATA.indicate

PMD_SIGNAL.indicate

### 54.1.2 PMD_UNITDATA.request

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMA to the PMD.

#### 54.1.2.1 Semantics of the service primitive

PMD_UNITDATA.request (tx_bit <0:3>)

The data conveyed by PMD_UNITDATA.request is a continuous sequence of four parallel code-group streams, one stream for each lane. The tx_bit <0:3> correspond to the bits in the tx_lane<0:3> bit streams. Each bit in the tx_bit parameter can take one of two values: ONE or ZERO.

#### 54.1.2.2 When generated

The PMA continuously sends four parallel code-group streams to the PMD at a nominal signaling speed of 3.125 GBaud.

#### 54.1.2.3 Effect of Receipt

Upon receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals on the MDI.

### 54.1.3 PMD_UNITDATA.indicate

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMD to the PMA.

#### 54.1.3.1 Semantics of the service primitive

PMD_UNITDATA.indicate (rx_bit <0:3>)

The data conveyed by PMD_UNITDATA.indicate is a continuous sequence of four parallel encoded bit streams. The rx_bit<0:3> correspond to the bits in the rx_lane<0:3> bit streams. Each bit in the rx_bit parameter can take one of two values: ONE or ZERO.

#### 54.1.3.2 When generated

The PMD continuously sends stream of bits to the PMA corresponding to the signals received from the MDI.

#### 54.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

### 54.1.4 PMD_SIGNAL.indicate

This primitive is generated by the PMD to indicate the status of the signals being received from the MDI.

#### 54.1.4.1 Semantics of the service primitive

PMD_SIGNAL.indicate (SIGNAL_DETECT)

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, rx_bit is undefined, but consequent actions based on PMD_UNITDATA.indicate, where necessary, interpret rx_bit as a logic ZERO.

NOTE—SIGNAL_DETECT = OK does not guarantee that rx_bit is known to be good. It is possible for a poor quality link to provide sufficient power for a SIGNAL_DETECT = OK indication and still not meet the $10^{-12}$ BER objective.

#### 54.1.4.2 When generated

The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT.

#### 54.1.4.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

## 54.2 PCS and PMA functionality

The 10GBase-CX4 PCS and PMA shall conform to the PCS and PMA defined in clause 48 unless otherwise noted herein.

## 54.3 Input / Output mapping

Figure 54–2 depicts the XGMII to MDI input / output mapping.

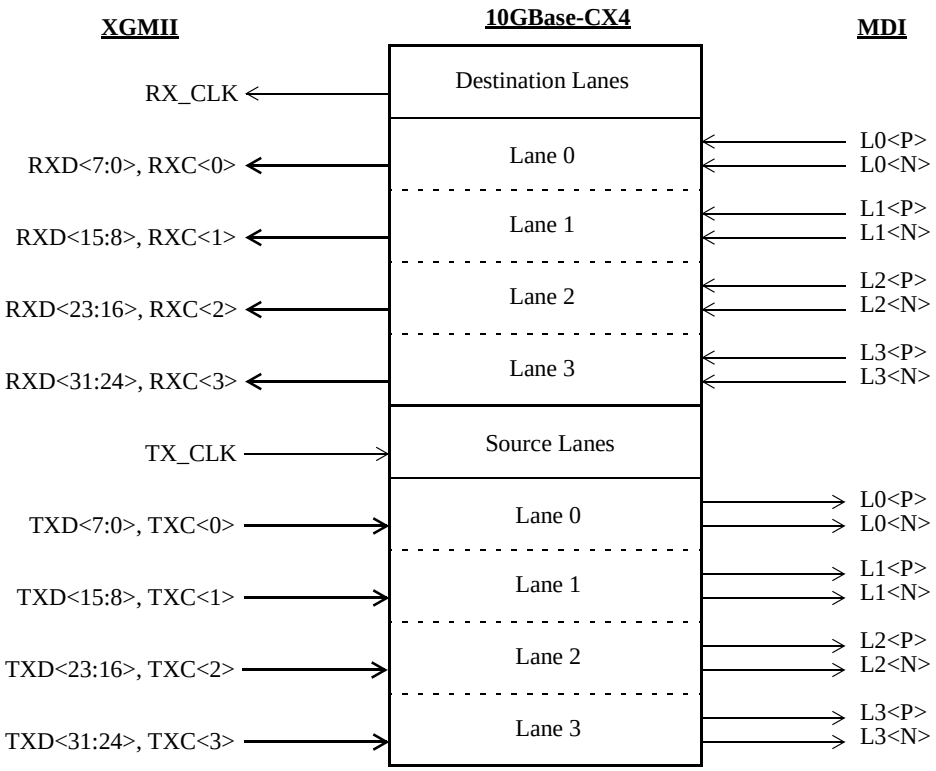



**Figure 54–2—10GBase-CX4 inputs and outputs**

## 54.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of transmit and receive delay contributed by the 10GBASE-X PCS shall be no more than 2048 BT.

The sum of transmit and receive delay contributed by the 10GBASE-CX4 PMD shall be no more than TBD (512??) BT (including 15 meters of cable).

The sum of transmit and receive delay contributed by the PCS, PMA and PMD shall be no more than TBD (2560?) BT (including 15 meters of cable).

## 54.5 PMD MDIO function mapping

**NOTE:** Does CX4 need these PMD MDIO functions or is Clause 48 PCS and PMA MDIO mapping functions sufficient?

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. Mapping of MDIO control variables to PMD control variables is shown in Table 54–2. Mapping of MDIO status variables to PMD status variables is shown in Table 54–3.

**Table 54–2—MDIO/PMD control variable mapping**

| MDIO control variable | PMA/PMD register name | Register/ bit number | PMD control variable |
|---|---|---|---|
| Reset | Control register 1 | 1.0.15 | PMD_reset |
| Global transmit disable | Control register 1 | 1.9.0 | Global_PMD_transmit_disable |
| Transmit disable 3 | Transmit disable register | 1.9.4 | PMD_transmit_disable_3 |
| Transmit disable 2 | Transmit disable register | 1.9.3 | PMD_transmit_disable_2 |
| Transmit disable 1 | Transmit disable register | 1.9.2 | PMD_transmit_disable_1 |
| Transmit disable 0 | Transmit disable register | 1.9.1 | PMD_transmit_disable_0 |

**Table 54–3—MDIO/PMD status variable mapping**

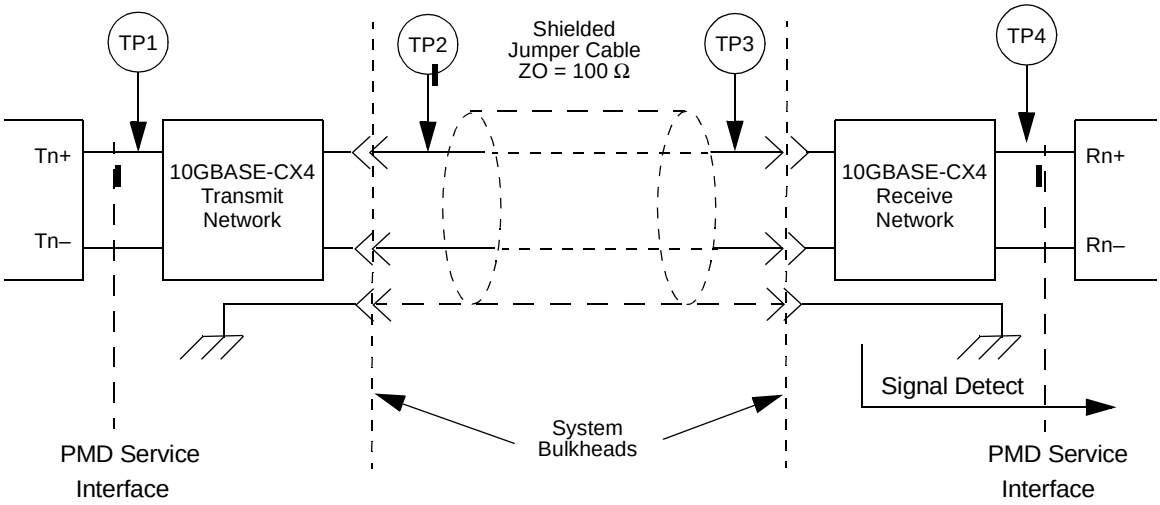
| MDIO status variable | PMA/PMD register name | Register/ bit number | PMD status variable |
|---|---|---|---|
| Local fault | Status register 1 | 1.1.7 | PMD_fault |
| Transmit fault | Status register 2 | 1.8.11 | PMD_transmit_fault |
| Receive fault | Status register 2 | 1.8.10 | PMD_receive_fault |
| Global PMD signal detect | Receive signal detect register | 1.10.0 | Global_PMD_signal_detect |
| PMD signal detect 3 | Receive signal detect register | 1.10.4 | PMD_signal_detect_3 |
| PMD signal detect 2 | Receive signal detect register | 1.10.3 | PMD_signal_detect_2 |
| PMD signal detect 1 | Receive signal detect register | 1.10.2 | PMD_signal_detect_1 |
| PMD signal detect 0 | Receive signal detect register | 1.10.1 | PMD_signal_detect_0 |

## 54.6 PMD functional specifications

The 10GBASE-CX4 PMD performs the Transmit and Receive functions which convey data between the PMD service interface and the MDI plus various management functions if the optional MDIO is implemented.

### 54.6.1 PMD block diagram

The PMD block diagram is shown in Figure 54–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The electrical transmit signal is defined at the output end of the connector (TP2), between TBD and TBD meters in length, of a type consistent with the link type connected to the transmitter receptacle defined in 54.14.2. Unless specified otherwise, all transmitter measurements and tests defined in 54.9.1 through 54.9.8 are made at TP2. The electrical receive signal is defined at the output of the cabling connector (TP3) at the MDI (see 54.14.3). Unless specified otherwise, all receiver measurements and tests defined in 54.9.9 through 54.9.15 are made at TP3.




NOTE—Jumper cable assembly shielding is attached to the system chassis via the connector shroud.

**Figure 54–3—10GBASE-CX4 link (half link is shown)**

+ and Tn- are the positive and negative sides of the transmit differential signal pair and Rn+ and Rn- are the positive and negative sides of the receive differential signal pair for Lane n ($n$ = 0, 1, 2, 3)

TP1 <0:3> and TP4 <0:3> are informative reference points that may be useful to implementers for testing components (these test points will not typically be testable in an implemented system).

### 54.6.2 PMD transmit function

The PMD Transmit function shall convert the four electronic bit streams requested by the PMD service interface message PMD_UNITDATA.request (tx_bit<0:3>) into four separate electrical signal streams. The four electrical signal streams shall then be delivered to the MDI, all according to the transmit electrical specifications in this clause. The higher output voltage of Tn+ minus Tn– (differential voltage) shall correspond to tx_bit = ONE.

### 54.6.3 PMD receive function

The PMD Receive function shall demultiplex the composite electrical signal stream received from the MDI into four separate electrical signal streams. The four electrical signal streams shall then be converted into four electronic bit streams for delivery to the PMD service interface using the message

PMD_UNITDATA.indicate (rx_bit<0:3>), all according to the receive electrical specifications in this clause. The higher electrical power level in each signal stream shall correspond to a rx_bit = ONE.

The PMD shall convey the bits received from the PMD_UNITDATA.request(tx_bit<0:3>) service primitive to the PMD service interface using the message PMD_UNITDATA.indicate(rx_bit<0:3>), where rx_bit<0:3> = tx_bit<0:3>.

### 54.6.4 Global PMD signal detect function

The Global PMD Receive Signal OK function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD_SIGNAL.indicate message is generated when a change in the value of SIGNAL_DETECT occurs.

SIGNAL_DETECT shall be a global indicator of the presence of electrical signals on all four lanes. The PMD receiver is not required to verify whether a compliant 10GBASE-CX4 signal is being received. This standard imposes no response time requirements on the generation of the SIGNAL_DETECT parameter.

**Table 54–4—SIGNAL_DETECT value definition**

| Receive conditions | Receive Signal OK value |
|---|---|
| For any lane; Input electrical power ≤ TBD dBm | FAIL |
| For all lanes;<br>[(Input_electrical power ≥ Receiver sensitivity (max) in OMA in Table 54–8)<br>AND<br>(compliant 10GBASE-CX4 signal input)] | OK |
| All other conditions | Unspecified |

As an unavoidable consequence of the requirements for the setting of the SIGNAL_DETECT parameter, implementations must provide adequate margin between the input electrical power level at which the SIGNAL_DETECT parameter is set to OK, and the inherent noise level of the PMD due to crosstalk, power supply noise, etc.

Various implementations of the Signal Detect function are permitted by this standard, including implementations that generate the SIGNAL_DETECT parameter values in response to the amplitude of the modulation of the electrical signal and implementations that respond to the average electrical power of the modulated electrical signal.

### 54.6.5 PMD lane by lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_n, where n represents the lane number in the range 0:3, value shall be continuously set in response to the amplitude of the average electrical power of the modulated electrical signal on its associated lane, according to the requirements of Table 54–4.

### 54.6.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

### 54.6.7 Global PMD transmit disable function

The Global_PMD_transmit_disable function is optional and allows all of the electrical transmitters to be disabled.

a) When a Global_PMD_transmit_disable variable is set to ONE, this function shall turn off all of the electrical transmitters so that the each transmitter meets the requirements of the Absolute output voltage limits in Table 54–7.
b) If a PMD_fault is detected, then the PMD may set the Global_PMD_transmit_disable to ONE, turning off the electrical transmitter in each lane. (**NOTE:** KEEP THIS OR TOSS IT?)

### 54.6.8 PMD lane by lane transmit disable function

The PMD_transmit_disable function is optional and allows the electrical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_n variable is set to ONE, this function shall turn off the electrical transmitter associated with that variable so that the transmitter meets the requirements of the Absolute output voltage limits in Table 54–7.
b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_n to ONE, turning off the electrical transmitter in each lane. (**NOTE:** KEEP THIS OR TOSS IT?)

If the optional PMD_lane_by_lane_transmit_disable function is not implemented in MDIO, an alternative method shall be provided to independently disable each transmit lane.

### 54.6.9 PMD fault function

**NOTE:** Do we need PMD fault detection when we have PCS fault detection?

If the MDIO is implemented, and the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to ONE.

### 54.6.10 PMD transmit fault function (optional)

If the MDIO is implemented, and the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to ONE.

### 54.6.11 PMD receive fault function (optional)

If the MDIO is implemented, and the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to ONE.

## 54.7 PMD to MDI electrical specifications

**NOTE:** These next set of paragraphs come from clause 39.

All interface specifications are valid only at the point of entry and exit from the equipment. These points are identified as points TP2 and TP3 as shown in Figure 54–3. The specifications assume that all measurements are made after a mated connector pair, relative to the source or destination.

TP1 and TP4 are standardized reference points for use by implementers to certify component conformance. The electrical specifications of the PMD service interface (TP1 and TP4) are not system compliance points

(these are not readily testable in a system implementation). It is expected that in many implementations TP1 and TP4 for 10GBase-CX4 will be common with 10GBASE-LX4 (<put xfer here> Clause 53).

PMD specifications shall be measured using the measurement techniques defined in TBD (put paragraph xfer here).

The reference points for all connections are those points TP2 and TP3 where the cabinet Faraday shield transitions between the cabinet and the jumper cable shield. If sections of transmission line exist within the Faraday shield, they are considered to be part of the associated transmit or receive network, and not part of the jumper cable assembly.

Schematics in the diagrams in this clause are for illustration only and do not represent the only feasible implementation.

### 54.7.1 Transmitter electrical specifications

The transmitter shall meet the specifications in Table 54–5.

**Table 54–5—Transmitter characteristics at TP2**

| Description | Value | Unit |
|---|---|---|
| Data rate | 3.125 | Gb/s |
| Clock tolerance | ±100 | ppm |
| Nominal signalling period | 320 | ps |
| Differential amplitude (p-p) | | |
| Max (worst case p-p) | TBD | mV |
| Min (opening) | 1100 | mV |
| Rise/Fall time (20-80%) | | |
| maximum | TBD | ps |
| minimum | TBD | ps |
| TBD other specifications | | |

For all links, the output driver shall be ac-coupled to the jumper cable assembly through a transmission network, and have output levels, measured at the input to the jumper cable assembly (TP2), meeting the eye diagram requirements of Figure 54–5 and Figure 54–6, when terminated as shown in Figure 54–4. The symbols X1 and X2 in Figure 54–5 and Figure 54–6 are defined in Table 54–6.

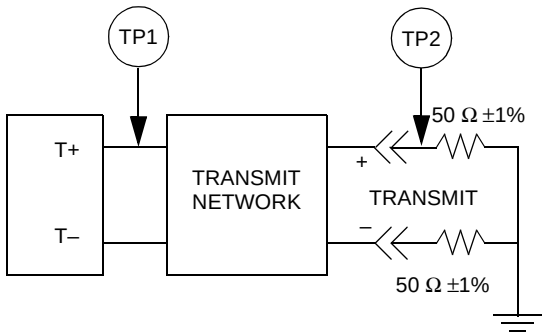



**Figure 54–4—Balanced transmitter test load**

The normalized amplitude limits in Figure 54–5 are set to allow signal overshoot of TBD 10% and undershoot of TBD 20%, relative to the amplitudes determined to be a logic 1 and 0. The absolute transmitter out-

put timing and amplitude requirements are specified in Table 54–5, Table 54–6, and Figure 54–6. The normalized transmitter output timing and amplitude requirements are specified in Table 54–5, Table 54–6, and Figure 54–5. The transmit masks of Figure 54–5 and Figure 54–6 are not used for response time and jitter specifications.

NOTE 1—The relationship between Figure 54–5 and Figure 54–6 can best be explained by a counter example. If a transmitter outputs a nominal 600 mV-ppd logic one level with overshoot to 900 mV-ppd, it will pass the absolute mask of Figure 54–6 but will not pass the normalized mask of Figure 54–5. Normalized, this signal would have 50% overshoot. This exceeds the 10% overshoot limit defined by the normalized eye mask.

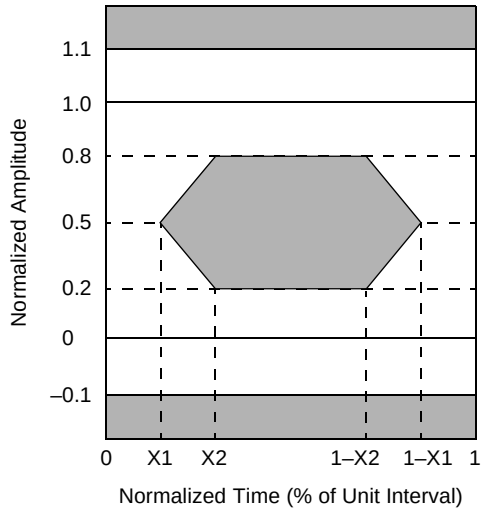



**Figure 54–5—Normalized eye diagram mask at TP2**

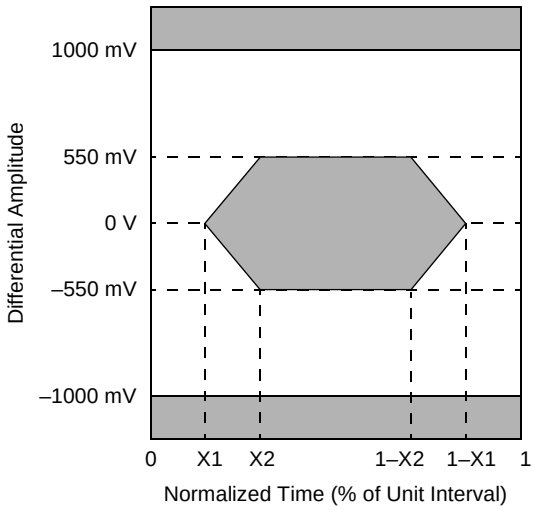



**Figure 54–6—Absolute eye diagram mask at TP2**

The recommended interface to electrical transmission media is via transformer or capacitive coupling.

NOTE 2—All specifications, unless specifically listed otherwise, are based on differential measurements.

NOTE 3—All times indicated for TDR measurements are recorded times. Recorded times are twice the transit time of the TDR signal.

NOTE 4—The transmit differential skew is the maximum allowed time difference (on both low-to-high and high-to low transitions) as measured at TP2, between the true and complement signals. This time difference is measured at the midway point on the signal swing of the true and complement signals. These are single-ended measurements.

**Table 54–6—Normalized time intervals for TP2**

| Symbol | Value | Units |
|---|---|---|
| X1 | TBD 0.14 | Unit Intervals (UI) |
| X2 | TBD 0.34 | Unit Intervals (UI) |

NOTE 5—The transmitter amplitude maximum specification identifies the maximum p-p signal that can be delivered into a resistive load matching that shown in Figure 54–4.

NOTE 6—The transmitter amplitude minimum specification identifies the minimum allowed p-p eye amplitude opening that can be delivered into a resistive load matching that shown in Figure 54–4.

NOTE 7—The normalized 1 is that amplitude determined to be the average amplitude when driving a logic 1. The normalized 0 is that amplitude determined to be the average amplitude when driving a logic 0.

NOTE 8—Eye diagram assumes the presence of only high-frequency jitter components that are not tracked by the clock recovery circuit. For this standard the lower cutoff frequency for jitter is TBD 637 kHz.

### 54.7.2 Receiver electrical specifications

The receiver shall be ac-coupled to the media through a receive network located between TP3 and TP4 as shown in Figure 54–3. The receiver shall meet the signal requirements listed in Table 54–7.

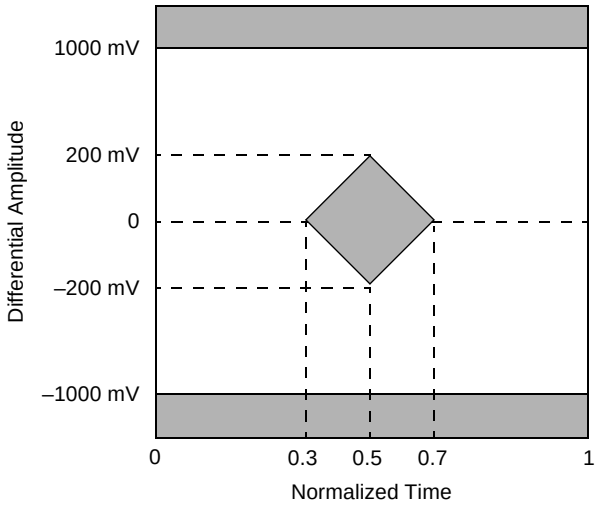



**Figure 54–7—Eye diagram mask at point-TP3**

**Table 54–7—Receiver characteristics (TP3)**

| Description | Value | Units |
|---|---|---|
| Data rate | 3.125 | Gb/s |
| Nominal signalling period | 320 | ps |
| Tolerance | ±100 | ppm |
| Minimum differential sensitivity (peak-peak) | TBD | mV |
| Maximum differential input (peak-peak) | TBD | mV |
| Input Impedance @ TP3 | | |
| TDR Rise Time | TBD | ps |
| Exception_window[a] | TBD | ps |
| Through_connection | TBD | Ω |
| At Termination[b] | TBD | Ω |
| Differential Skew | TBD | ps |

[a]Within the Exception_window no single impedance excursion shall exceed the Through_Connection-impedance tolerance for a period of twice the TDR rise time specification.
[b]The input impedance at TP3, for the termination, shall be recorded 4.0 ns following the reference location determined by an open connector between TP3 and TP4.

The minimum input amplitude to the receiver listed in Table 54–7 and Figure 54–7 is a worst case specification across all environmental conditions. Restricted environments may allow operation at lower minimum differential voltages, allowing significantly longer operating distances.

NOTE 1—All specifications, unless specifically listed otherwise, are based on differential measurements.

NOTE 2—The receiver minimum differential sensitivity identifies the minimum p-p eye amplitude at TP3 to meet the BER objective.

NOTE 3—Eye diagrams assume the presence of only high-frequency jitter components that are not tracked by the clock recovery circuit. For this standard the lower cutoff frequency for jitter is 637 kHz.

NOTE 4—All times indicated for TDR measurements are recorded times. Recorded times are twice the transit time of the TDR signal.

NOTE 5—Through_Connection impedance describes the impedance tolerance through a mated connector. This tolerance is greater than the termination or cable impedance due to limits in the technology of the connectors.

### 54.7.3 Jitter specifications for 10GBASE-CX4

The 10GBASE-CX4 PMD shall meet the total jitter specifications defined in Table 54–8. Normative values are highlighted **in bold.** All other values are informative. Compliance points are defined in 54.7.

Jitter shall be measured as defined in (TBD paragraph).

Deterministic jitter budgetary specifications are included here to assist implementers in specifying components. Measurements for DJ are described in (TBD paragraph).

**Table 54–8—10GBASE-CX4 jitter budget**

| Compliance point | Total jitter[a] | | Deterministic jitter | |
|---|---|---|---|---|
| | UI | ps | UI | ps |
| **TP1** | **0.240** | **192** | 0.120 | 96 |
| TP1 to TP2 | 0.090 | 72 | 0.020 | 16 |
| **TP2** | **0.279** | **223** | 0.140 | 112 |
| TP2 to TP3 | 0.480 | 384 | 0.260 | 208 |
| **TP3** | **0.660** | **528** | 0.400 | 320 |
| TP3 to TP4 | 0.050 | 40 | 0.050 | 40 |
| **TP4** | **0.710** | **568** | 0.450 | 360 |

[a]Total jitter is composed of both deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter at that point.

## 54.8 PMD to MDI Electrical specifications for 10GBASE-CX4

**NOTE:** These next set of paragraphs come from clause 47.

### 54.8.1 Signal levels

The 10GBASE-CX4 MDI is a low swing AC coupled differential interface. AC coupling allows for interoperability between components operating from different supply voltages. Low swing differential signaling provides noise immunity and improved electromagnetic interference (EMI).

### 54.8.2 Signal paths

The 10GBASE-CX4 MDI signal paths are point-to-point connections. Each path corresponds to a 10GBASE-CX4 MDI lane and is comprised of two complementary signals making a balanced differential pair. There are four differential paths in each direction for a total of eight pairs, or sixteen connections. The signal paths are intended to operate up to approximately 15m over standard TBD cables.

### 54.8.3 Driver characteristics

The 10GBASE-CX4 MDI driver characteristics are summarized in Table 54–9. The 10GBASE-CX4 MDI Baud shall be 3.125 GBaud ±100 ppm. The corresponding Baud period is nominally 320 ps.

**Table 54–9—Driver characteristics**

| Parameter | Value | Units |
|---|---|---|
| Baud rate tolerance | 3.125 GBd ± 100 ppm | GBd ppm |
| Unit interval nominal | 320 | ps |
| Differential amplitude maximum | TBD | $mV_{ppd}$ |
| Absolute output voltage limits<br>maximum<br>minimum | <br>2.3<br>–0.4 | <br>V<br>V |
| Differential output return loss minimum | TBD [See Equation (54-1)] | dB |
| Output jitter<br>Near-end maximums<br>Random jitter<br>Deterministic jitter<br>Total jitter<br>Far-end maximums<br>Random jitter<br>Deterministic jitter<br>Total jitter | <br><br>± TBD peak from the mean<br>± TBD peak from the mean<br><br>± TBD peak from the mean<br>± TBD peak from the mean | <br><br>UI<br>UI<br><br>UI<br>UI |

#### 54.8.3.1 Load

The load is 100 Ω ± 5% differential to 2.5 GHz for these measurements, unless otherwise noted.

### 54.8.3.2 Amplitude and swing

Driver differential output amplitude shall be less than TBD $mV_{p-p}$. DC-referenced logic levels are not defined since the receiver is AC coupled. Absolute driver output voltage shall be between –0.4 V and 2.3 V with respect to ground. See Figure 54–8 for an illustration of absolute driver output voltage limits and definition of differential peak-to-peak amplitude.

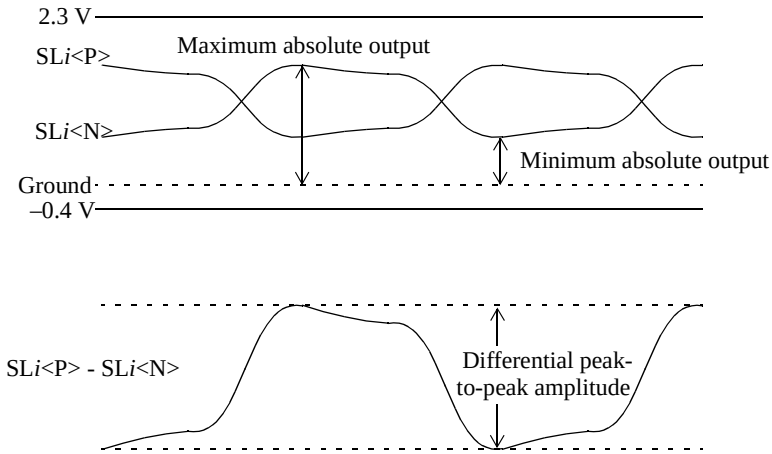



**Figure 54–8—Driver output voltage limits and definitions**
**[L*i*<P> and L*i*<N> are the positive and negative sides of the differential signal pair for Lane *i* (*i* = 0, 1, 2, 3)]**

### 54.8.3.3 Transition time

Differential transition times between 60 and 130 ps are recommended, as measured between the 20% and 80% levels. Shorter transitions may result in excessive high-frequency components and increase EMI and crosstalk. The upper recommended limit of 130 ps corresponds to a sine wave at half the Baud rate.

### 54.8.3.4 Output impedance (TBD)

For frequencies from 312.5 MHz to 3.125 GHz, the differential return loss of the driver shall exceed Equation (54-1). Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 Ω.

$$s_{11} = -10 \text{ dB for } 312.5 \text{ MHz} < \text{Freq } (f) < 625 \text{ MHz, and} \quad (54\text{-}1)$$
$$-10 + 10\log(f/625) \text{ dB for } 625 \text{ MHz} <= \text{Freq } (f) = < 3.125 \text{ GHz}$$

### 54.8.3.5 Driver template and jitter

The driver shall satisfy either the near-end eye template and jitter requirements, or the far-end eye template and jitter requirements. The eye templates are given in Figure 54–9 and Table 54–10. The template measurement requirements are specified in 54.9.2. The jitter requirements at the near end are for a maximum total jitter of ± TBD 0.175 UI peak from the mean and a maximum deterministic component of ± TBD 0.085 UI peak from the mean. The far-end requirements are for a maximum total jitter of ± TBD 0.275 UI peak

from the mean and a maximum deterministic component of ± TBD 0.185 UI peak from the mean. Note that these values assume symmetrical jitter distributions about the mean. If a distribution is not symmetrical, its peak-to-peak total jitter value must be less than these total jitter values to claim compliance to the template requirements per the methods of 54.9.2. Jitter specifications include all but $10^{-12}$ of the jitter population. The maximum random jitter is equal to the maximum total jitter minus the actual deterministic jitter. Jitter measurement requirements are described in 54.9.3.

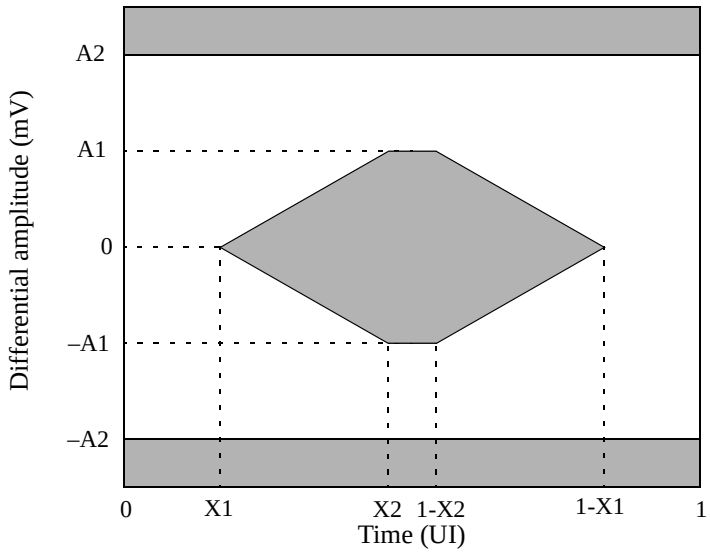



**Figure 54–9—Driver template**

**Table 54–10—Driver template intervals**

| Symbol | Near-end value | Far-end value | Units |
|---|---|---|---|
| X1 | TBD 0.175 | TBD 0.275 | UI |
| X2 | TBD 0.390 | TBD 0.400 | UI |
| A1 | TBD 400 | TBD 100 | mV |
| A2 | TBD 800 | TBD 800 | mV |

### 54.8.4 Receiver characteristics

Receiver characteristics are summarized in Table 54–11 and detailed in the following subclauses.

#### 54.8.4.1 Bit error ratio

The receiver shall operate with a BER of better than $10^{-12}$ in the presence of a reference input signal as defined in 54.8.4.2.

### 54.8.4.2 Reference input signals

Reference input signals to a XAUI receiver have the characteristics determined by compliant XGXSs and XAUI drivers. Reference input signals satisfy the far-end template given in Figure 54–9 and Table 54–10 when the signal source impedance is 100 Ω ±5%. The template measurement requirements are specified in 54.9.2. Note that the input signal might not meet this template when this load is replaced by the actual receiver. Signal jitter does not exceed the jitter tolerance requirements specified in 54.8.4.6.

**Table 54–11—Receiver characteristics**

| Parameter | Value | Units |
|---|---|---|
| Baud rate<br>tolerance | 3.125<br>±100 | GBd<br>ppm |
| Unit interval (UI) nominal | 320 | ps |
| Receiver coupling | AC | |
| Return loss[a]<br>differential<br>common mode | <br>TBD 10<br>TBD 6 | <br>dB<br>dB |
| Jitter amplitude tolerance[b] | TBD 0.65 | $UI_{p-p}$ |

[a]Relative to 100 Ω differential and 25 Ω common mode. See 54.8.4.5 for input impedance details.
[b]See 54.8.4.6 for jitter tolerance details.

### 54.8.4.3 Input signal amplitude

XAUI receivers shall accept differential input signal amplitudes produced by compliant transmitters connected without attenuation to the receiver. Note that this may be larger than the TBD 1600 $mV_{p-p}$ maximum of 54.8.3.2 due to actual driver and receiver input impedances. The minimum input amplitude is defined by the far-end driver template and the actual receiver input impedance. Note that the far-end driver template is defined using a well controlled load impedance. The minimum signal amplitude into an actual receiver may vary from the minimum template height due to the actual receiver input impedance. Since the XAUI receiver is AC coupled to the XAUI, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

### 54.8.4.4 AC coupling

The XAUI receiver shall be AC coupled to the cable assembly to allow for maximum interoperability between various 10 Gbps components. AC coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC coupling in actual implementations.

### 54.8.4.5 Input impedance

Receiver input impedance shall result in a differential return loss better than TBD ~~10~~ dB and a common mode return loss better than TBD ~~6~~ dB from TBD ~~100~~ MHz to TBD ~~2.5~~ GHz. This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ω for differential return loss and 25 Ω for common mode.

#### 54.8.4.6 Jitter tolerance

The XAUI receiver shall have a peak-to-peak total jitter amplitude tolerance of at least TBD ~~0.65~~ UI. This total jitter is composed of three components: deterministic jitter, random jitter, and an additional sinusoidal jitter. Deterministic jitter tolerance shall be at least TBD ~~0.37~~ $UI_{p-p}$. Random jitter tolerance shall be at least TBD ~~0.18~~ $UI_{p-p}$. Tolerance to the sum of deterministic and random jitter shall be at least ~~0.55~~ $UI_{p-p}$. The XAUI receiver shall tolerate an additional sinusoidal jitter with any frequency and amplitude defined by the mask of Figure 54–10. This additional component is intended to ensure margin for low-frequency jitter, wander, noise, crosstalk and other variable system effects. Jitter specifications include all but $10^{-12}$ of the jitter population. Jitter tolerance test requirements are specified in 54.9.3.

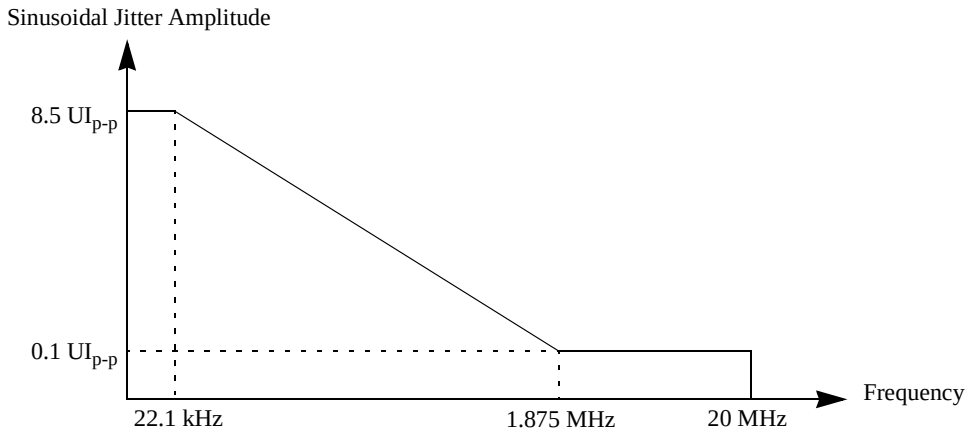



**Figure 54–10—Single-tone sinusoidal jitter mask** (TBD Sinusoidal Jitter Amplitude)

### 54.8.5 Interconnect characteristics

**NOTE:** Put cabling specs here.

The 10GBASE-CX4 is primarily intended as a point-to-point interface of up to approximately 15 m between integrated circuits using controlled impedance cables. Loss and jitter budgets are presented in Table 54–12 to demonstrate the feasibility of standard FR4 epoxy PCBs. The performance of an actual XAUI interconnect is highly dependent on the implementation. The compliance interconnect limit of 54.9.1 represents the median performance of a range of interconnect designs. The range included designs from 46 to 56 cm in total length, having trace widths of 0.125 to 0.300 mm, and using different grades and thicknesses of FR4. Interconnect configurations ranged from single-board designs to systems of two daughter cards mating to a backplane through high-speed electrical connectors.

#### 54.8.5.1 Characteristic impedance

The recommended differential characteristic impedance of circuit board trace pairs is 100 Ω ± 10% from 100 MHz to 2.5 GHz.

#### 54.8.5.2 Connector impedance

The recommended impedance of any connectors, such as used between circuit board subsystems, is 100 Ω ± 30%.

**Table 54–12—Normative 10GBASE-CX4 loss, skew and jitter budget (TBD values)**

| | Loss (dB)[a] | ~~Differential skew ($ps_{p-p}$)~~ | Total jitter ($UI_{p-p}$)[c] | Random jitter ($UI_{p-p}$)[c] | Deterministic jitter ($UI_{p-p}$)[c] |
|---|---|---|---|---|---|
| Driver | 0 | ~~15~~ | 0.35 | 0.18 | 0.17 |
| Interconnect | 7.5 | ~~60~~ | 0.20 | | 0.20 |
| Other[b] | 4.5 | | 0.10 | | 0.10 |
| Total | 12.0 | ~~75~~ | 0.65 | 0.18 | 0.47 |

[a]Budgetary loss in height of eye opening.
[b]Includes such effects as crosstalk, noise, and interaction between jitter and eye height.
[c]Jitter specifications include all but $10^{-12}$ of the jitter population.

## 54.9 Electrical measurement requirements

### 54.9.1 Compliance interconnect definition

**NOTE:** move this paragraph to cable specification section?

The compliance interconnect is a 100 Ω differential system specified with respect to transmission magnitude response and intersymbol interference (ISI) loss. The compliance interconnect limits have been chosen to allow a realistic differential interconnect of about 50 cm length on FR4 epoxy PCB. See 54.8.5 for a more detailed description of the target XAUI interconnect. The transmission magnitude response, $|s_{21}|$, of the compliance interconnect in dB satisfies Equation (54-2).

$$|s_{21}| \le |s_{21}|_{limit} = -20\log(e) \times [a_1\sqrt{f} + a_2 f + a_3 f^2] \quad (54\text{-}2)$$

where $f$ is frequency in Hz, $a_1 = 6.5 \times 10^{-6}$, $a_2 = 2.0 \times 10^{-10}$, and $a_3 = 3.3 \times 10^{-20}$. This limit applies from DC to 3.125 GHz. The magnitude response above 3.125 GHz does not exceed –11.4 dB. The ISI loss, defined as

the difference in magnitude response between two frequencies, is greater than 4.0 dB between 312.5 MHz and 1.5625 GHz. The magnitude response and ISI loss limits are illustrated in Figure 54–11.

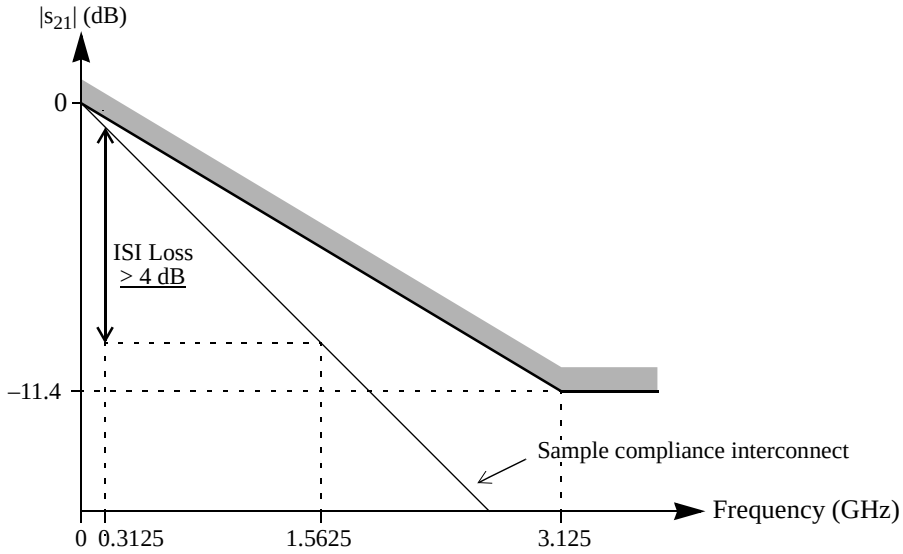



**Figure 54–11—Compliance interconnect magnitude response and ISI loss**

### 54.9.2 Eye template measurements

For the purpose of eye template measurements, the effect of a single-pole high pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. See 48B.1.3 for an explanation of this technique. The data pattern for template measurements is the TBD ~~CJPAT~~ pattern defined in Annex 48A. All 10GBASE-CX4 lanes are active in both the transmit and receive directions, and opposite ends of the link use asynchronous clocks. The amount of data represented in the data eye must be adequate to ensure a bit error ratio of less than $10^{-12}$. The eye template is measured with AC coupling and centered at 0 Volts differential. The left and right edges of the template are aligned with the mean zero crossing points of the measured data eye, as illustrated in Figure 54–12. The near-end load for this test is specified in 54.8.3.1. The far-end template is measured at the end of the compliance interconnect specified in 54.9.1. The far-end load for the compliance link is specified in 54.8.3.1.

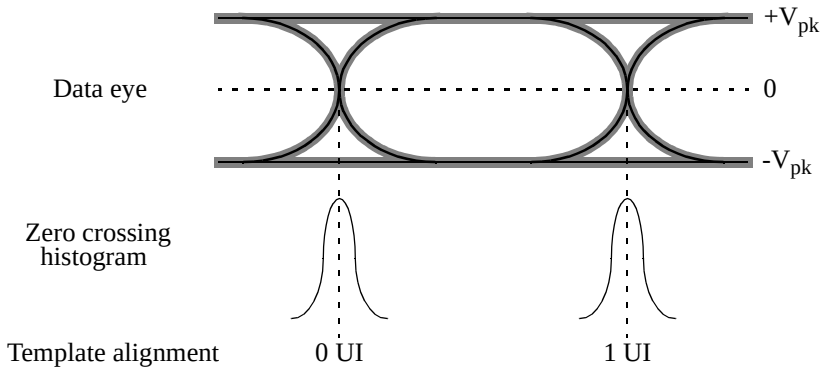



**Figure 54–12—Eye template alignment**

### 54.9.3 Jitter test requirements

For the purpose of jitter measurement, the effect of a single-pole high pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements is the TBD ~~CJPAT~~ pattern defined in Annex 48A. All four lanes of 10GBASE-CX4 are active in both directions, and opposite ends of the link use asynchronous clocks. Jitter is measured with AC coupling and at 0 volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER bathtub curve such as that described in Annex 48B.

#### 54.9.3.1 Transmit jitter

Transmit near-end jitter is measured at the driver output when terminated into the load specified in 54.8.3.1. Far-end jitter is measured at the end of a compliance interconnect specified in 54.9.1. The far-end load for the compliance link is specified in 54.8.3.1.

#### 54.9.3.2 Jitter tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the required sum of deterministic and random jitter defined in 54.8.4.6 and then adjusting the signal amplitude until the data eye contacts the 6 points of the driver's template shown in Figure 54–9 and Table 54–10. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean of the zero crossing. If these symmetries are not achieved, then some portions of the test signal will encroach into the template and provide overstress of the receiver, and/or some points of the template may not be contacted, resulting in understress of the receiver. Eye template measurement requirements are given in 54.9.2. Random jitter is calibrated using a high pass filter with a low-frequency corner of 20 MHz and 20 dB/decade rolloff below this. The required sinusoidal jitter specified in 54.8.4.6 is then added to the signal and the far-end load is replaced by the receiver being tested.

## 54.10 PMA electrical specifications

**NOTE:** These next set of paragraphs come from clause 40.

This subclause defines the electrical characteristics of the PMA.

Common-mode tests use the common-mode return point as a reference.

### 54.10.1 PMA-to-MDI interface tests

#### 54.10.1.1 Isolation requirement (TBD need & values)

The PHY shall provide electrical isolation between the port device circuits, including frame ground (if any) and all MDI leads. This electrical separation shall withstand at least one of the following electrical strength tests:

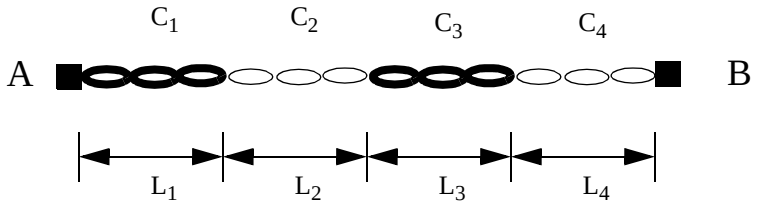
a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC 60950: 1991.
b) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC 60950: 1991.
c) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time or half value), as defined in IEC 60060.

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC 60950: 1991, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

#### 54.10.1.1.1 Test channel

**NOTE:** Imbed test modes into pcs/pma/pmd or require channel to all test waveforms via a data sequence from XGMII to XAUI?

To perform the transmitter MASTER-SLAVE timing jitter tests described in this clause, a test channel is required to ensure that jitter is measured under conditions of poor signal to echo ratio. This test channel shall be constructed by combining 100 and 120 Ω cable segments that both meet or exceed ISO/IEC 11801 Category 5 specifications for each pair, as shown in Figure 54–13, with the lengths and additional restrictions on parameters described in Table 54–13. The ends of the test channel shall be terminated with connectors meeting or exceeding ANSI/TIA/EIA-568-A:1995 or ISO/IEC 11801:1995 Category 5 specifications. The return loss of the resulting test channel shall meet the return loss requirements of <XREF>54.11.2.3 and the crosstalk requirements of <XREF>54.11.3.




Identical for each of the four pairs.

**Figure 54–13—Test channel topology for each cable pair**

**Table 54–13—Test channel cable segment specifications**

| Cable segment | Length (meters) | Characteristic impedance (at frequencies > 1 MHz) | Attenuation (per 100 meters at 31.25 MHz) |
|---|---|---|---|
| 1 | $L_1$=1.20 | 120 ± 5Ω | 7.8 to 8.8 dB |
| 2 | $L_2$=x | 100 ± 5Ω | 10.8 to 11.8 dB |
| 3 | $L_3$=1.48 | 120 ± 5Ω | 7.8 to 8.8 dB |
| 4 | $L_4$=y | 100 ± 5Ω | 10.8 to 11.8 dB |

NOTE—x is chosen so that the total delay of segments C1, C2, and C3, averaged across all pairs, is equal to 570 ns at 31.25 MHz; however, if this would cause the total attenuation of segments C1, C2, and C3, averaged across all pairs, to exceed the worst case insertion loss specified in <XREF>54.11.2.1 then x is chosen so that the total attenuation of segments C1, C2, and C3, averaged across all pairs, does not violate <XREF>54.11.2.1 at any frequencies. The value of y is chosen so that the total attenuation of segments C1, C2, C3, and C4, averaged across all pairs, does not violate <XREF>54.11.2.1 at any frequency (y may be 0).

#### 54.10.1.1.2 Test modes

The test modes described below shall be provided to allow for testing of the transmitter waveform, transmitter distortion, and transmitted jitter.

For a PHY with a GMII interface, these modes shall be enabled by setting bits 9.13:15 (1000BASE-T Control Register) of the GMII Management register set as shown in Table 54–14. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation. PHYs without a GMII shall provide a means to enable these modes for conformance testing.

**Table 54–14—GMII management register settings for test modes**

| Bit 1 (9.15) | Bit 2 (9.14) | Bit 3 (9.13) | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Normal operation |
| 0 | 0 | 1 | Test mode 1—Transmit waveform test |
| 0 | 1 | 0 | Test mode 2—Transmit jitter test in MASTER mode |
| 0 | 1 | 1 | Test mode 3—Transmit jitter test in SLAVE mode |
| 1 | 0 | 0 | Test mode 4—Transmitter distortion test |
| 1 | 0 | 1 | Reserved, operations not identified. |
| 1 | 1 | 0 | Reserved, operations not identified. |
| 1 | 1 | 1 | Reserved, operations not identified. |

When test mode 1 is enabled, the PHY shall transmit the following sequence of data symbols $A_n$, $B_n$, $C_n$, $D_n$, of 40.3.1.3.6 continually from all four transmitters:

{{+2 followed by 127 0 symbols}, {–2 followed by 127 0 symbols},{+1 followed by 127 0 symbols}, {–1 followed by 127 0 symbols}, {128 +2 symbols, 128 –2 symbols, 128 +2 symbols, 128 –2 symbols}, {1024 0 symbols}}

This sequence is repeated continually without breaks between the repetitions when the test mode is enabled. A typical transmitter output is shown in Figure 54–14. The transmitter shall time the transmitted symbols from a 125.00 MHz ± 0.01% clock in the MASTER timing mode.

When test mode 2 is enabled, the PHY shall transmit the data symbol sequence {+2, –2} repeatedly on all channels. The transmitter shall time the transmitted symbols from a 125.00 MHz ± 0.01% clock in the MASTER timing mode.

When test mode 3 is enabled, the PHY shall transmit the data symbol sequence {+2, –2} repeatedly on all channels. The transmitter shall time the transmitted symbols from a 125.00 MHz ± 0.01% clock in the SLAVE timing mode. A typical transmitter output for transmitter test modes 2 and 3 is shown in Figure 54–15.

When test mode 4 is enabled, the PHY shall transmit the sequence of symbols generated by the following scrambler generator polynomial, bit generation, and level mappings:

$$g_{s1} = 1 + x^9 + x^{11}$$

The maximum-length shift register used to generate the sequences defined by this polynomial shall be updated once per symbol interval (8 ns). The bits stored in the shift register delay line at a particular time n are denoted by $Scr_n[10:0]$. At each symbol period the shift register is advanced by one bit and one new bit represented by $Scr_n[0]$ is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive OR'd together to generate the next $Scr_n[0]$ bit. The bit sequences, $x0_n$, $x1_n$, and $x2_n$, generated from combinations of the scrambler bits as shown in the following equations, shall be used to generate the quinary symbols, $s_n$, as shown in Table 54–15. The quinary symbol sequence shall be presented simultaneously to all transmitters. The transmitter shall time the transmitted symbols from a 125.00 MHz ± 0.01% clock in the MASTER timing mode. A typical transmitter output for transmitter test mode 4 is shown in Figure 54–16.

$$x0_n = Scr_n[0]$$

$$x1_n = Scr_n[1] \wedge Scr_n[4]$$

$$x2_n = Scr_n[2] \wedge Scr_n[4]$$

**Table 54–15—Transmitter test mode 4 symbol mapping**

| x2n | x1n | x0n | quinary symbol, $s_n$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | –1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | –2 |
| 1 | 1 | 1 | –1 |

**Figure 53–14—Channel test conditions for conformance test at TP3**

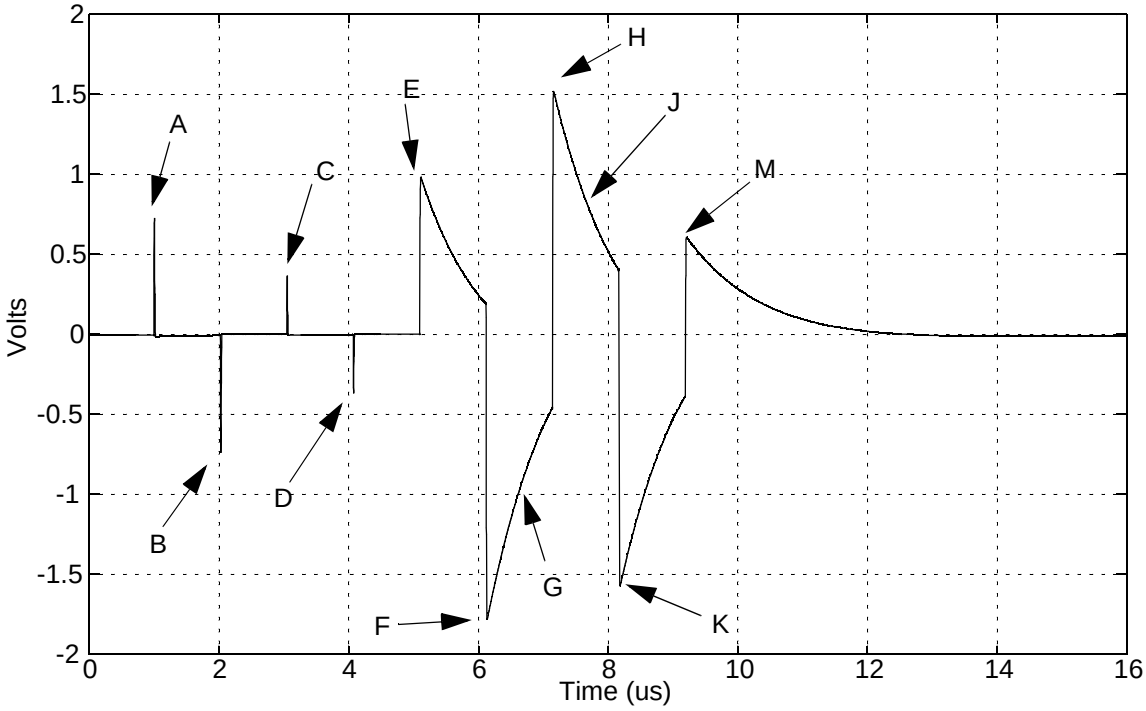



**Figure 54–14—Example of transmitter test mode 1 waveform (1 cycle)**

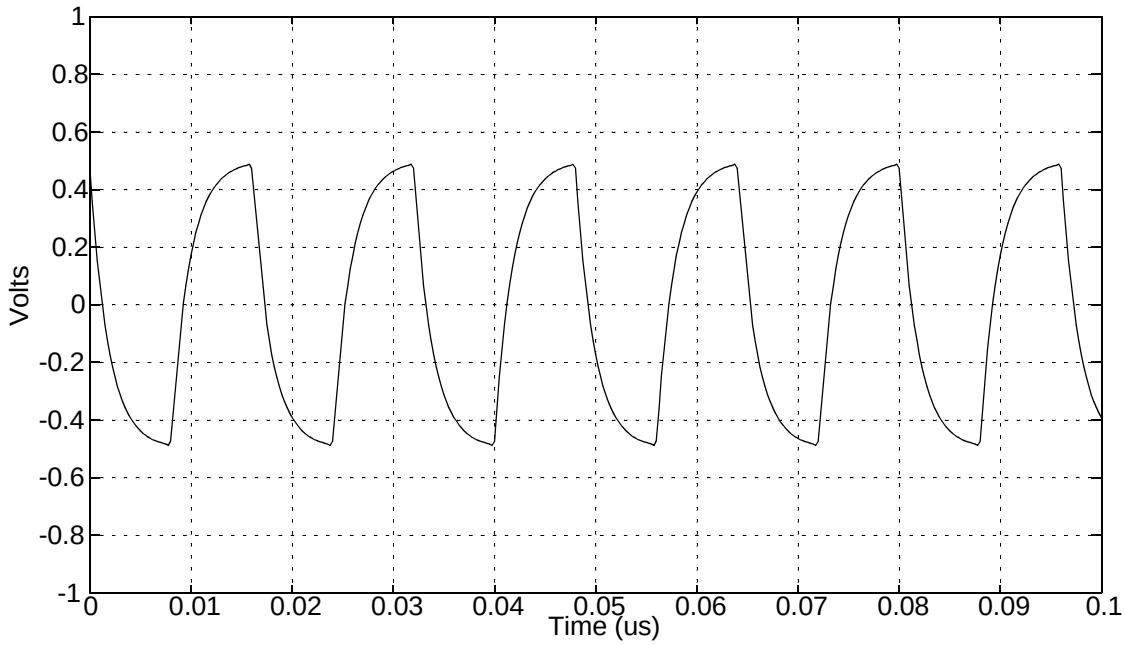



**Figure 54–15—Example of transmitter test modes 2 and 3 waveform**

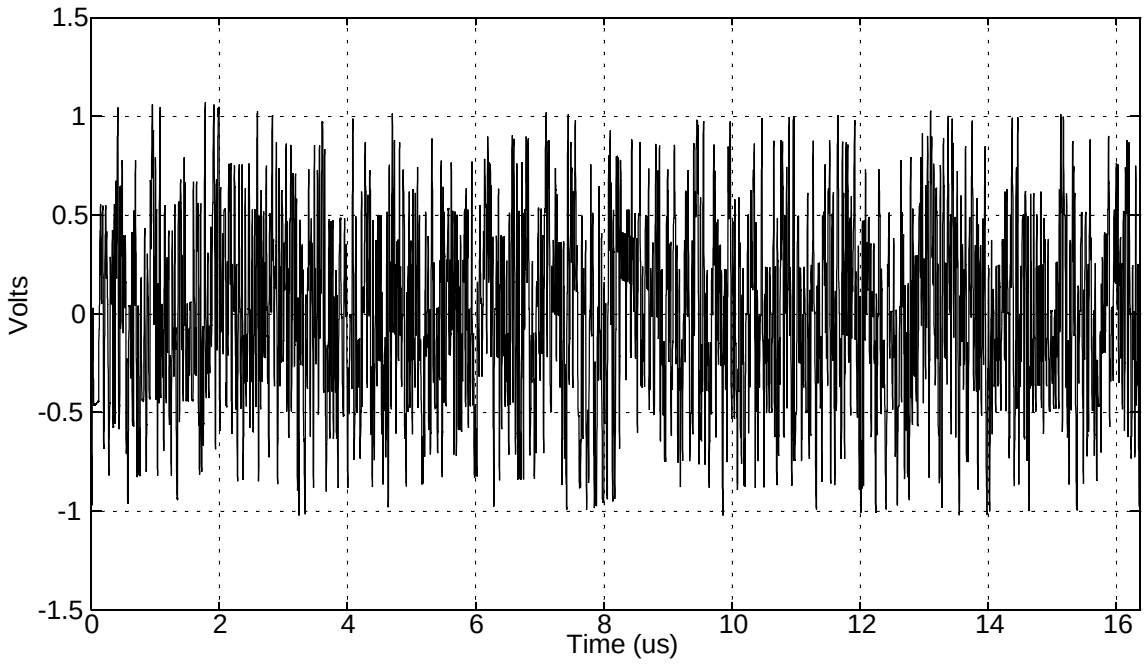



**Figure 54–16—Example of Transmitter Test Mode 4 waveform (1 cycle)**

### 54.10.1.1.3 Test Fixtures

The following fixtures (illustrated by Figure 54–17, Figure 54–18, Figure 54–19, and Figure 54–20), or their functional equivalents, shall be used for measuring the transmitter specifications described in 54.10.1.2.

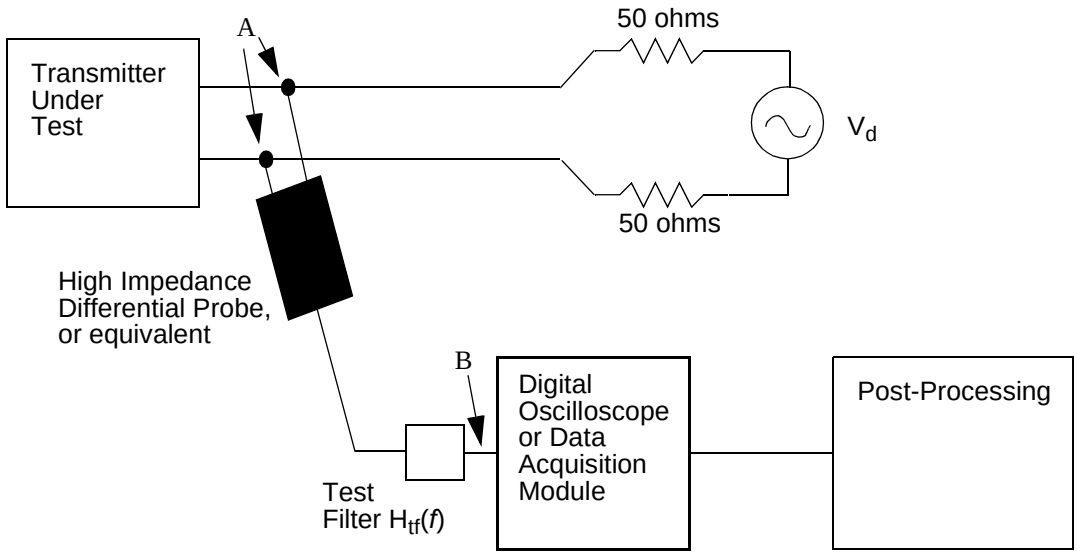



**Figure 54–17—Transmitter test fixture 1 for template measurement**

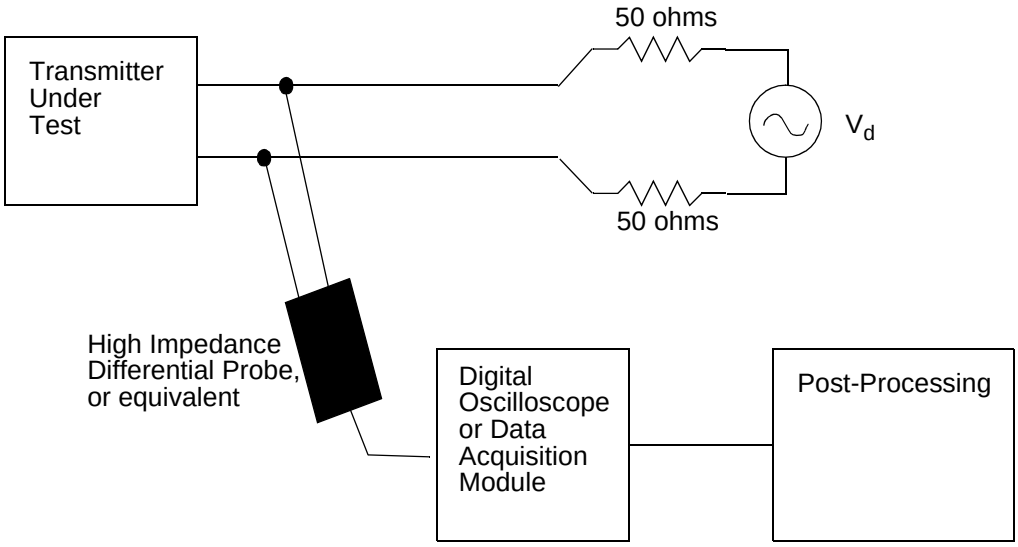



**Figure 54–18—Transmitter test fixture 2 for droop measurement**

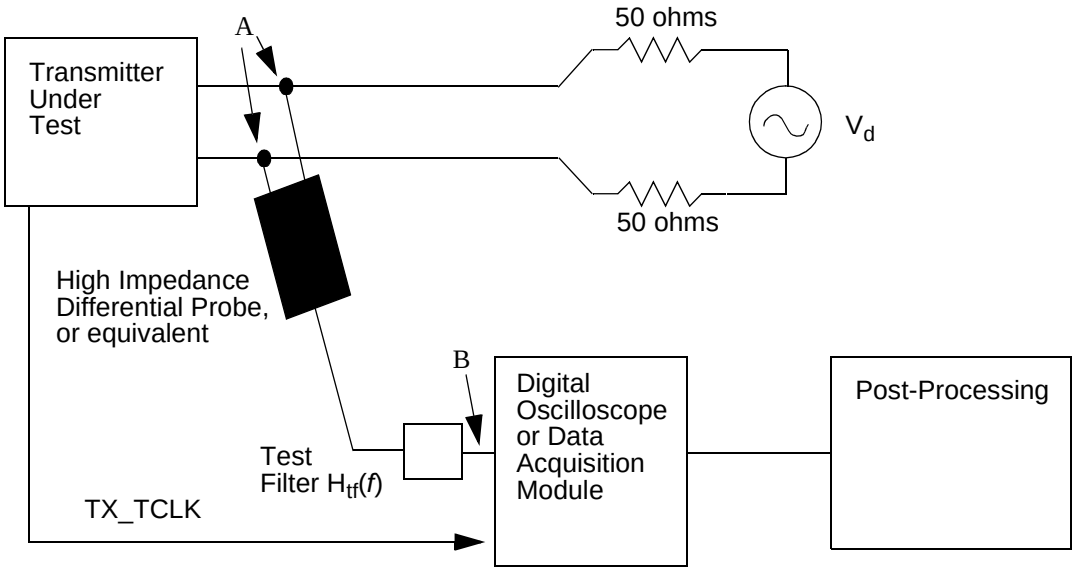



**Figure 54–19—Transmitter test fixture 3 for distortion measurement**

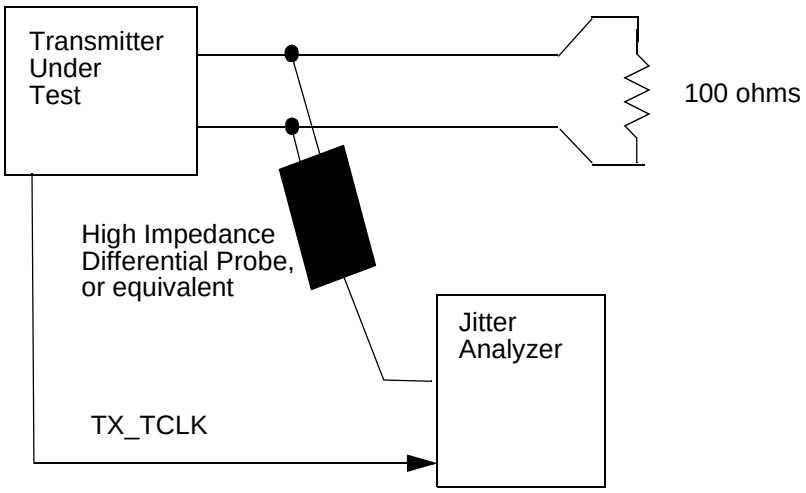



**Figure 54–20—Transmitter test fixture 4 for transmitter jitter measurement**

The test filter, $H_{tf}(f)$, used in transmitter test fixtures 1 and 3 may be located between the points A and B as long as the test filter does not significantly alter the impedance seen by the transmitter. The test filter may instead be implemented as a digital filter in the post processing block. The test filter shall have the following continuous time transfer function or its discrete time equivalent:

$$H_{tf}(f) = \frac{jf}{jf + 2\times10^{6}} \qquad f \text{ in Hz}$$

NOTE—j denotes the square root of –1.

The disturbing signal, $V_d$, shall have the characteristics listed in Table 54–16.

**Table 54–16—$V_d$ Characteristics**

| Characteristic | Transmit test fixture 1 | Transmit test fixture 2 | Transmit test fixture 3 |
|---|---|---|---|
| Waveform | Sine wave | | |
| Amplitude | 2.8 volts peak-to-peak | 2.8 volts peak-to-peak | 5.4 volts peak-to-peak |
| Frequency | 31.25 MHz | 31.25 MHz | 20.833 MHz (125/6 MHz) |
| Purity | All harmonics >40 dB below fundamental | | |

The post-processing block has two roles. The first is to remove the disturbing signal from the measurement. A method of removing the disturbing signal is to take a single shot acquisition of the transmitted signal plus test pattern, then remove the best fit of a sine wave at the fundamental frequency of the disturbing signal from the measurement. It will be necessary to allow the fitting algorithm to adjust the frequency, phase, and amplitude parameters of the sine wave to achieve the best fit.

The second role of the post-processing block is to compare the measured data with the templates, droop specification, or distortion specification.

Trigger averaging of the transmitter output to remove measurement noise and increase measurement resolution is acceptable provided it is done in a manner that does not average out possible distortions caused by the interaction of the transmitter and the disturbing voltage. For transmitter template and droop measurements, averaging can be done by ensuring the disturbing signal is exactly synchronous to the test pattern so that the phase of the disturbing signal at any particular point in the test pattern remains constant. Trigger averaging also requires a triggering event that is synchronous to the test pattern. A trigger pulse generated by the PHY would be ideal for this purpose; however, in practice, triggering off the waveform generated by one of the other transmitter outputs that does not have the disturbing signal present may be possible.

NOTE—The disturbing signal may be made synchronous to the test pattern by creating the disturbing signal using a source of the transmit clock for the PHY under test, dividing it down to the proper frequency for the disturbing signal, passing the result through a high Q bandpass filter to eliminate harmonics and then amplifying the result to the proper amplitude.

The generator of the disturbing signal must have sufficient linearity and range so it does not introduce any appreciable distortion when connected to the transmitter output (see Table 54–16). This may be verified by replacing the transmitter under test with another identical disturbing signal generator having a different frequency output and verifying that the resulting waveform's spectrum does not show significant distortion products.

Additionally, to allow for measurement of transmitted jitter in master and slave modes, the PHY shall provide access to the 125 MHz symbol clock, TX_TCLK, that times the transmitted symbols (see 40.4.2.2). The PHY shall provide a means to enable this clock output if it is not normally enabled.

#### 54.10.1.2 Transmitter electrical specifications

The PMA shall provide the Transmit function specified in 40.4.2.2 in accordance with the electrical specifications of this clause.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output.

The tolerance on the poles of the test filters used in this subclause shall be ±1%.

Practical considerations prevent measurement of the local transmitter performance in the presence of the remotely driven signal in this standard; however, the design of the transmitter to tolerate the presence of the remotely driven signal with acceptable distortion or other changes in performance is a critical issue and must be addressed by the implementor. To this end, a disturbing sine wave is used to simulate the presence of a remote transmitter for a number of the transmitter tests described in the following subordinate subclauses.

##### 54.10.1.2.1 Peak differential output voltage and level accuracy

The absolute value of the peak of the waveform at points A and B, as defined in Figure 54–14, shall fall within the range of 0.67 V to 0.82 V (0.75 V ± 0.83 dB). These measurements are to be made for each pair while operating in test mode 1 and observing the differential signal output at the MDI using transmitter test fixture 1 with no intervening cable.

The absolute value of the peak of the waveforms at points A and B shall differ by less than 1%.

The absolute value of the peak of the waveform at points C and D as defined in Figure 54–14 shall differ by less than 2% from 0.5 times the average of the absolute values of the peaks of the waveform at points A and B.

##### 54.10.1.2.2 Maximum output droop

The magnitude of the negative peak value of the waveform at point G, as defined in Figure 54–14, shall be greater than 73.1% of the magnitude of the negative peak value of the waveform at point F. These measurements are to be made for each pair while in test mode 1 and observing the differential signal output at the MDI using transmit test fixture 2 with no intervening cable. Point G is defined as the point exactly 500 ns after point F. Point F is defined as the point where the waveform reaches its minimum value at the location indicated in Figure 54–14. Additionally, the magnitude of the peak value of the waveform at point J as defined in Figure 54–14 shall be greater than 73.1% of the magnitude of the peak value of the waveform at point H. Point J is defined as the point exactly 500 ns after point H. Point H is defined as the point where the waveform reaches its maximum value at the location indicated in Figure 54–14.

##### 54.10.1.2.3 Differential output templates

The voltage waveforms around points A, B, C, D defined in Figure 54–14, after the normalization described herein, shall lie within the time domain template 1 defined in Figure 54–21 and the piecewise linear interpolation between the points in Table 54–17. These measurements are to be made for each pair while in test mode 1 and while observing the differential signal output at the MDI using transmitter test fixture 1 with no intervening cable. The waveforms may be shifted in time as appropriate to fit within the template.

The waveform around point A is normalized by dividing by the peak value of the waveform at A.

The waveform around point B is normalized by dividing by the negative of the peak value of the waveform at A.

The waveform around point C is normalized by dividing by 1/2 the peak value of the waveform at A.

The waveform around point D is normalized by dividing by the negative of 1/2 the peak value of the waveform at A.

The voltage waveforms around points F and H defined in Figure 54–14, after the normalization described herein, shall lie within the time domain template 2 defined in Figure 54–21 and the piecewise linear interpolation between the points in Table 54–18. These measurements are to be made for each pair while in test mode 1 and while observing the differential signal output at the MDI using transmitter test fixture 1 with no intervening cable. The waveforms may be shifted in time as appropriate to fit within the template.

The waveform around point F is normalized by dividing by the peak value of the waveform at F.

The waveform around point H is normalized by dividing by the peak value of the waveform at H.

NOTE—The templates were created with the following assumptions about the elements in the transmit path:

1) Digital Filter: $0.75 + 0.25\ z^{-1}$
2) Ideal DAC
3) Single pole continuous time low pass filter with pole varying from 70.8 MHz to 117 MHz or linear rise/fall time of 5 ns.
4) Single pole continuous time high-pass filter (transformer high pass) with pole varying from 1 Hz to 100 kHz.
5) Single pole continuous time high-pass filter (test filter) with pole varying from 1.8 MHz to 2.2 MHz.
6) Additionally, +0.025 was added to the upper template and –0.025 was added to the lower template to allow for noise and measurement error.

NOTE—The transmit templates are not intended to address electromagnetic radiation limits.

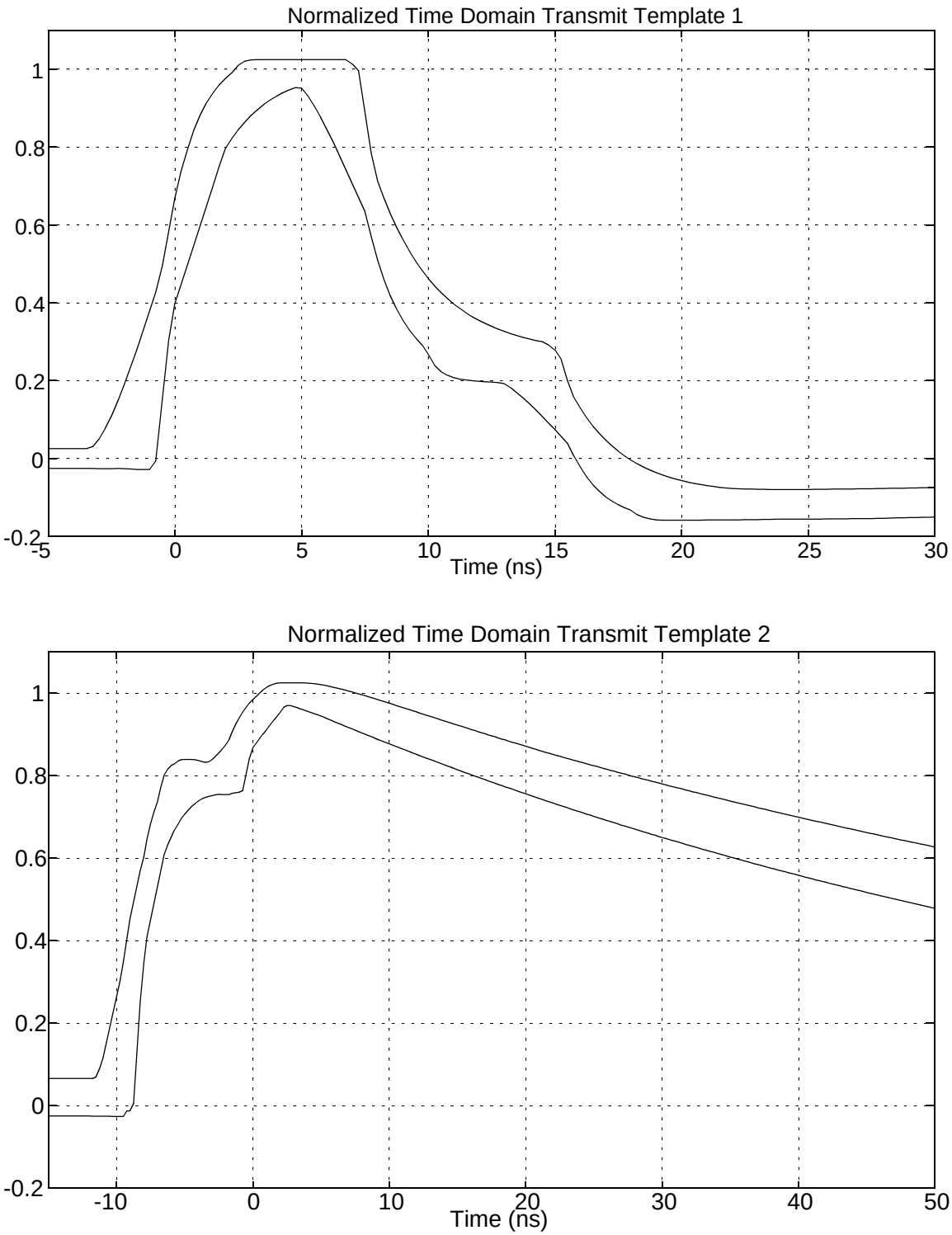



**Figure 54–21—Normalized transmit templates as measured at MDI using transmit test fixture 1**

NOTE—The ASCII for Tables 54–17 and 54–18 is available from http://www.ieee802.org/3/publication/index.html.[18]

**Table 54–17—Normalized time domain voltage template 1**

| Time, ns | Normalized transmit time domain template, upper limit | Normalized transmit time domain template, lower limit | Time, ns | Normalized transmit time domain template, upper limit | Normalized transmit time domain template, lower limit |
|---|---|---|---|---|---|
| –5.00 | 0.025 | –0.026 | 12.75 | 0.332 | 0.195 |
| –4.75 | 0.025 | –0.026 | 13.00 | 0.326 | 0.192 |
| –4.50 | 0.025 | –0.026 | 13.25 | 0.320 | 0.181 |
| –4.25 | 0.025 | –0.026 | 13.50 | 0.315 | 0.169 |
| –4.00 | 0.025 | –0.026 | 13.75 | 0.311 | 0.155 |
| –3.75 | 0.025 | –0.026 | 14.00 | 0.307 | 0.140 |
| –3.50 | 0.025 | –0.026 | 14.25 | 0.303 | 0.124 |
| –3.25 | 0.031 | –0.026 | 14.50 | 0.300 | 0.108 |
| –3.00 | 0.050 | –0.026 | 14.75 | 0.292 | 0.091 |
| –2.75 | 0.077 | –0.026 | 15.00 | 0.278 | 0.074 |
| –2.50 | 0.110 | –0.026 | 15.25 | 0.254 | 0.056 |
| –2.25 | 0.148 | –0.026 | 15.50 | 0.200 | 0.039 |
| –2.00 | 0.190 | –0.027 | 15.75 | 0.157 | 0.006 |
| –1.75 | 0.235 | –0.027 | 16.00 | 0.128 | –0.023 |
| –1.50 | 0.281 | –0.028 | 16.25 | 0.104 | –0.048 |
| –1.25 | 0.329 | –0.028 | 16.50 | 0.083 | –0.068 |
| –1.00 | 0.378 | –0.028 | 16.75 | 0.064 | –0.084 |
| –0.75 | 0.427 | –0.006 | 17.00 | 0.047 | –0.098 |
| –0.50 | 0.496 | 0.152 | 17.25 | 0.032 | –0.110 |
| –0.25 | 0.584 | 0.304 | 17.50 | 0.019 | –0.119 |
| 0.00 | 0.669 | 0.398 | 17.75 | 0.007 | –0.127 |
| 0.25 | 0.739 | 0.448 | 18.00 | –0.004 | –0.133 |
| 0.50 | 0.796 | 0.499 | 18.25 | –0.014 | –0.145 |
| 0.75 | 0.844 | 0.550 | 18.50 | –0.022 | –0.152 |
| 1.00 | 0.882 | 0.601 | 18.75 | –0.030 | –0.156 |
| 1.25 | 0.914 | 0.651 | 19.00 | –0.037 | –0.158 |
| 1.50 | 0.940 | 0.701 | 19.25 | –0.043 | –0.159 |

[18]*Copyright release for 802.3® template data:* Users of this standard may freely reproduce the template data in this subclause so it can be used for its intended purpose.

**Table 54–17—Normalized time domain voltage template 1 *(continued)***

| Time, ns | Normalized transmit time domain template, upper limit | Normalized transmit time domain template, lower limit | Time, ns | Normalized transmit time domain template, upper limit | Normalized transmit time domain template, lower limit |
|---|---|---|---|---|---|
| 1.75 | 0.960 | 0.751 | 19.50 | –0.048 | –0.159 |
| 2.00 | 0.977 | 0.797 | 19.75 | –0.053 | –0.159 |
| 2.25 | 0.992 | 0.822 | 20.00 | –0.057 | –0.159 |
| 2.50 | 1.010 | 0.845 | 20.25 | –0.061 | –0.159 |
| 2.75 | 1.020 | 0.864 | 20.50 | –0.064 | –0.159 |
| 3.00 | 1.024 | 0.881 | 20.75 | –0.067 | –0.159 |
| 3.25 | 1.025 | 0.896 | 21.00 | –0.070 | –0.159 |
| 3.50 | 1.025 | 0.909 | 21.25 | –0.072 | –0.159 |
| 3.75 | 1.025 | 0.921 | 21.50 | –0.074 | –0.158 |
| 4.00 | 1.025 | 0.931 | 21.75 | –0.076 | –0.158 |
| 4.25 | 1.025 | 0.939 | 22.00 | –0.077 | –0.158 |
| 4.50 | 1.025 | 0.946 | 22.25 | –0.078 | –0.158 |
| 4.75 | 1.025 | 0.953 | 22.50 | –0.079 | –0.158 |
| 5.00 | 1.025 | 0.951 | 22.75 | –0.079 | –0.157 |
| 5.25 | 1.025 | 0.931 | 23.00 | –0.079 | –0.157 |
| 5.50 | 1.025 | 0.905 | 23.25 | –0.080 | –0.157 |
| 5.75 | 1.025 | 0.877 | 23.50 | –0.080 | –0.157 |
| 6.00 | 1.025 | 0.846 | 23.75 | –0.080 | –0.156 |
| 6.25 | 1.025 | 0.813 | 24.00 | –0.080 | –0.156 |
| 6.50 | 1.025 | 0.779 | 24.25 | –0.080 | –0.156 |
| 6.75 | 1.025 | 0.743 | 24.50 | –0.080 | –0.156 |
| 7.00 | 1.014 | 0.707 | 24.75 | –0.080 | –0.156 |
| 7.25 | 0.996 | 0.671 | 25.00 | –0.080 | –0.156 |
| 7.50 | 0.888 | 0.634 | 25.25 | –0.080 | –0.156 |
| 7.75 | 0.784 | 0.570 | 25.50 | –0.080 | –0.156 |
| 8.00 | 0.714 | 0.510 | 25.75 | –0.079 | –0.156 |
| 8.25 | 0.669 | 0.460 | 26.00 | –0.079 | –0.156 |
| 8.50 | 0.629 | 0.418 | 26.25 | –0.079 | –0.156 |
| 8.75 | 0.593 | 0.383 | 26.50 | –0.079 | –0.155 |

**Table 54–17—Normalized time domain voltage template 1 *(continued)***

| Time, ns | Normalized transmit time domain template, upper limit | Normalized transmit time domain template, lower limit | Time, ns | Normalized transmit time domain template, upper limit | Normalized transmit time domain template, lower limit |
|---|---|---|---|---|---|
| 9.00 | 0.561 | 0.354 | 26.75 | –0.079 | –0.155 |
| 9.25 | 0.533 | 0.330 | 27.00 | –0.078 | –0.155 |
| 9.50 | 0.507 | 0.309 | 27.25 | –0.078 | –0.155 |
| 9.75 | 0.483 | 0.292 | 27.50 | –0.078 | –0.154 |
| 10.00 | 0.462 | 0.268 | 27.75 | –0.078 | –0.154 |
| 10.25 | 0.443 | 0.239 | 28.00 | –0.077 | –0.154 |
| 10.50 | 0.427 | 0.223 | 28.25 | –0.077 | –0.153 |
| 10.75 | 0.411 | 0.213 | 28.50 | –0.077 | –0.153 |
| 11.00 | 0.398 | 0.208 | 28.75 | –0.076 | –0.153 |
| 11.25 | 0.385 | 0.204 | 29.00 | –0.076 | –0.152 |
| 11.50 | 0.374 | 0.201 | 29.25 | –0.076 | –0.152 |
| 11.75 | 0.364 | 0.199 | 29.50 | –0.076 | –0.152 |
| 12.00 | 0.355 | 0.198 | 29.75 | –0.075 | –0.151 |
| 12.25 | 0.346 | 0.197 | 30.00 | –0.075 | –0.151 |
| 12.50 | 0.339 | 0.196 | | | |

**Table 54–18—Normalized time domain voltage template 2**

| Time, ns | Normalized transmit time domain template, upper limit | Normalized transmit time domain template, lower limit | Time, ns | Normalized transmit time domain template, upper limit | Normalized transmit time domain template, lower limit |
|---|---|---|---|---|---|
| –15.00 | 0.066 | –0.025 | 18.00 | 0.891 | 0.779 |
| –14.50 | 0.066 | –0.025 | 18.50 | 0.886 | 0.773 |
| –14.00 | 0.066 | –0.025 | 19.00 | 0.881 | 0.767 |
| –13.50 | 0.066 | –0.025 | 19.50 | 0.876 | 0.762 |
| –13.00 | 0.066 | –0.025 | 20.00 | 0.871 | 0.756 |
| –12.50 | 0.066 | –0.025 | 20.50 | 0.866 | 0.750 |
| –12.00 | 0.066 | –0.025 | 21.00 | 0.861 | 0.745 |
| –11.50 | 0.069 | –0.025 | 21.50 | 0.856 | 0.739 |
| –11.00 | 0.116 | –0.025 | 22.00 | 0.852 | 0.734 |
| –10.50 | 0.183 | –0.025 | 22.50 | 0.847 | 0.728 |

**Table 54–18—Normalized time domain voltage template 2 *(continued)***

| Time, ns | Normalized transmit time domain template, upper limit | Normalized transmit time domain template, lower limit | Time, ns | Normalized transmit time domain template, upper limit | Normalized transmit time domain template, lower limit |
|---|---|---|---|---|---|
| –10.00 | 0.261 | –0.027 | 23.00 | 0.842 | 0.723 |
| –9.50 | 0.348 | –0.027 | 23.50 | 0.838 | 0.717 |
| –9.00 | 0.452 | –0.013 | 24.00 | 0.833 | 0.712 |
| –8.50 | 0.535 | 0.130 | 24.50 | 0.828 | 0.707 |
| –8.00 | 0.604 | 0.347 | 25.00 | 0.824 | 0.701 |
| –7.50 | 0.683 | 0.451 | 25.50 | 0.819 | 0.696 |
| –7.00 | 0.737 | 0.531 | 26.00 | 0.815 | 0.691 |
| –6.50 | 0.802 | 0.610 | 26.50 | 0.811 | 0.686 |
| –6.00 | 0.825 | 0.651 | 27.00 | 0.806 | 0.680 |
| –5.50 | 0.836 | 0.683 | 27.50 | 0.802 | 0.675 |
| –5.00 | 0.839 | 0.707 | 28.00 | 0.797 | 0.670 |
| –4.50 | 0.839 | 0.725 | 28.50 | 0.793 | 0.665 |
| –4.00 | 0.837 | 0.739 | 29.00 | 0.789 | 0.660 |
| –3.50 | 0.832 | 0.747 | 29.50 | 0.784 | 0.655 |
| –3.00 | 0.839 | 0.752 | 30.00 | 0.780 | 0.650 |
| –2.50 | 0.856 | 0.755 | 30.50 | 0.776 | 0.645 |
| –2.00 | 0.875 | 0.755 | 31.00 | 0.772 | 0.641 |
| –1.50 | 0.907 | 0.758 | 31.50 | 0.767 | 0.636 |
| –1.00 | 0.941 | 0.760 | 32.00 | 0.763 | 0.631 |
| –0.50 | 0.966 | 0.803 | 32.50 | 0.759 | 0.626 |
| 0.00 | 0.986 | 0.869 | 33.00 | 0.755 | 0.621 |
| 0.50 | 1.001 | 0.890 | 33.50 | 0.751 | 0.617 |
| 1.00 | 1.014 | 0.912 | 34.00 | 0.747 | 0.612 |
| 1.50 | 1.022 | 0.933 | 34.50 | 0.743 | 0.607 |
| 2.00 | 1.025 | 0.954 | 35.00 | 0.739 | 0.603 |
| 2.50 | 1.025 | 0.970 | 35.50 | 0.734 | 0.598 |
| 3.00 | 1.025 | 0.967 | 36.00 | 0.730 | 0.594 |
| 3.50 | 1.025 | 0.962 | 36.50 | 0.727 | 0.589 |
| 4.00 | 1.025 | 0.956 | 37.00 | 0.723 | 0.585 |

**Table 54–18—Normalized time domain voltage template 2 *(continued)***

| Time, ns | Normalized transmit time domain template, upper limit | Normalized transmit time domain template, lower limit | Time, ns | Normalized transmit time domain template, upper limit | Normalized transmit time domain template, lower limit |
|---|---|---|---|---|---|
| 4.50 | 1.023 | 0.950 | 37.50 | 0.719 | 0.580 |
| 5.00 | 1.020 | 0.944 | 38.00 | 0.715 | 0.576 |
| 5.50 | 1.017 | 0.937 | 38.50 | 0.711 | 0.571 |
| 6.00 | 1.014 | 0.931 | 39.00 | 0.707 | 0.567 |
| 6.50 | 1.010 | 0.924 | 39.50 | 0.703 | 0.563 |
| 7.00 | 1.005 | 0.917 | 40.00 | 0.699 | 0.558 |
| 7.50 | 1.001 | 0.910 | 40.50 | 0.695 | 0.554 |
| 8.00 | 0.996 | 0.903 | 41.00 | 0.692 | 0.550 |
| 8.50 | 0.991 | 0.897 | 41.50 | 0.688 | 0.546 |
| 9.00 | 0.986 | 0.890 | 42.00 | 0.684 | 0.541 |
| 9.50 | 0.981 | 0.884 | 42.50 | 0.680 | 0.537 |
| 10.00 | 0.976 | 0.877 | 43.00 | 0.677 | 0.533 |
| 10.50 | 0.970 | 0.871 | 43.50 | 0.673 | 0.529 |
| 11.00 | 0.965 | 0.864 | 44.00 | 0.669 | 0.525 |
| 11.50 | 0.960 | 0.858 | 44.50 | 0.666 | 0.521 |
| 12.00 | 0.954 | 0.852 | 45.00 | 0.662 | 0.517 |
| 12.50 | 0.949 | 0.845 | 45.50 | 0.659 | 0.513 |
| 13.00 | 0.944 | 0.839 | 46.00 | 0.655 | 0.509 |
| 13.50 | 0.938 | 0.833 | 46.50 | 0.651 | 0.505 |
| 14.00 | 0.933 | 0.827 | 47.00 | 0.648 | 0.501 |
| 14.50 | 0.928 | 0.820 | 47.50 | 0.644 | 0.497 |
| 15.00 | 0.923 | 0.814 | 48.00 | 0.641 | 0.493 |
| 15.50 | 0.917 | 0.808 | 48.50 | 0.637 | 0.490 |
| 16.00 | 0.912 | 0.802 | 49.00 | 0.634 | 0.486 |
| 16.50 | 0.907 | 0.796 | 49.50 | 0.631 | 0.482 |
| 17.00 | 0.902 | 0.791 | 50.00 | 0.627 | 0.478 |
| 17.50 | 0.897 | 0.785 | | | |

#### 54.10.1.2.4 Transmitter distortion

When in test mode 4 and observing the differential signal output at the MDI using transmitter test fixture 3, for each pair, with no intervening cable, the peak distortion as defined below shall be less than 10 mV.

The peak distortion is determined by sampling the differential signal output with the symbol rate TX_TCLK at an arbitrary phase and processing a block of any 2047 consecutive samples with the MATLAB (see 1.3) code listed below or equivalent. Note that this code assumes that the differential signal has already been filtered by the test filter.

NOTE—The ASCII for the following MATLAB code is available from http://www.ieee802.org/3/publication/index.html.[19]

MATLAB code for Distortion Post Processing is as follows:

```
%
% Distortion Specification Post Processing
%

% Initialize Variables
clear
symbolRate=125e6;                                % symbol rate
dataFile=input('Data file name: ','s')

% Generate test pattern symbol sequence

scramblerSequence=ones(1,2047);
for i=12:2047
  scramblerSequence(i)=mod(scramblerSequence(i-11) + scramblerSequence(i-9),2);
end

for i=1:2047
  temp=scramblerSequence(mod(i-1,2047)+1) + ...
           2*mod(scramblerSequence(mod(i-2,2047)+1)  +  scramblerSequence(mod(i-
5,2047)+1),2) + ...
           4*mod(scramblerSequence(mod(i-3,2047)+1)  +  scramblerSequence(mod(i-
5,2047)+1),2);
  switch temp
    case 0,
      testPattern(i)=0;
    case 1,
      testPattern(i)=1;
    case 2,
      testPattern(i)=2;
    case 3,
      testPattern(i)=-1;
    case 4,
      testPattern(i)=0;
    case 5,
      testPattern(i)=1;
    case 6,
      testPattern(i)=-2;
    case 7,
      testPattern(i)=-1;
  end
end



% Input data file
fid=fopen(dataFile,'r');
```

[19]*Copyright release for MATLAB code*: Users of this standard may freely reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

```
sampledData=fscanf(fid,'%f');
fclose(fid);
sampledData=sampledData.';


if (length(sampledData) < 2047)
  error('Must have 2047 consecutive samples for processing');
elseif (length(sampledData) > 2047)
  fprintf(1,'\n Warning - only using first 2047 samples in data file');
  sampledData=sampledData(1:2047);
end


% Fit a sine wave to the data and temporarily remove it to yield processed data

options=foptions;
options(1)=0;
options(2)=1e-8;
options(3)=1e-8;
options(14)=2000;
gradfun=zeros(0);
P=fmins('sinefit',[2.0 0 125/6.],options,gradfun,sampledData,symbolRate);

P

processedData=sampledData - ...
    P(1)*sin(2*pi*(P(3)*1e6*[0:2046]/symbolRate + P(2)*1e-9*symbolRate));



% LMS Canceller

numberCoeff=70;  % Number of coefficients in canceller
coefficients=zeros(1,numberCoeff);
delayLine=testPattern;

% Align data in delayLine to sampled data pattern
temp=xcorr(processedData,delayLine);
index=find(abs(temp)==max(abs(temp)));
index=mod(mod(length(processedData) - index(1),2047)+numberCoeff-10,2047);
delayLine=[delayLine((end-index):end) delayLine(1:(end-index-1))];


% Compute coefficients that minimize squared error in cyclic block

for i=1:2047
  X(i,:)=delayLine(mod([0:(numberCoeff-1)]+i-1,2047)+1);
end
coefficients=(inv(X.' * X)*(processedData*X).').';



% Canceller
for i=1:2047
       err(i)=processedData(i)    -    sum(delayLine(1+mod((i-1):(i+numberCoeff-
2),2047)).*coefficients);
end

% Add back temporarily removed sine wave

err=err+P(1)*sin(2*pi*(P(3)*1e6*[0:2046]./symbolRate + P(2)*1e-9*symbolRate));


% Re-fit sine wave and do a final removal
```

```
options=foptions;
options(1)=0;
options(2)=1e-12;
options(3)=1e-12;
options(14)=10000;
gradfun=zeros(0);
P=fmins('sinefit',[2.0 0 125/6.],options,gradfun,err,symbolRate);

P

processedData=sampledData - ...
    P(1)*sin(2*pi*(P(3)*1e6*[0:2046]/symbolRate + P(2)*1e-9*symbolRate));


% Compute coefficients that minimize squared error in cyclic block

coefficients=(inv(X.' * X)*(processedData*X).').';



% Canceller
for i=1:2047
       err(i)=processedData(i)    -    sum(delayLine(1+mod((i-1):(i+numberCoeff-
2),2047)).*coefficients);
end

% SNR Calculation
signal=0.5;
noise=mean(err.^2);

SNR=10*log10(signal./noise);

% Output Peak Distortion

peakDistortion=max(abs(err))


% Function for fitting sine wave
function err=sinefit(parameters,data,symbolRate)
err=sum((data- ...
     parameters(1)*sin(2*pi*(parameters(3)*1e6*[0:(length(data)-1)]/symbolRate +
parameters(2)*1e-9*symbolRate))).^2);
```

#### 54.10.1.2.5 Transmitter timing jitter

When in test mode 2 or test mode 3, the peak-to-peak jitter $J_{txout}$ of the zero crossings of the differential signal output at the MDI relative to the corresponding edge of TX_TCLK is measured. The corresponding edge of TX_TCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured.

When in the normal mode of operation as the MASTER, the peak-to-peak value of the MASTER TX_TCLK jitter relative to an unjittered reference shall be less than 1.4 ns. When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf1}(f)$, having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus $J_{txout}$ shall be less than 0.3 ns.

$$H_{jf1}(f) = \frac{jf}{jf + 5000} \qquad f \text{ in Hz}$$

When in the normal mode of operation as the SLAVE, receiving valid signals from a compliant PHY operating as the MASTER using the test channel defined in <XREF>54.10.1.1.1, with test channel port A connected to the SLAVE, the peak-to-peak value of the SLAVE TX_TCLK jitter relative to the MASTER TX_TCLK shall be less than 1.4 ns after the receiver is properly receiving the data and has set bit 10.13 of

the GMII management register set to 1. When the jitter waveform on TX_TCLK is filtered by a high-pass filter, $H_{jf2}(f)$, having the transfer function below, the peak-to-peak value of the resulting filtered timing jitter plus $J_{txout}$ shall be no more than 0.4 ns greater than the simultaneously measured peak-to-peak value of the MASTER jitter filtered by $H_{jf1}(f)$.

$$H_{jf2}(f) = \frac{jf}{jf + 32000} \qquad f \text{ in Hz}$$

NOTE—j denotes the square root of –1.

For all high-pass filtered jitter measurements, the peak-to-peak value shall be measured over an unbiased sample of at least $10^5$ clock edges. For all unfiltered jitter measurements, the peak-to-peak value shall be measured over an interval of not less than 100 ms and not more than 1 second.

#### 54.10.1.2.6 Transmit clock frequency

The quinary symbol transmission rate on each pair of the master PHY shall be 125.00 MHz ± 0.01%.

### 54.10.1.3 Receiver electrical specifications

The PMA shall provide the Receive function specified in 40.4.2.3 in accordance with the electrical specifications of this clause. The patch cabling and interconnecting hardware used in test configurations shall be within the limits specified in <XREF>54.11.

#### 54.10.1.3.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of <XREF>54.10.1.2 and have passed through a link specified in <XREF>54.11 are translated into one of the PMA_UNITDATA.indicate messages with a 4-D symbol error rate less than $10^{-10}$ and sent to the PCS after link reset completion. Since the 4-D symbols are not accessible, this specification shall be satisfied by a frame error rate less than $10^{-7}$ for 125 octet frames.

#### 54.10.1.3.2 Receiver frequency tolerance

The receive feature shall properly receive incoming data with a 5-level symbol rate within the range 125.00 MHz ± 0.01%.

#### 54.10.1.3.3 Common-mode noise rejection

This specification is provided to limit the sensitivity of the PMA receiver to common-mode noise from the cabling system. Common-mode noise generally results when the cabling system is subjected to electromagnetic fields. Figure 54–22 shows the test configuration, which uses a capacitive cable clamp, that injects common-mode signals into a cabling system.

A 100-meter, 4-pair Category 5 cable that meets the specification of <XREF>54.11 is connected between two 1000BASE-T PHYs and inserted into the cable clamp. The cable should be terminated on each end with an MDI connector plug specified in 40.8.1. The clamp should be located a distance of ~20 cm from the receiver. It is recommended that the cable between the transmitter and the cable clamp be installed either in a linear run or wrapped randomly on a cable rack. The cable rack should be at least 3 m from the cable clamp. In addition, the cable clamp and 1000BASE-T receiver should be placed on a common copper ground plane and the ground of the receiver should be in contact with the ground plane. The chassis grounds of all test equipment used should be connected to the copper ground plane. No connection is required between the copper ground plane and an external reference. A description of the cable clamp, as well as the validation procedure, can be found in Annex 40B.

A signal generator with a 50 Ω impedance is connected to one end of the clamp and an oscilloscope with a 50 Ω input is connected to the other end of the clamp. The signal generator shall be capable of providing a sine wave signal of 1 MHz to 250 MHz. The output of the signal generator is adjusted for a voltage of 1.0 Vrms (1.414 Vpeak) on the oscilloscope.

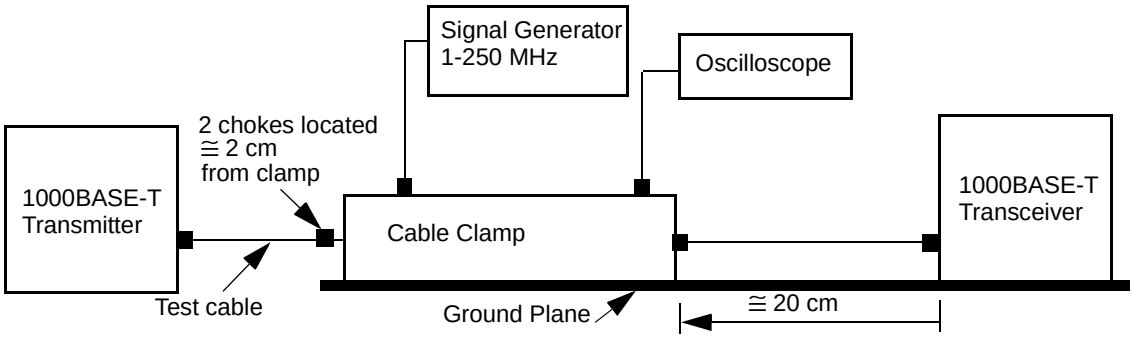



**Figure 54–22—Receiver common-mode noise rejection test**

While sending data from the transmitter, the receiver shall send the proper PMA_UNITDATA.indicate messages to the PCS as the signal generator frequency is varied from 1 MHz to 250 MHz.

NOTE—Although the signal specification is constrained within the 1–100 MHz band, this test is performed up to 250 MHz to ensure the receiver under test can tolerate out-of-band (100–250 MHz) noise.

### 54.10.1.3.4 Alien Crosstalk noise rejection

While receiving data from a transmitter specified in 54.10.1.2 through a link segment specified in <XREF>54.11 connected to all MDI duplex channels, a receiver shall send the proper PMA_UNITDATA.indicate message to the PCS when any one of the four pairs is connected to a noise source as described in Figure 54–23. Because symbol encoding is employed, this specification shall be satisfied by a frame error rate of less than $10^{-7}$ for 125 octet frames. The level of the noise signal at the MDI is nominally 25 mV peak-to-peak. (Measurements are to be made on each of the four pairs.) The noise source shall be connected to one of the MDI inputs using Category 5 balanced cable of a maximum length of 0.5 m.

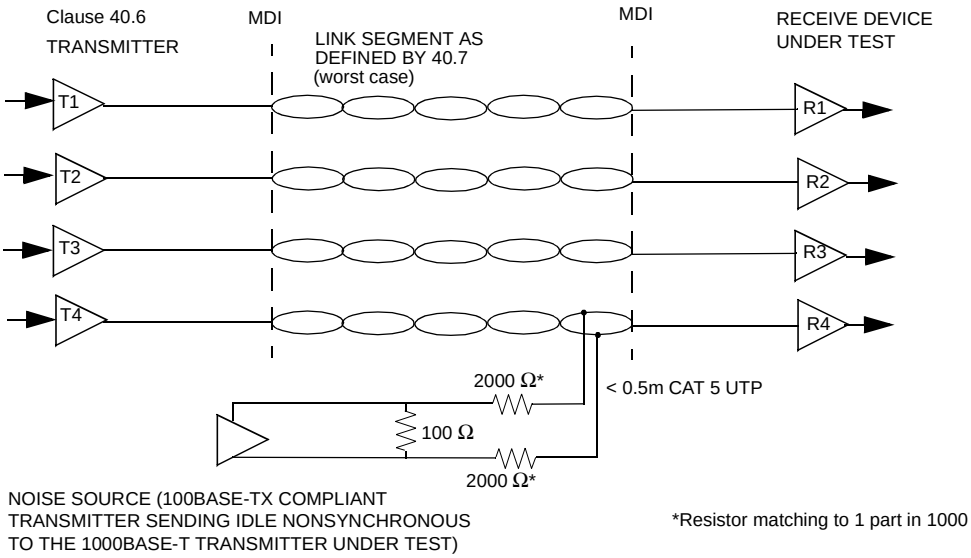



**Figure 54–23—Differential mode noise rejection test**

## 54.11 Link segment characteristics

1000BASE-T is designed to operate over a 4-pair Category 5 balanced cabling system. Each of the four pairs supports an effective data rate of 250 Mbps in each direction simultaneously. The term “link segment” used in this clause refers to four duplex channels. The term “duplex channel” will be used to refer to a single channel with full duplex capability. Specifications for a link segment apply equally to each of the four duplex channels. All implementations of the balanced cabling link shall be compatible at the MDI.

### 54.11.1 Cabling system characteristics

The cabling system used to support 1000BASE-T requires 4 pairs of Category 5 balanced cabling with a nominal impedance of 100 Ω. The cabling system components (cables, cords, and connectors) used to provide the link segment shall consist of Category 5 components as specified in ANSI/TIA/EIA-568-A:1995 and ISO/IEC 11801:1995. Additionally:

a) 1000BASE-T uses a star topology with Category 5 balanced cabling used to connect PHY entities.
b) 1000BASE-T is an ISO/IEC 11801 Class D application, with additional installation requirements and transmission parameters specified in Annex 40A.
c) The width of the PMD transmit signal spectrum is approximately 80 MHz.
d) The use of shielding is outside the scope of this standard.

### 54.11.2 Link transmission parameters

The transmission parameters contained in this subclause are specified to ensure that a Category 5 link segment of up to at least 100 m will provide a reliable medium. The transmission parameters of the link segment include insertion loss, delay parameters, characteristic impedance, NEXT loss, ELFEXT loss, and return loss.

Link segment testing shall be conducted using source and load impedances of 100 Ω. The tolerance on the poles of the test filter used in this subclause shall be no worse than 1%.

#### 54.11.2.1 Insertion loss

The insertion loss of each duplex channel shall be less than

$$\text{Insertion\_Loss}(f) < 2.1\, f^{0.529} + 0.4/f \quad \text{(dB)}$$

at all frequencies from 1 MHz to 100 MHz. This includes the attenuation of the balanced cabling pairs, including work area and equipment cables plus connector losses within each duplex channel. The insertion loss specification shall be met when the duplex channel is terminated in 100 Ω.

NOTE—The above equation approximates the insertion loss specification at discrete frequencies for Category 5 100-meter links specified in ANSI/TIA/EIA-568-A Annex E and in TIA/EIA TSB 67.

#### 54.11.2.2 Differential characteristic impedance

The nominal differential characteristic impedance of each link segment duplex channel, which includes cable cords and connecting hardware, is 100 Ω for all frequencies between 1 MHz and 100 MHz.

#### 54.11.2.3 Return loss

Each link segment duplex channel shall meet or exceed the return loss specified in the following equation at all frequencies from 1 MHz to 100 MHz

$$\text{Return\_Loss}(f) \begin{cases} 15 & (1 - 20\ \text{MHz}) \\ 15 - 10\log_{10}(f/20) & (20 - 100\ \text{MHz}) \end{cases} \text{ (dB)}$$

where $f$ is the frequency in MHz. The reference impedance shall be 100 Ω.

### 54.11.3 Coupling parameters

In order to limit the noise coupled into a duplex channel from adjacent duplex channels, Near-End Crosstalk (NEXT) loss and Equal Level Far-End Crosstalk (ELFEXT) loss are specified for each link segment. Each duplex channel can be disturbed by more than one duplex channel. Requirements for Multiple Disturber Near-End Crosstalk (MDNEXT) are satisfied even when worst case conditions of differential pair-to-pair NEXT as specified under <XREF>54.11.3.1.1 occur. Therefore, there are no separate requirements for MDNEXT. Requirements for Multiple Disturber Equal-Level Far-End Crosstalk (MDELFEXT) loss are specified in <XREF>54.11.3.2.2.

#### 54.11.3.1 Near-End Crosstalk (NEXT)

#### 54.11.3.1.1 Differential Near-End Crosstalk

In order to limit the crosstalk at the near end of a link segment, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between a duplex channel and the other three duplex channels is specified to meet the symbol error rate objective specified in 40.1. The NEXT loss between any two duplex channels of a link segment shall be at least

$$27.1 - 16.8\log_{10}(f/100)$$

where f is the frequency over the range of 1 MHz to 100 MHz.

NOTE—The above equation approximates the NEXT loss specification at discrete frequencies for Category 5 100-meter links specified in ANSI/TIA/EIA-568-A Annex E and in TSB-67.

#### 54.11.3.2 Far-End Crosstalk (FEXT)

#### 54.11.3.2.1 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk at the far end of each link segment duplex channel and meet the BER objective specified in <XREF>54.10.1.3.1. Far-End Crosstalk (FEXT) is crosstalk that appears at the far end of a duplex channel (disturbed channel), which is coupled from another duplex channel (disturbing channel) with the noise source (transmitters) at the near end. FEXT loss is defined as

$$\text{FEXT\_Loss}(f) = 20\log_{10}[V\text{pds}(f)/V\text{pcn}(f)]$$

and ELFEXT_Loss is defined as

$$\text{ELFEXT\_Loss}(f) = 20\log_{10}[V\text{pds}(f)/V\text{pcn}(f)] - \text{SLS\_Loss}(f)$$

where

| | |
|---|---|
| *V*pds | is the peak voltage of disturbing signal (near-end transmitter) |
| *V*pcn | is the peak crosstalk noise at far end of disturbed channel |
| SLS_Loss | is the insertion loss of disturbed channel in dB |

The worst pair ELFEXT loss between any two duplex channels shall be greater than $17 - 20\log_{10}(f/100)$ dB where $f$ is the frequency over the range of 1 MHz to 100 MHz.

#### 54.11.3.2.2 Multiple Disturber Equal Level Far-End Crosstalk (MDELFEXT) loss

Since four duplex channels are used to transfer data between PMDs, the FEXT that is coupled into a data carrying channel will be from the three adjacent disturbing duplex channels. This specification is consistent with three channel-to-channel disturbers—one with a ELFEXT loss of at least $17 - 20\log_{10}(f/100)$ dB, one with a ELFEXT loss of at least $19.5 - 20\log_{10}(f/100)$ dB, and one with a ELFEXT loss of at least $23 - 20\log_{10}(f/100)$ dB. To ensure the total FEXT coupled into a duplex channel is limited, multiple disturber ELFEXT loss is specified as the power sum of the individual ELFEXT losses.

The Power Sum loss between a duplex channel and the three adjacent disturbers shall be

$$\text{PSELFEXT loss} > 14.4 - 20\log_{10}(f/100)\ \text{dB}$$

where $f$ is the frequency over the range of 1 MHz to 100 MHz.

#### 54.11.3.2.3 Multiple-Disturber Power Sum Equal Level Far-End Crosstalk (PSELFEXT) loss

PSELFEXT loss is determined by summing the magnitude of the three individual pair-to-pair differential ELFEXT loss values over the frequency range 1 to 100 MHz as follows:

$$\text{PSELFEXT\_Loss(f)} = -10\log_{10}\sum_{i=1}^{i=3} 10^{-(NL(f)i)/10}$$

where

NL($f$)i is the magnitude of ELFEXT loss at frequency $f$ of pair combination i
i is the 1, 2, or 3 (pair-to-pair combination)

## 54.12 Environmental specifications

**NOTE:** These next set of paragraphs come from clause 53.

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801: 1995.

## 54.13 Protocol Implementation Conformance Statement (PICS) proforma for Clause 53, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-LX4[20]

### 54.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ae-2002, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-LX4 (Long Wavelength Laser), shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

[20] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

### 54.13.2 Identification

#### 54.13.2.1 Implementation identification

| | |
|---|---|
| Supplier[1] | |
| Contact point for enquiries about the PICS[1] | |
| Implementation Name(s) and Version(s)[1,3] | |
| Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2] | |
| NOTES<br>1—Required for all implementations.<br>2—May be completed as appropriate in meeting the requirements for the identification.<br>3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model). | |

#### 54.13.2.2 Protocol summary

| | |
|---|---|
| Identification of protocol standard | IEEE Std 802.3ae-2002, Clause 53, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-LX4 |
| Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS | |
| Have any Exception items been required? No [ ] Yes [ ]<br>(See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ae-2002.) | |

| | |
|---|---|
| Date of Statement | |

### 54.13.3 Major capabilities/options

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| LX4 | 10GBASE-LX4 PMD | 54.1 | Device supports long wave-length operation (1269-1356nm) | O/1 | Yes [ ]<br>No [ ] |
| *INS | Installation / cable | 53.13 | Items marked with INS include installation practices and cable specifications not applicable to a PHY manufacturer | O | Yes [ ]<br>No [ ] |
| OFP | Singlemode offset-launch mode-conditioning patch cord | 53.6 | Items marked with OFP include installation practices and cable specifications not applicable to a PHY manufacturer | O | Yes [ ]<br>No [ ] |
| TP1 | Standardized reference point TP1 exposed and available for testing | 54.6.1 | This point may be made available for use by implementers to certify component conformance | O | Yes [ ]<br>No [ ] |
| TP4 | Standardized reference point TP4 exposed and available for testing | 54.6.1 | This point may be made available for use by implementers to certify component conformance | O | Yes [ ]<br>No [ ] |
| DC | Delay constraints | 54.4 | Device conforms to delay constraints | M | Yes [ ] |
| *MD | MDIO capability | 54.5 | Registers and interface supported | O | Yes [ ]<br>No [ ] |

### 54.13.4 PICS proforma tables for 10GBASE-LX4 and baseband medium

#### 54.13.4.1 PMD Functional specifications

| Item | Feature | Sub clause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| FN1 | Integration with 10GBASE-X PCS and PMA and management functions | 54.1 | | M | Yes [ ] |
| FN2 | Transmit function | 54.6.2 | Convey bits requested by PMD_UNITDATA.request() to the MDI | M | Yes [ ] |
| FN3 | electrical multiplexing and delivery to the MDI | 54.6.2 | electrically multiplexes the four electrical signal streams for delivery to the MDI | M | Yes [ ] |
| FN4 | Mapping between electrical signal and logical signal for transmitter | 54.6.2 | Higher electrical power is a one | M | Yes [ ] |
| FN5 | Receive function | 54.6.3 | Convey bits received from the MDI to PMD_UNITDATA.indicate(rx_bit<0:3>) | M | Yes [ ] |
| FN6 | Conversion of four electrical signals to four electrical signals | 54.6.3 | Converts the four electrical signal streams into four electrical bit streams for delivery to the PMD service | M | Yes [ ] |
| FN7 | Mapping between electrical signal and logical signal for receiver | 54.6.3 | Higher electrical power is a one | M | Yes [ ] |
| FN8 | Receive function behavior | 54.6.3 | Conveys bits from PMD service primitive to the PMD service interface | M | Yes [ ] |
| FN9 | Global Signal Detect function | 54.6.4 | Report to the PMD service interface the message PMD_SIGNAL.indicate(SIGNAL_DETECT) | M | Yes [ ] |
| FN10 | Global Signal Detect behavior | 54.6.4 | SIGNAL_DETECT is a global indicator of the presence of electrical signals on all four lanes | M | Yes [ ] |
| FN11 | Lane-by-Lane Signal Detect function | 54.6.5 | Sets PMD_signal_detect_n values on a lane-by-lane basis per requirements of Table 54–4 | MD:O | Yes [ ]<br>No [ ]<br>N/A [ ] |
| FN12 | PMD_reset function | 54.6.6 | Resets the PMD sublayer | MD:O | Yes [ ]<br>No [ ]<br>N/A [ ] |

### 54.13.4.2 PMD to MDI electrical specifications for 10GBASE-LX4

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| PMS1 | Wavelength division multiplexed lane assignment | 53.5 | Device supports passbands defined in Table 53–5 | M | Yes [ ]<br>N/A [ ] |
| PMS2 | Transmitter meets specifications in Table 53–7 | 53.7.1 | Per measurement techniques in 53.9 | M | Yes [ ]<br>N/A [ ] |
| PMS3 | Receiver meets specifications in Table 53–8 | 53.7.2 | Per measurement techniques in 53.9 | M | Yes [ ]<br>N/A [ ] |

### 54.13.4.3 Management functions

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| MR1 | Management register set | 54.5 | | MD:M | Yes [ ]<br>N/A [ ] |
| MR2 | Global transmit disable function | 54.6.7 | Disables all of the electrical transmitters with the Global_PMD_transmit_disable variable | MD:O | Yes [ ]<br>No [ ]<br>N/A [ ] |
| MR3 | PMD_lane_by_lane_transmit_disable function | 54.6.8 | Disables the electrical transmitter on the lane associated with the PMD_transmit_disable_n variable | MD:O | Yes [ ]<br>No [ ]<br>N/A [ ] |
| MR4 | PMD_lane_by_lane_transmit_disable | 54.6.8 | Disables each electrical transmitter independently if FN12 = NO | O | Yes [ ]<br>No [ ] |
| MR5 | PMD_fault function | 54.6.9 | Sets PMD_fault to a logical 1 if any local fault is detected | MD:O | Yes [ ]<br>No [ ]<br>N/A [ ] |
| MR6 | PMD_transmit_fault function | 54.6.10 | Sets PMD_transmit_fault_n to a logical 1 if a local fault is detected on the transmit path x | MD:O | Yes [ ]<br>No [ ]<br>N/A [ ] |
| MR7 | PMD_receive_fault function | 54.6.11 | Sets PMD_receive_fault_x to a logical 1 if a local fault is detected on the receive path x | MD:O | Yes [ ]<br>No [ ]<br>N/A [ ] |

### 54.13.4.4 Jitter specifications

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| JS1 | Transmit jitter | 53.8.1 | Meet BER “bathtub curve” specifications | M | Yes [ ] |
| JS2 | Channel transmit jitter | 53.8.1.1 | As described in steps a) through c) in 53.8.1.1 | M | Yes [ ] |
| JS3 | Channel transmit jitter | 53.8.1.1 | Also tested on MMF as defined in 53.9.10.1 | M | Yes [ ] |
| JS4 | Receive jitter | 53.8.2 | BER less than $10^{-12}$ | M | Yes [ ] |
| JS5 | Receive jitter | 53.8.2.1 | Meets requirements of the receiver input jitter mask | M | Yes [ ] |
| JS6 | Receive jitter | 53.8.2.1 | Uniform spectral content over the measurement frequency range of 18.75kHz to 1.5GHz | M | Yes [ ] |
| JS7 | Receive jitter | 53.8.2.1 | Using a Clock Recovery Unit | M | Yes [ ] |
| JS8 | Receive jitter | 53.8.2.1 | Using a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade | M | Yes [ ] |
| JS9 | Receive jitter | 53.8.2.1 | Using fourth-order Bessel-Thomson filter | M | Yes [ ] |
| JS10 | Receive jitter | 53.8.2.2 | Meets the requirements of Table 53–11 | M | Yes [ ] |
| JS11 | Receive jitter | 53.8.2.2 | Sinusoidal jitter added to the test signal in compliance with 53.8.2.1 | M | Yes [ ] |

### 54.13.4.5 electrical measurement requirements

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| OM1 | Length of patch cord used for measurements | 53.9 | 2 to 5 m | M | Yes [ ] |
| OM2 | Wavelength ranges | 53.9.1 | Wavelengths fall within ranges specified inTable 53–5, and under modulated conditions using valid 10GBASE-X signals | M | Yes [ ] |
| OM3 | electrical power measurements | 53.9.2 | Per TIA/EIA-455-95 | M | Yes [ ] |
| OM4 | Source spectral window measurements | 53.9.3 | Individually measured per test setup in Figure 53–7, with all other channels below –30 dBm | M | Yes [ ] |
| OM5 | Source spectral window measurements | 53.9.3 | Under modulated conditions using valid 10GBASE-X signals | M | Yes [ ] |
| OM6 | Extinction ratio measurements | 53.9.4 | Per ANSI/TIA/EIA-526-4A | M | Yes [ ] |
| OM7 | OMA measurements | 53.9.5 | Each channel tested individually per methodology defined in 52.9.5 | M | Yes [ ] |
| OM8 | $RIN_{12}OMA$ | 53.9.6 | Each channel tested individually per methodology defined in 52.9.6 | | Yes [ ] |
| OM9 | Transmit eye | 53.9.7 | Per ANSI/TIA/EIA-526-4A (OFSTP-4) | M | Yes [ ] |
| OM10 | Transmit eye mask measurement conditions | 53.9.7 | Using fourth-order Bessel-Thomson filter | M | Yes [ ] |
| OM11 | Transmit eye mask measurement conditions | 53.9.7 | Using a Clock Recovery Unit to trigger the scope | M | Yes [ ] |
| OM12 | Transmit eye mask measurement conditions | 53.9.7 | Using a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade | M | Yes [ ] |
| OM13 | Transmit rise/fall characteristics conditions | 53.9.8 | Waveforms conform to mask in Figure 53–8, measured from 20% to 80%, using a patch cord | M | Yes [ ] |
| OM14 | Transmit rise/fall characteristics conditions | 53.9.8 | Removed mask conforming filter mathematically | M | Yes [ ] |
| OM15 | Transmit rise/fall characteristics conditions | 53.9.8 | Mask filters use a fourth-order Bessel-Thomson filter | M | Yes [ ] |
| OM16 | Receive sensitivity measurement conditions | 53.9.9 | Using conformance test at TP3 and meeting conditions specified in Table 53–8 | M | Yes [ ] |
| OM17 | Transmit jitter conformance measurement conditions | 53.9.10.1 | Using a fourth-order Bessel-Thomson filter for single-mode fiber | M | Yes [ ] |

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| OM18 | Transmit jitter conformance measurement conditions | 53.9.10.1 | Using a fourth-order Bessel-Thomson filter followed by a transversal filter with 2 equal amplitude paths with a differential delay of 157ps for multimode fiber | M | Yes [ ] |
| OM19 | Transmit jitter conformance measurement conditions | 53.9.10.1 | Using a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade | M | Yes [ ] |
| OM20 | Transmit jitter conformance measurement conditions | 53.9.10.1 | Measured at the average value of the overall waveform | M | Yes [ ] |
| OM21 | Transmit jitter conformance measurement conditions | 53.9.10.1 | Asynchronous data flowing in all four electrical receiver channels | M | Yes [ ] |
| OM22 | Transmit jitter conformance measurement conditions | 53.9.10.2 | Meets requirements listed in Table 53–12 | M | Yes [ ] |
| OM23 | Transmit jitter conformance measurement conditions | 53.9.10.2 | For single-mode fiber; compliant with dispersion at least as negative as the “minimum dispersion” and at least as positive as the “maximum dispersion” | M | Yes [ ] |
| OM24 | Transmit jitter conformance measurement conditions | 53.9.10.2 | Achieved using ITU-T G.652 fiber | M | Yes [ ] |
| OM25 | Transmit jitter conformance measurement conditions | 53.9.10.2 | Using the linear regime of the single-mode fiber | M | Yes [ ] |
| OM26 | Transmit jitter conformance measurement conditions | 53.9.10.2 | Provide an electrical back reflection specified in Table 53–7 | M | Yes [ ] |
| OM27 | Transmit jitter conformance measurement conditions | 53.9.10.2 | Back reflection adjusted to create the greatest RIN | M | Yes [ ] |
| OM28 | Transmit jitter conformance measurement conditions | 53.9.10.2 | For multimode fiber, back reflection set to –12dB | M | Yes [ ] |
| OM29 | Transmit jitter conformance measurement conditions | 53.9.10.3 | Using a low-frequency corner of less than or equal to 1.875MHz and a slope of 20dB/decade | M | Yes [ ] |
| OM30 | Receiver sensitivity | 53.9.11 | Meet the specifications in Table 53–8 | M | Yes [ ] |
| OM31 | Stressed receiver conformance conditions | 53.9.12 | Asynchronous data flowing out of the electrical transmitter of the system under test | M | Yes [ ] |
| OM32 | Stressed receiver conformance conditions | 53.9.12 | Data is consistent with normal signal properties and content | M | Yes [ ] |
| OM33 | Stressed receiver conformance conditions | 53.9.12.1 | Using a Clock Recovery Unit meeting the requirements of 53.8.2.1 | M | Yes [ ] |

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| OM34 | Stressed receiver conformance conditions | 53.9.12.1 | Calibrated at the average value of the overall electrical waveform | M | Yes [ ] |
| OM35 | Stressed receiver conformance conditions | 53.9.12.3 | Using a Clock Recovery Unit meeting the requirements of 53.8.2.1 | M | Yes [ ] |
| OM36 | Receiver 3dB electrical upper cutoff frequency | 53.9.13 | Performed on each channel independently using a laser source with its output wavelength within the specified wavelength range of the channel to be tested | M | Yes [ ] |
| OM37 | Receiver 3dB electrical upper cutoff frequency | 53.9.13 | As described in steps a) through e) of 53.9.13 | M | Yes [ ] |
| OM38 | Compliance test signal at TP3 | 53.9.14 | Meets the requirements of Figure 53–12 | M | Yes [ ] |
| OM39 | Compliance test signal at TP3 | 53.9.14 | DJ eye closure no less than 14ps | M | Yes [ ] |
| OM40 | Compliance test signal at TP3 | 53.9.14 | Vertical eye-closure penalty meets requirements of Table 53–8 | M | Yes [ ]<br>N/A [ ] |
| OM41 | Compliance test signal at TP3 | 53.9.14 | Bandwidth of photodetector > 2.34GHz, and couple through fourth-order Bessel-Thomson filter | M | Yes [ ] |
| OM42 | Receiver WDM conformance conditions | 53.9.15 | As described in steps a) through f) of 53.9.15 | M | Yes [ ] |
| OM43 | General safety | 53.10.1 | Conform to IEC-60950: 1991 | M | Yes [ ] |
| OM44 | Laser safety | 53.10.2 | Class 1 | M | Yes [ ] |
| OM45 | Compliance with all requirements over the life of the product | 53.11 | | M | Yes [ ] |
| OM46 | Compliance with applicable local and national codes for the limitation of electromagnetic interference | 53.11.1 | | M | Yes [ ] |

### 54.13.4.6 Characteristics of the fiber optic cabling

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| LI1 | Fiber optic cabling | 53.13 | Meets specifications in Table 53–13 | INS:M | Yes [ ]<br>N/A [ ] |
| LI2 | Return loss for multimode connections | 53.14.2.2 | > 20 dB | INS:M | Yes [ ]<br>No [ ]<br>N/A [ ] |
| LI3 | Return loss for singlemode connections | 53.14.2.2 | > 26 dB | INS:M | Yes [ ]<br>No [ ]<br>N/A [ ] |
| LI4 | MDI | 53.14.3 | IEC 61753-1-1 and IEC 61753-3-2 | M | Yes [ ] |