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**Proposal  
for  
an initial draft  
of a  
10GBASE-CX4 PMD**

by: Howard Baumer, Broadcom  
David Law, 3Com  
Naresh Raman, LSI Logic  
Peter Bradshaw, BitBlitz  
Schelto VanDoorn, Intel  
Jeff Cain, Cisco

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### 30.5.1.1.2 aMAUType

*Change this subclause as follows:*

ATTRIBUTE

APPROPRIATE SYNTAX:

A GET-SET ENUMERATION that meets the requirements of the description below:

global	undefined
other	See
unknown	Initializing, true state or type not yet known
AUI	no internal MAU, view from AUI
10BASE5	Thick coax MAU as specified in Clause 8
FOIRL	FOIRL MAU as specified in 9.9
10BASE2	Thin coax MAU as specified in Clause 10
10BROAD36	Broadband DTE MAU as specified in Clause 11
10BASE-T	UTP MAU as specified in Clause 14, duplex mode unknown
10BASE-THD	UTP MAU as specified in Clause 14, half duplex mode
10BASE-TFD	UTP MAU as specified in Clause 14, full duplex mode
10BASE-FP	Passive fiber MAU as specified in Clause 16
10BASE-FB	Synchronous fiber MAU as specified in Clause 17
10BASE-FL	Asynchronous fiber MAU as specified in Clause 18, duplex mode unknown
10BASE-FLHD	Asynchronous fiber MAU as specified in Clause 18, half duplex mode
10BASE-FLFD	Asynchronous fiber MAU as specified in Clause 18, full duplex mode
100BASE-T4	Four-pair Category 3 UTP as specified in Clause 23
100BASE-TX	Two-pair Category 5 UTP as specified in Clause 25, duplex mode unknown
100BASE-TXHD	Two-pair Category 5 UTP as specified in Clause 25, half duplex mode
100BASE-TXFD	Two-pair Category 5 UTP as specified in Clause 25, full duplex mode
100BASE-FX	X fiber over PMD as specified in Clause 26, duplex mode unknown
100BASE-FXHD	X fiber over PMD as specified in Clause 26, half duplex mode
100BASE-FXFD	X fiber over PMD as specified in Clause 26, full duplex mode
100BASE-T2	Two-pair Category 3 UTP as specified in Clause 32, duplex mode unknown
100BASE-T2HD	Two-pair Category 3 UTP as specified in Clause 32, half duplex mode
100BASE-T2FD	Two-pair Category 3 UTP as specified in Clause 32, full duplex mode
1000BASE-X	X PCS/PMA as specified in Clause 36 over undefined PMD, duplex mode unknown
1000BASE-XHD	X PCS/PMA as specified in Clause 36 over undefined PMD, half duplex mode
1000BASE-XFD	X PCS/PMA as specified in Clause 36 over undefined PMD, full duplex mode
1000BASE-LX	X fiber over long-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-LXHD	X fiber over long-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-LXFD	X fiber over long-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-SX	X fiber over short-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-SXHD	X fiber over short-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-SXFD	X fiber over short-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-CX	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, duplex mode unknown
1000BASE-CXHD	copper over 150-Ohm balanced cable PMD as specified in Clause 39, half duplex mode

1	1000BASE-CXFD	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, full
2		duplex mode
3	1000BASE-T	Four-pair Category 5 UTP PHY to be specified in Clause 40, duplex mode
4		unknown
5	1000BASE-THD	Four-pair Category 5 UTP PHY to be specified in Clause 40, half duplex mode
6	1000BASE-TFD	Four-pair Category 5 UTP PHY to be specified in Clause 40, full duplex mode
7	10GBASE-X	X PCS/PMA as specified in Clause 48 over undefined PMD
8	10GBASE-LX4	X fibre over 4 lane 1310nm optics as specified in Clause 53
9	<u>10GBASE-CX4</u>	<u>X copper over 8 pair 100-Ohm balanced cable as specified in Clause 54</u>
10	10GBASE-R	R PCS/PMA as specified in Clause 49 over undefined PMD
11	10GBASE-ER	R fibre over 1550nm optics as specified in Clause 52
12	10GBASE-LR	R fibre over 1310nm optics as specified in Clause 52
13	10GBASE-SR	R fibre over 850nm optics as specified in Clause 52
14	10GBASE-W	W PCS/PMA as specified in Clauses 49 and 50 over undefined PMD
15	10GBASE-EW	W fibre over 1550nm optics as specified in Clause 52
16	10GBASE-LW	W fibre over 1310nm optics as specified in Clause 52
17	10GBASE-SW	W fibre over 850nm optics as specified in Clause 52
18	802.9a	Integrated services MAU as specified in IEEE Std 802.9 ISLAN-16T

## 30B.2 ASN.1 module for CSMA/CD managed objects

*Change this subclause as follows:*

25	TypeValue::= ENUMERATED {	
26	global	(0), --undefined
27	other	(1), --undefined
28	unknown	(2), --initializing, true state not yet known
29	AUI	(7), --no internal MAU, view from AUI
30	10BASE5	(8), --Thick coax MAU as specified in Clause 8
31	FOIRL	(9), --FOIRL MAU as specified in 9.9
32	10BASE2	(10), --Thin coax MAU as specified in Clause 10
33	10BROAD36	(11), --Broadband DTE MAU as specified in Clause 11
34	10BASE-T	(14), --UTP MAU as specified in Clause 14, duplex mode
35		unknown
36	10BASE-THD	(141), --UTP MAU as specified in Clause 14, half duplex mode
37	10BASE-TFD	(142), --UTP MAU as specified in Clause 14, full duplex mode
38	10BASE-FP	(16), --Passive fiber MAU as specified in Clause 16
39	10BASE-FB	(17), --Synchronous fiber MAU as specified in Clause 17
40	10BASE-FL	(18), --Asynchronous fiber MAU as specified in Clause 18, duplex
41		mode unknown
42	10BASE-FLHD	(181), --Asynchronous fiber MAU as specified in Clause 18, half
43		duplex mode
44	10BASE-FLFD	(182), --Asynchronous fiber MAU as specified in Clause 18, full
45		duplex mode
46	100BASE-T4	(23), --Four-pair Category 3 UTP as specified in Clause 23
47	100BASE-TX	(25), --Two-pair Category 5 UTP as specified in Clause 25, duplex
48		mode unknown
49	100BASE-TXHD	(251), --Two-pair Category 5 UTP as specified in Clause 25, half
50		duplex mode
51	100BASE-TXFD	(252), --Two-pair Category 5 UTP as specified in Clause 25, full
52		duplex mode
53	100BASE-FX	(26), --X fiber over PMD as specified in Clause 26, duplex mode
54		unknown

100BASE-FXHD	(261),	--X fiber over PMD as specified in Clause 26, half duplex mode	1
100BASE-FXFD	(262),	--X fiber over PMD as specified in Clause 26, full duplex mode	2
100BASE-T2	(32),	--Two-pair Category 3 UTP as specified in Clause 32, duplex mode unknown	3 4
100BASE-T2HD	(321),	--Two-pair Category 3 UTP as specified in Clause 32, half duplex mode	5 6
100BASE-T2FD	(322),	--Two-pair Category 3 UTP as specified in Clause 32, full duplex mode	7 8
1000BASE-X	(36),	--X PCS/PMA as specified in Clause 36 over unknown PMD, duplex mode unknown	9 10
1000BASE-XHD	(361),	--X PCS/PMA as specified in Clause 36 over unknown PMD, half duplex mode	11 12
1000BASE-XFD	(362),	--X PCS/PMA as specified in Clause 36 over unknown PMD, full duplex mode	13 14
1000BASE-LX	(381),	--X fiber over long-wavelength laser PMD as specified in Clause 38, duplex mode unknown	15 16
1000BASE-LXHD	(382),	--X fiber over long-wavelength laser PMD as specified in Clause 38, half duplex mode	17 18
1000BASE-LXFD	(383),	--X fiber over long-wavelength laser PMD as specified in Clause 38, full duplex mode	19 20
1000BASE-SX	(384),	--X fiber over short-wavelength laser PMD as specified in Clause 38, duplex mode unknown	21 22
1000BASE-SXHD	(385),	--X fiber over short-wavelength laser PMD as specified in Clause 38, half duplex mode	23 24
1000BASE-SXFD	(386),	--X fiber over short-wavelength laser PMD as specified in Clause 38, full duplex mode	25 26
1000BASE-CX	(39),	--X copper over 150-Ohm balanced cable PMD as specified in Clause 39, duplex mode unknown	27 28
1000BASE-CXHD	(391),	--X copper over 150-Ohm balanced cable PMD as specified in Clause 39, half duplex mode	29 30
1000BASE-CXFD	(392),	--X copper over 150-Ohm balanced cable PMD as specified in Clause 39, full duplex mode	31 32
1000BASE-T	(40),	--Four-pair Category 5 UTP PHY as specified in Clause 40, duplex mode unknown	33 34
1000BASE-THD	(401),	--Four-pair Category 5 UTP PHY as specified in Clause 40, half duplex mode	35 36
1000BASE-TFD	(402),	--Four-pair Category 5 UTP PHY as specified in Clause 40, full duplex mode	37 38
10GBASE-X	(48)	--X PCS/PMA as specified in Clause 48 over undefined PMD	39
10GBASE-LX4	(481)	--X fibre over WWDM optics as specified in Clause 53	40
<u>10GBASE-CX4</u>	<u>(482)</u>	<u>--X copper over 8 pair 100-Ohm balanced cable as specified in Clause 54</u>	41 42
10GBASE-R	(49)	--R PCS/PMA as specified in Clause 49 over undefined PMD	43
10GBASE-ER	(491)	--R fibre over 1550nm optics as specified in Clause 52	44
10GBASE-LR	(492)	--R fibre over 1310nm optics as specified in Clause 52	45
10GBASE-SR	(493)	--R fibre over 850nm optics as specified in Clause 52	46
10GBASE-W	(50)	--W PCS/PMA as specified in Clauses 49 and 50 over undefined PMD	47 48
10GBASE-EW	(501)	--W fibre over 1550nm optics as specified in Clause 52	49
10GBASE-LW	(502)	--W fibre over 1310nm optics as specified in Clause 52	50
10GBASE-SW	(503)	--W fibre over 850nm optics as specified in Clause 52	51
802.9a	(99)	--Integrated services MAU as specified in IEEE Std 802.9 ISLAN-16T	52 53 54

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7 **IEEE Standard for Information technology—**  
8 **Telecommunications and information exchange between systems—**  
9 **Local and metropolitan area networks—**  
10 **Specific requirements—**

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12 **Part 3: Carrier Sense Multiple Access with**  
13 **Collision Detection (CSMA/CD) Access Method**  
14 **and Physical Layer Specifications—**

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16 **Amendment: Media Access Control (MAC)**  
17 **Parameters, Physical Layers, and Management**  
18 **Parameters for 10 Gb/s Operation**

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25 **44. Introduction to 10 Gb/s baseband network**

26  
27 **44.1 Overview**

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29 **44.1.1 Scope**

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31  
32 10 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer, connected through a 10 Gigabit Media Independent  
33 Interface (XGMII) to Physical Layer entities such as 10GBASE-SR, 10GBASE-LX4, 10GBASE-CX4,  
34 10GBASE-LR, 10GBASE-ER, 10GBASE-SW, 10GBASE-LW, and 10GBASE-EW.

35  
36 10 Gigabit Ethernet extends the IEEE 802.3 MAC beyond 1000 Mb/s to 10 Gb/s. The bit rate is faster and  
37 the bit times are shorter—both in proportion to the change in bandwidth. The minimum packet transmission  
38 time has been reduced by a factor of ten. A rate control mode (see 4.2.3.2.2) is added to the MAC to adapt  
39 the average MAC data rate to the SONET/SDH data rate for WAN-compatible applications of this standard.  
40 Achievable topologies for 10 Gb/s operation are comparable to those found in 1000BASE-X full duplex  
41 mode and equivalent to those found in WAN applications.

42  
43 10 Gigabit Ethernet is defined for full duplex mode of operation only.

44  
45 **44.1.2 Objectives**

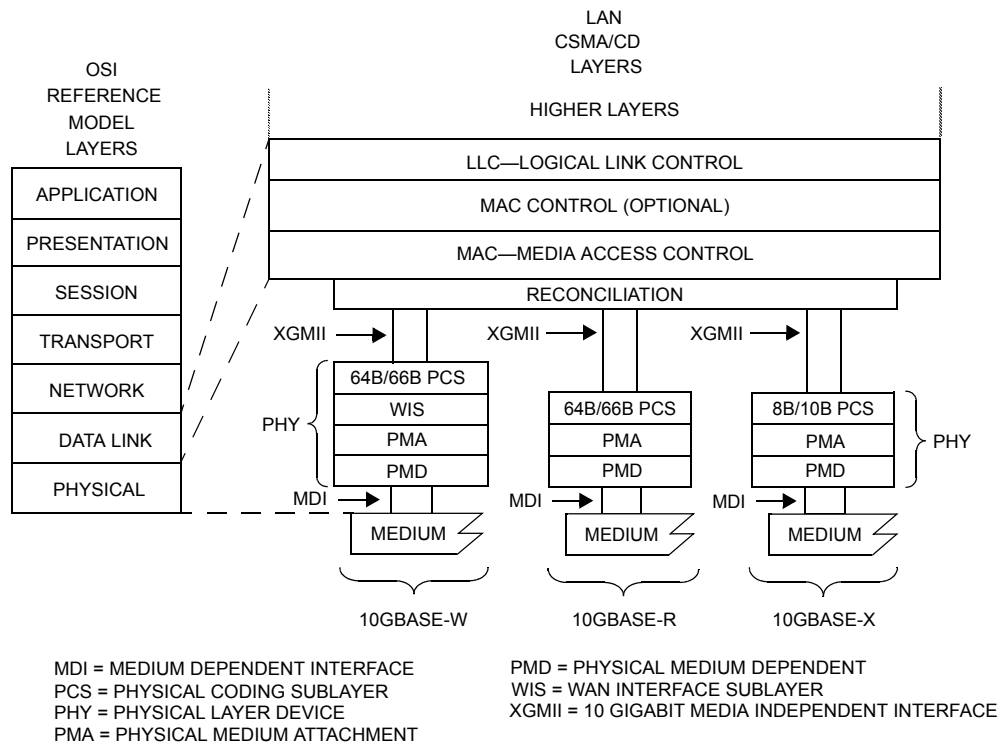
46 The following are the objectives of 10 Gigabit Ethernet:

- 47  
48 a) Support the full duplex Ethernet MAC.  
49 b) Provide 10 Gb/s data rate at the XGMII.  
50 c) Support LAN PMDs operating at 10 Gb/s, and WAN PMDs operating at SONET STS-192c/SDH  
51 VC-4-64c rate.  
52 d) Support cable plants using optical fiber compliant with ISO/IEC 11801: 1995.  
53 e) Allow for a nominal network extent of up to 40 km.  
54

- f) Support operation over 15m of copper cable as specified in section 54.x.
- g) Meet or exceed FCC/CISPR Class A operation.
- h) Support a BER objective of  $10^{-12}$ .

**44.1.3 Relationship of 10 Gigabit Ethernet to the ISO OSI reference model**

10 Gigabit Ethernet couples the IEEE 802.3 (CSMA/CD) MAC to a family of 10 Gb/s Physical Layers. The relationships among 10 Gigabit Ethernet, the IEEE 802.3 (CSMA/CD) MAC, and the ISO Open System Interconnection (OSI) reference model are shown in Figure 44-1.



**Figure 44-1—Architectural positioning of 10 Gigabit Ethernet**

It is important to note that, while this specification defines interfaces in terms of bits, octets, and frames, implementations may choose other data-path widths for implementation convenience. The only exceptions are as follows:

- a) The XGMII, which, when implemented at an observable interconnection port, uses a four octet-wide data path as specified in Clause 46.
- b) The management interface, which, when physically implemented as the MDIO/MDC (Management Data Input/Output and Management Data Clock) at an observable interconnection port, uses a bit-wide data path as specified in Clause 45.
- c) The PMA Service Interface, which, when physically implemented as the XSBI (10 Gigabit Sixteen Bit Interface) at an observable interconnection port, uses a 16-bit-wide data path as specified in Clause 51.
- d) The MDI as specified in Clause 53 for 10GBASE-LX4, Clause 54 for 10GBASE-CX4 and in Clause 52 for other PMD types.



**44.1.4 Summary of 10 Gigabit Ethernet sublayers**

**44.1.4.1 Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)**

The 10 Gigabit Media Independent Interface (Clause 46) provides an interconnection between the Media Access Control (MAC) sublayer and Physical Layer entities (PHY). This XGMII supports 10 Gb/s operation through its 32-bit-wide transmit and receive data paths. The Reconciliation Sublayer provides a mapping between the signals provided at the XGMII and the MAC/PLS service definition.

While the XGMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for Clauses 47, 48, and 49.

**44.1.4.2 XGMII Extender Sublayer (XGXS) and 10 Gigabit Attachment Unit Interface (XAUI)**

The 10 Gigabit Attachment Unit Interface (Clause 47) provides an interconnection between two XGMII Extender sublayers to increase the reach of the XGMII. This XAUI supports 10 Gb/s operation through its four-lane, differential-pair transmit and receive paths. The XGXS provides a mapping between the signals provided at the XGMII and the XAUI.

**44.1.4.3 Management interface (MDIO/MDC)**

The MDIO/MDC management interface (Clause 45) provides an interconnection between MDIO Manageable Devices (MMD) and Station Management (STA) entities.

**44.1.4.4 Physical Layer signaling systems**

This standard specifies a family of Physical Layer implementations. The generic term 10 Gigabit Ethernet refers to any use of the 10 Gb/s IEEE 802.3 MAC (the 10 Gigabit Ethernet MAC) coupled with any IEEE 802.3 10GBASE physical layer implementation. Table 44–1 specifies the correlation between nomenclature and clauses. Implementations conforming to one or more nomenclatures shall meet the requirements of the corresponding clauses.

**Table 44–1—Nomenclature and clause correlation**

Nomenclature	Clause								
	48 8B/10B PCS & PMA	49 64B/66B PCS	50 WIS	51 Serial PMA	52			53	54
					850 nm Serial PMD	1310 nm Serial PMD	1550 nm Serial PMD	1310 nm WDM PMD	PMD
10GBASE-SR		M <sup>a</sup>		M	M				
10GBASE-SW		M	M	M	M				
10GBASE-LX4	M							M	
10GBASE-CX4	M								M
10GBASE-LR		M		M		M			
10GBASE-LW		M	M	M		M			
10GBASE-ER		M		M			M		
10GBASE-EW		M	M	M			M		

<sup>a</sup>M = Mandatory

1 The term 10GBASE-X, specified in Clauses 48, 53 and 54, refers to a specific family of physical layer  
2 implementations based upon 8B/10B data coding method. The 10GBASE-X family of physical layer imple-  
3 mentations is composed of 10GBASE-LX4 and 10GBASE-CX4.

4  
5 The term 10GBASE-R, specified in Clauses 49, 51, and 52, refers to a specific family of physical layer  
6 implementations based upon 64B/66B data coding method. The 10GBASE-R family of physical layer  
7 implementations is composed of 10GBASE-SR, 10GBASE-LR, and 10GBASE-ER.

8  
9 The term 10GBASE-W, specified in Clause 49 to Clause 52, refers to a specific family of physical layer  
10 implementations based upon STS-192c/SDH VC-4-64c encapsulation of 64B/66B encoded data. The  
11 10GBASE-W family of physical layer standards has been adapted from the ANSI T1.416-1999 (SONET  
12 STS-192c/SDH VC-4-64c) physical layer specifications. The 10GBASE-W family of physical layer imple-  
13 mentations is composed of 10GBASE-SW, 10GBASE-LW, and 10GBASE-EW.

14  
15 All 10GBASE-R and 10GBASE-W PHY devices share a common PCS specification (see Clause 49). The  
16 10GBASE-W PHY devices also require the use of the WAN Interface Sublayer, (WIS) (Clause 50).

17  
18 Specifications of each physical layer device are contained in Clause 52 and Clause 53 and Clause 54.

#### 19 **44.1.4.5 WAN Interface Sublayer (WIS), type 10GBASE-W**

20  
21 The WIS provides a 10GBASE-W device with the capability to transmit and receive IEEE 802.3 MAC  
22 frames within the payload envelope of a SONET STS-192c/SDH VC-4-64c frame.

#### 23 **44.1.5 Management**

24  
25 Managed objects, attributes, and actions are defined for all 10 Gigabit Ethernet components. Clause 30 con-  
26 solidates all IEEE 802.3 management specifications so that 10/100/1000 Mb/s and 10 Gb/s agents can be  
27 managed by existing network management stations with little or no modification to the agent code.

#### 28 **44.2 State diagrams**

29  
30 State machine diagrams take precedence over text.

31  
32 The conventions of 1.2 are adopted, along with the extensions listed in 21.5.

#### 33 **44.3 Delay constraints**

34  
35 Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be  
36 an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sub-  
37 layer, and PHY implementers must conform to certain delay maxima, and that network planners and admin-  
38 istrators conform to constraints regarding the cable topology and concatenation of devices. Table 44-2  
39 contains the values of maximum sublayer round-trip (sum of transmit and receive) delay in bit time as spec-  
40 ified in 1.4 and pause\_quanta as specified in 31B.2.

41  
42 Equation (44-1) specifies the calculation of bit time per meter of fiber based upon the parameter  $n$ , which  
43 represents the ratio of the speed of light in the fiber to the speed of light in a vacuum. The value of  $n$  should  
44 be available from the fiber manufacturer, but if no value is known then a conservative delay estimate can be  
45 calculated using a default value of  $n = 0.66$ . The speed of light in a vacuum is  $c = 3 \times 10^8$  m/s. Table 44-3  
46 can be used to convert fiber delay values specified relative to the speed of light or in nanoseconds per meter.

**Table 44-2—Round-trip delay constraints (informative)**

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Notes
MAC, RS and MAC Control	8192	16	See 46.1.4.
XGXS and XAUI	4096	8	Round-trip of 2 XGXS and trace for both directions. See 47.2.2.
10GBASE-X PCS and PMA	2048	4	See 48.5.
10GBASE-R PCS	3584	7	See 49.2.15.
WIS	14336	28	See 50.3.7.
CX4 PMD	512	1	Includes 15m of 24AWG cable.
LX4 PMD	512	1	Includes 2 meters of fiber. See 53.2.
Serial PMA and PMD	512	1	Includes 2 meters of fiber. See 52.2.

$$\text{cable delay} = \frac{10^{10}}{nc} \text{ BT/m} \tag{44-1}$$

**Table 44-3—Conversion table for cable delays**

Speed relative to c	ns/m	BT/m
0.40	8.33	83.3
0.50	6.67	66.7
0.51	6.54	65.4
0.52	6.41	64.1
0.53	6.29	62.9
0.54	6.17	61.7
0.55	6.06	60.6
0.56	5.95	59.5
0.57	5.85	58.5
0.58	5.75	57.5
0.5852	5.70	57.0
0.59	5.65	56.5
0.60	5.56	55.6

**Table 44–3—Conversion table for cable delays (continued)**

Speed relative to c	ns/m	BT/m
0.61	5.46	54.6
0.62	5.38	53.8
0.63	5.29	52.9
0.64	5.21	52.1
0.65	5.13	51.3
0.654	5.10	51.0
0.66	5.05	50.5
0.666	5.01	50.1
0.67	4.98	49.8
0.68	4.90	49.0
0.69	4.83	48.3
0.7	4.76	47.6
0.8	4.17	41.7
0.9	3.70	37.0

**44.4 Protocol Implementation Conformance Statement (PICS) proforma**

The supplier of a protocol implementation that is claimed to conform to any part of IEEE 802.3, Clause 45 through Clause 54, demonstrates compliance by completing a Protocol Implementation Conformance Statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. Each of the 10 Gigabit Ethernet PICS conforms to the same notation and conventions used in 100BASE-T (see 21.6).

**44.5 Relation of 10 Gigabit Ethernet to other standards**

Suitable entries for Table G1 of ISO/IEC 11801: 1995, Annex G, would be as follows:

- a) Within the section Optical Link:  
CSMA/CD 10GBASE-SR      ISO/IEC 8802-3/ PDAM 26
- b) Within the section Optical Link:  
CSMA/CD 10GBASE-SW      ISO/IEC 8802-3/PDAM 26
- c) Within the section Optical Link:  
CSMA/CD 10GBASE-LR      ISO/IEC 8802-3/PDAM 26

- d) Within the section Optical Link:  
CSMA/CD 10GBASE-LW      ISO/IEC 8802-3/PDAM 26
- e) Within the section Optical Link:  
CSMA/CD 10GBASE-ER      ISO/IEC 8802-3/PDAM 26
- f) Within the section Optical Link:  
CSMA/CD 10GBASE-EW      ISO/IEC 8802-3/PDAM 26
- g) Within the section Optical Link:  
CSMA/CD 10GBASE-LX4      ISO/IEC 8802-3/PDAM 26

A suitable entry for Table G5 of ISO/IEC 11801: 1995, Annex G, is exemplified in Table 44–4.

**Table 44–4—Table G5 of ISO/IEC 11801: 1995**

	Fibre			Optical link per Clause 8								
	per Clauses 5, 7, and 8			Horizontal			Building backbone			Campus backbone		
	62.5/ 125 µm MMF	50/125 µm MMF	10/125 µm SMF	62.5/ 125 µm MMF	50/ 125 µm MMF	10/ 125 µm SMF	62.5/ 125 µm MMF	50/ 125 µm MMF	10/ 125 µm SMF	62.5/ 125 µm MMF	50/ 125 µm MMF	10/ 125 µm SMF
8802-3: 10GBASE-SR	I	I		I	N		I	I		I	I	
8802-3: 10GBASE-SW	I	I		I	N		I	I		I	I	
8802-3: 10GBASE-LR	I	I	I	I	I	N	I	I	N	I	I	N
8802-3: 10GBASE-LW	I	I	I	I	I	N	I	I	N	I	I	N
8802-3: 10GBASE-ER			I			N			N			N
8802-3: 10GBASE-EW			I			N			N			N
8802-3: 10GBASE-LX4	I	I	I	N	N	N	N	N	N	N	N	N

NOTE—"N" denotes normative support of the media in the standard.  
"I" denotes that there is information in the International Standard regarding operation on this media.

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## 45. Management Data Input/Output (MDIO) Interface

### 45.1 Overview

This clause defines the logical and electrical characteristics of an extension to the two signal Management Data Input/Output (MDIO) Interface specified in Clause 22.

The purpose of this extension is to provide the ability to access more device registers while still retaining logical compatibility with the MDIO interface defined in Clause 22. Clause 22 specifies the MDIO frame format and uses an ST code of 01 to access registers. In this clause, additional registers are added to the address space by defining MDIO frames that use an ST code of 00.

This extension to the MDIO interface is applicable to Ethernet implementations that operate at speeds of 10 Gb/s and above.

The MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

Throughout this clause, an “a.b.c” format is used to identify register bits, where “a” is the device address, “b” is the register address, and “c” is the bit number within the register.

#### 45.1.1 Summary of major concepts

The following are major concepts of the MDIO Interface:

- a) Preserve the management frame structure defined in 22.2.4.5.
- b) Define a mechanism to address more registers than specified in 22.2.4.5.
- c) Define ST and OP codes to identify and control the extended access functions.
- d) Provide an electrical interface specification that is compatible with common digital CMOS ASIC processes.

#### 45.1.2 Application

This clause defines a management interface between Station Management (STA) and the sublayers that form a 10 Gb/s Physical Layer device (PHY) entity. Where a sublayer, or grouping of sublayers, is an individually manageable entity, it is known as an MDIO Manageable Device (MMD). This clause allows a single STA, through a single MDIO interface, to access up to 32 PHYs (defined as PRTAD in the frame format defined in 45.3) consisting of up to 32 MMDs as shown in Figure 45–1. The MDIO interface can support up to a maximum of 65 536 registers in each MMD.

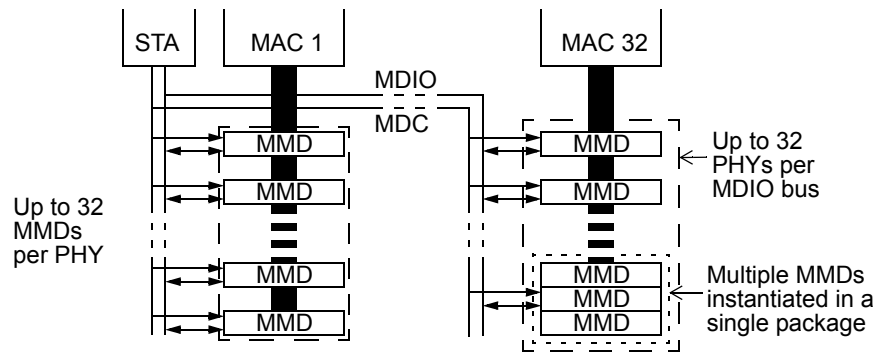


Figure 45–1—DTE and MMD devices

45.2 MDIO Interface Registers

The management interface specified in Clause 22 provides a simple, two signal, serial interface to connect a Station Management entity and a managed PHY for providing access to management parameters and services. The interface is referred to as the MII management interface.

The MDIO interface is based on the MII management interface, but differs from it in several ways. The MDIO interface uses indirect addressing to create an extended address space allowing a much larger number of registers to be accessed within each MMD. The MDIO address space is orthogonal to the MII management interface address space. The mechanism for the addressing is defined in 45.3. The MDIO electrical interface operates at lower voltages than those specified for the MII management interface. The electrical interface is specified in 45.4. For cases where a single entity combines Clause 45 MMDs with Clause 22 registers, then the Clause 22 registers may be accessed using the Clause 45 electrical interface and the Clause 22 management frame structure. The list of possible MMDs is shown in Table 45–1. The PHY XS and DTE XS devices are the two partner devices used to extend the interface that sits immediately below the Reconciliation Sublayer. For 10 Gigabit Ethernet, the interface extenders are defined as the XGXS devices.

If a device supports the MDIO interface it shall respond to all possible register addresses for the device and return a value of zero for undefined and unsupported registers. Writes to undefined registers and read-only registers shall have no effect. The operation of an MMD shall not be affected by writes to reserved and unsupported register bits, and such register bits shall return a value of zero when read.

To ensure compatibility with future use of reserved bits and registers, the Management Entity should write to reserved bits with a value of zero and ignore reserved bits on read.

Some of the bits within MMD registers are defined as latching low (LL) or latching high (LH). When a bit is defined as latching low and the condition for the bit to be low has occurred, the bit shall remain low until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors. When a bit is defined as latching high and the condition for the bit to be high has occurred, the bit shall remain high until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors.

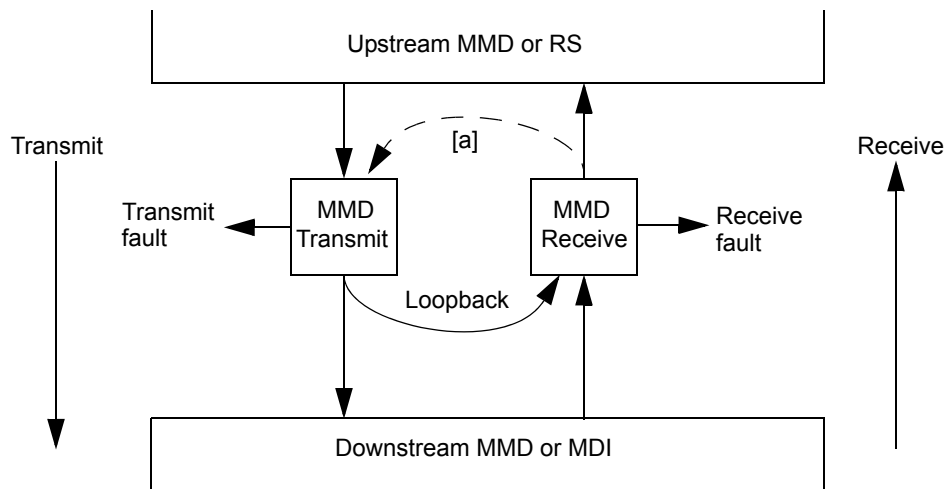


**Table 45–1—MDIO Manageable Device addresses**

Device address	MMD name
0	Reserved
1	PMA/PMD
2	WIS
3	PCS
4	PHY XS
5	DTE XS
6 through 29	Reserved
30	Vendor specific 1
31	Vendor specific 2

For multi-bit fields, the lowest numbered bit of the field in the register corresponds to the least significant bit of the field.

Figure 45–2 describes the signal terminology used for the MMDs.



**Figure 45–2—MMD signal terminology**

[a] Direction of the optional PHY XS loopback

**45.2.1 PMA/PMD registers**

The assignment of registers in the PMA/PMD is shown in Table 45–2.

**Table 45-2—PMA/PMD registers**

Register address	Register name
1.0	PMA/PMD control 1
1.1	PMA/PMD status 1
1.2, 1.3	PMA/PMD device identifier
1.4	PMA/PMD speed ability
1.5, 1.6	PMA/PMD devices in package
1.7	10G PMA/PMD control 2
1.8	10G PMA/PMD status 2
1.9	10G PMD transmit disable
1.10	10G PMD receive signal detect
1.11 through 1.13	Reserved
1.14, 1.15	PMA/PMD package identifier
1.16 through 1.32 767	Reserved
1.32 768 through 1.65 535	Vendor specific

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**45.2.1.1 PMA/PMD control 1 register (Register 1.0)**

The assignment of bits in the PMA/PMD control 1 register is shown in Table 45–3. The default value for each bit of the PMA/PMD control 1 register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

**Table 45–3—PMA/PMD control 1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
1.0.15	Reset	1 = PMA/PMD reset 0 = Normal operation	R/W SC
1.0.14	Reserved	Value always 0, writes ignored	R/W
1.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
1.0.12	Reserved	Value always 0, writes ignored	R/W
1.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
1.0.10:7	Reserved	Value always 0, writes ignored	R/W
1.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
1.0.5:2	Speed selection	$\underline{5} \ \underline{4} \ \underline{3} \ \underline{2}$ 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
1.0.1	Reserved	Value always 0, writes ignored	R/W
1.0.0	PMA loopback	1 = Enable PMA Loopback mode 0 = Disable PMA Loopback mode	R/W

<sup>a</sup>R/W = Read/Write, SC = Self Clearing

**45.2.1.1.1 Reset (1.0.15)**

Resetting a PMA/PMD is accomplished by setting bit 1.0.15 to a one. This action shall set all PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PMA/PMD shall return a value of one in bit 1.0.15 when a reset is in progress; otherwise, it shall return a value of zero. A PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.0.15. During a reset, a PMD/PMA shall respond to reads from register bits 1.0.15 and 1.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication. The data path of a PMD, depending on type and temperature, may take many seconds to run at optimum error rate after exiting from reset or low-power mode.

**45.2.1.1.2 Low power (1.0.11)**

A PMA/PMD may be placed into a low-power mode by setting bit 1.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PMA/PMD. The behavior of the PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.0.11 is zero.

NOTE—This operation will interrupt data communication. The data path of a PMD, depending on type and temperature, may take many seconds to run at optimum error rate after exiting from reset or low-power mode.

**45.2.1.1.3 Speed selection (1.0.13,1.0.6, 1.0.5:2)**

Speed selection bits 1.0.13 and 1.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PMA/PMD may be selected using bits 5 through 2. The speed abilities of the PMA/PMD are advertised in the PMA/PMD speed ability register. A PMA/PMD may ignore writes to the PMA/PMD speed selection bits that select speeds it has not advertised in the PMA/PMD speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PMA/PMD speed selection defaults to a supported ability.

**45.2.1.1.4 PMA loopback (1.0.0)**

The PMA shall be placed in a Loopback mode of operation when bit 1.0.0 is set to a one. When bit 1.0.0 is set to a one, the PMA shall accept data on the transmit path and return it on the receive path.

The loopback function is mandatory for the 10GBASE-X port type and optional for all other port types. A device's ability to perform the loopback function is advertised in the loopback ability bit of the related speed-dependent status register. A PMA that is unable to perform the loopback function shall ignore writes to this bit and shall return a value of zero when read. For 10 Gb/s operation, the loopback functionality is detailed in 48.3.3 and 51.8, and the loopback ability bit is specified in the 10G PMA/PMD status 2 register.

The default value of bit 1.0.0 is zero.

NOTE—The signal path through the PMA that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PMA circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

**45.2.1.2 PMA/PMD status 1 register (Register 1.1)**

The assignment of bits in the status 1 register is shown in Table 45–4. All the bits in the status 1 register are read only; therefore, a write to the status 1 register shall have no effect.

**Table 45–4—PMA/PMD status 1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
1.1.15:8	Reserved	Ignore when read	RO
1.1.7	Fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.1.6:3	Reserved	Ignore when read	RO
1.1.2	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL
1.1.1	Low-power ability	1 = PMA/PMD supports low-power mode 0 = PMA/PMD does not support low-power mode	RO
1.1.0	Reserved	Ignore when read	RO

<sup>a</sup>RO = Read Only, LL = Latching Low

**45.2.1.2.1 Fault (1.1.7)**

Fault is a global PMA/PMD variable. When read as a one, bit 1.1.7 indicates that either (or both) the PMA or the PMD has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 1.1.7 indicates that neither the PMA nor the PMD has detected a fault condition. For 10 Gb/s operation, bit 1.1.7 is set to a one when either of the fault bits (1.8.11, 1.8.10) located in register 1.8 are set to a one.

**45.2.1.2.2 Receive link status (1.1.2)**

When read as a one, bit 1.1.2 indicates that the PMA/PMD receive link is up. When read as a zero, bit 1.1.2 indicates that the PMA/PMD receive link is down. The receive link status bit shall be implemented with latching low behavior.

**45.2.1.2.3 Low-power ability (1.1.1)**

When read as a one, bit 1.1.1 indicates that the PMA/PMD supports the low-power feature. When read as a zero, bit 1.1.1 indicates that the PMA/PMD does not support the low-power feature. If a PMA/PMD supports the low-power feature, then it is controlled using the low-power bit 1.0.11.

**45.2.1.3 PMA/PMD device identifier (Registers 1.2 and 1.3)**

Registers 1.2 and 1.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PMA/PMD. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PMA/PMD may return a value of zero in each of the 32 bits of the PMA/PMD device identifier.

The format of the PMA/PMD device identifier is specified in 22.2.4.3.1.

**45.2.1.4 PMA/PMD speed ability (Register 1.4)**

The assignment of bits in the PMA/PMD speed ability register is shown in Table 45–5.

**Table 45–5—PMA/PMD speed ability register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
1.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
1.4.0	10G capable	1 = PMA/PMD is capable of operating at 10 Gb/s 0 = PMA/PMD is not capable of operating at 10 Gb/s	RO

<sup>a</sup>RO = Read Only

**45.2.1.4.1 10G capable (1.4.0)**

When read as a one, bit 1.4.0 indicates that the PMA/PMD is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 1.4.0 indicates that the PMA/PMD is not able to operate at a data rate of 10 Gb/s.

**45.2.1.5 PMA/PMD devices in package (Registers 1.5 and 1.6)**

The assignment of bits in the PMA/PMD devices in package registers is shown in Table 45–6.

When read as a one, a bit in the PMA/PMD devices in package registers indicates that the associated MMD has been instantiated within the same package as other MMDs whose associated bits have been set to a one within the PMA/PMD devices in package registers. Bit 1.5.0 is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

**45.2.1.6 10G PMA/PMD control 2 register (Register 1.7)**

The assignment of bits in the 10G PMA/PMD control 2 register is shown in Table 45–7.

**45.2.1.6.1 PMA/PMD type selection (1.7.3:0)**

The PMA/PMD type of the 10G PMA/PMD shall be selected using bits 3 through 0. The PMA/PMD type abilities of the 10G PMA/PMD are advertised in bits 7 through 0 of the 10G PMA/PMD status 2 register. A 10G PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised in the status register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

The PMA/PMD type selection defaults to a supported ability.

**Table 45-6— PMA/PMD devices in package registers bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
1.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
1.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
1.6.13:0	Reserved	Ignore on read	RO
1.5.15:6	Reserved	Ignore on read	RO
1.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
1.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
1.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
1.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
1.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
1.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

<sup>a</sup>RO = Read Only

**Table 45-7—10G PMA/PMD control 2 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
1.7.15:4	Reserved	Value always 0, writes ignored	R/W
1.7.3:0	PMA/PMD type selection	$\begin{matrix} 3 & 2 & 1 & 0 \\ 1 & 1 & 1 & x = \text{Reserved} \\ 1 & 1 & 0 & 1 = \text{Reserved} \\ 1 & 1 & 0 & 0 = \text{10GBASE-CX4 PMA/PMD type} \\ 1 & 0 & x & x = \text{Reserved} \\ 0 & 1 & 1 & 1 = \text{10GBASE-SR PMA/PMD type} \\ 0 & 1 & 1 & 0 = \text{10GBASE-LR PMA/PMD type} \\ 0 & 1 & 0 & 1 = \text{10GBASE-ER PMA/PMD type} \\ 0 & 1 & 0 & 0 = \text{10GBASE-LX4 PMA/PMD type} \\ 0 & 0 & 1 & 1 = \text{10GBASE-SW PMA/PMD type} \\ 0 & 0 & 1 & 0 = \text{10GBASE-LW PMA/PMD type} \\ 0 & 0 & 0 & 1 = \text{10GBASE-EW PMA/PMD type} \\ 0 & 0 & 0 & 0 = \text{Reserved} \end{matrix}$	R/W

<sup>a</sup>R/W = Read/Write

**45.2.1.7 10G PMA/PMD status 2 register (Register 1.8)**

The assignment of bits in the 10G PMA/PMD status 2 register is shown in Table 45–8. All the bits in the 10G PMA/PMD status 2 register are read only; a write to the 10G PMA/PMD status 2 register shall have no effect.

**Table 45–8—10G PMA/PMD status 2 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>															
1.8.15:14	Device present	<table border="0"> <tr> <td><u>15</u></td> <td><u>14</u></td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>= Device responding at this address</td> </tr> <tr> <td>1</td> <td>1</td> <td>= No device responding at this address</td> </tr> <tr> <td>0</td> <td>1</td> <td>= No device responding at this address</td> </tr> <tr> <td>0</td> <td>0</td> <td>= No device responding at this address</td> </tr> </table>	<u>15</u>	<u>14</u>		1	0	= Device responding at this address	1	1	= No device responding at this address	0	1	= No device responding at this address	0	0	= No device responding at this address	RO
<u>15</u>	<u>14</u>																	
1	0	= Device responding at this address																
1	1	= No device responding at this address																
0	1	= No device responding at this address																
0	0	= No device responding at this address																
1.8.13	Transmit fault ability	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path	RO															
1.8.12	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO															
1.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH															
1.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH															
1.8.9	10GBASE-CX4 ability	1 = PMA/PMD is able to perform 10GBASE-CX4 0 = PMA/PMD is not able to perform 10GBASE-CX4	RO															
1.8.8	PMD transmit disable ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO															
1.8.7	10GBASE-SR ability	1 = PMA/PMD is able to perform 10GBASE-SR 0 = PMA/PMD is not able to perform 10GBASE-SR	RO															
1.8.6	10GBASE-LR ability	1 = PMA/PMD is able to perform 10GBASE-LR 0 = PMA/PMD is not able to perform 10GBASE-LR	RO															
1.8.5	10GBASE-ER ability	1 = PMA/PMD is able to perform 10GBASE-ER 0 = PMA/PMD is not able to perform 10GBASE-ER	RO															
1.8.4	10GBASE-LX4 ability	1 = PMA/PMD is able to perform 10GBASE-LX4 0 = PMA/PMD is not able to perform 10GBASE-LX4	RO															
1.8.3	10GBASE-SW ability	1 = PMA/PMD is able to perform 10GBASE-SW 0 = PMA/PMD is not able to perform 10GBASE-SW	RO															
1.8.2	10GBASE-LW ability	1 = PMA/PMD is able to perform 10GBASE-LW 0 = PMA/PMD is not able to perform 10GBASE-LW	RO															



**Table 45–8—10G PMA/PMD status 2 register bit definitions (continued)**

Bit(s)	Name	Description	R/W <sup>a</sup>
1.8.1	10GBASE-EW ability	1 = PMA/PMD is able to perform 10GBASE-EW 0 = PMA/PMD is not able to perform 10GBASE-EW	RO
1.8.0	PMA loopback ability	1 = PMA has the ability to perform a loopback function 0 = PMA does not have the ability to perform a loopback function	RO

<sup>a</sup>RO = Read Only, LH = Latching High

**45.2.1.7.1 Device present (1.8.15:14)**

When read as <10>, bits 1.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 1.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

**45.2.1.7.2 Transmit fault ability (1.8.13)**

When read as a one, bit 1.8.13 indicates that the PMA/PMD has the ability to detect a fault condition on the transmit path. When read as a zero, bit 1.8.13 indicates that the PMA/PMD does not have the ability to detect a fault condition on the transmit path.

**45.2.1.7.3 Receive fault ability (1.8.12)**

When read as a one, bit 1.8.12 indicates that the PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.8.12 indicates that the PMA/PMD does not have the ability to detect a fault condition on the receive path.

**45.2.1.7.4 Transmit fault (1.8.11)**

When read as a one, bit 1.8.11 indicates that the PMA/PMD has detected a fault condition on the transmit path. When read as a zero, bit 1.8.11 indicates that the PMA/PMD has not detected a fault condition on the transmit path. Detection of a fault condition on the transmit path is optional and the ability to detect such a condition is advertised by bit 1.8.13. A PMA/PMD that is unable to detect a fault condition on the transmit path shall return a value of zero for this bit. The description of the transmit fault function for serial PMDs is given in 52.4.8. The description of the transmit fault function for WWDM PMDs is given in 53.4.10. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 1.8.11 is zero.

**45.2.1.7.5 Receive fault (1.8.10)**

When read as a one, bit 1.8.10 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.8.10 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.8.12. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit. The description of the receive fault function for serial PMDs is given in 52.4.9. The description of the receive fault function for WWDM PMDs is given in 53.4.11. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 1.8.10 is zero.

**45.2.1.7.6 10GBASE-CX4 ability (1.8.9)**

When read as a one, bit 1.8.4 indicates that the PMA/PMD is able to support a 10GBASE-CX4 PMA/PMD type. When read as a zero, bit 1.8.4 indicates that the PMA/PMD is not able to support a 10GBASE-CX4 PMA/PMD type.

**45.2.1.7.7 PMD transmit disable ability (1.8.8)**

When read as a one, bit 1.8.8 indicates that the PMD is able to perform the transmit disable function. When read as a zero, bit 1.8.8 indicates that the PMD is not able to perform the transmit disable function. If a PMD is able to perform the transmit disable function, then it is controlled using the PMD transmit disable register.

**45.2.1.7.8 10GBASE-SR ability (1.8.7)**

When read as a one, bit 1.8.7 indicates that the PMA/PMD is able to support a 10GBASE-SR PMA/PMD type. When read as a zero, bit 1.8.7 indicates that the PMA/PMD is not able to support a 10GBASE-SR PMA/PMD type.

**45.2.1.7.9 10GBASE-LR ability (1.8.6)**

When read as a one, bit 1.8.6 indicates that the PMA/PMD is able to support a 10GBASE-LR PMA/PMD type. When read as a zero, bit 1.8.6 indicates that the PMA/PMD is not able to support a 10GBASE-LR PMA/PMD type.

**45.2.1.7.10 10GBASE-ER ability (1.8.5)**

When read as a one, bit 1.8.5 indicates that the PMA/PMD is able to support a 10GBASE-ER PMA/PMD type. When read as a zero, bit 1.8.5 indicates that the PMA/PMD is not able to support a 10GBASE-ER PMA/PMD type.

**45.2.1.7.11 10GBASE-LX4 ability (1.8.4)**

When read as a one, bit 1.8.4 indicates that the PMA/PMD is able to support a 10GBASE-LX4 PMA/PMD type. When read as a zero, bit 1.8.4 indicates that the PMA/PMD is not able to support a 10GBASE-LX4 PMA/PMD type.

**45.2.1.7.12 10GBASE-SW ability (1.8.3)**

When read as a one, bit 1.8.3 indicates that the PMA/PMD is able to support a 10GBASE-SW PMA/PMD type. When read as a zero, bit 1.8.3 indicates that the PMA/PMD is not able to support a 10GBASE-SW PMA/PMD type.

**45.2.1.7.13 10GBASE-LW ability (1.8.2)**

When read as a one, bit 1.8.2 indicates that the PMA/PMD is able to support a 10GBASE-LW PMA/PMD type. When read as a zero, bit 1.8.2 indicates that the PMA/PMD is not able to support a 10GBASE-LW PMA/PMD type.

**45.2.1.7.14 10GBASE-EW ability (1.8.1)**

When read as a one, bit 1.8.1 indicates that the PMA/PMD is able to support a 10GBASE-EW PMA/PMD type. When read as a zero, bit 1.8.1 indicates that the PMA/PMD is not able to support a 10GBASE-EW PMA/PMD type.

**45.2.1.7.15 PMA loopback ability (1.8.0)**

When read as a one, bit 1.8.0 indicates that the PMA is able to perform the loopback function. When read as a zero, bit 1.8.0 indicates that the PMA is not able to perform the loopback function. If a PMA is able to perform the loopback function, then it is controlled using the PMA loopback bit 1.0.0.

**45.2.1.8 10G PMD transmit disable register (Register 1.9)**

The assignment of bits in the 10G PMD transmit disable register is shown in Table 45–9. The transmit disable functionality is optional and a PMD’s ability to perform the transmit disable functionality is advertised in the PMD transmit disable ability bit 1.8.8. A PMD that does not implement the transmit disable functionality shall ignore writes to the 10G PMD transmit disable register and may return a value of zero for all bits. A PMD device that operates using a single wavelength and has implemented the transmit disable function shall use bit 1.9.0 to control the function. Such devices shall ignore writes to bits 1.9.4:1 and return a value of zero for those bits when they are read. The transmit disable function for serial PMDs is described in 52.4.7. The transmit disable function for wide wavelength division multiplexing (WWDM) PMDs is described in 53.4.7.

**Table 45–9—10G PMD transmit disable register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
1.9.15:5	Reserved	Value always 0, writes ignored	R/W
1.9.4	PMD transmit disable 3	1 = Disable output on transmit lane 3 0 = Enable output on transmit lane 3	R/W
1.9.3	PMD transmit disable 2	1 = Disable output on transmit lane 2 0 = Enable output on transmit lane 2	R/W
1.9.2	PMD transmit disable 1	1 = Disable output on transmit lane 1 0 = Enable output on transmit lane 1	R/W
1.9.1	PMD transmit disable 0	1 = Disable output on transmit lane 0 0 = Enable output on transmit lane 0	R/W
1.9.0	Global PMD transmit disable	1 = Disable transmitter output 0 = Enable transmitter output	R/W

<sup>a</sup>R/W = Read/Write

**45.2.1.8.1 PMD transmit disable 3 (1.9.4)**

When bit 1.9.4 is set to a one, the PMD shall disable output on lane 3 of the transmit path. When bit 1.9.4 is set to a zero, the PMD shall enable output on lane 3 of the transmit path.

The default value for bit 1.9.4 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

**45.2.1.8.2 PMD transmit disable 2 (1.9.3)**

When bit 1.9.3 is set to a one, the PMD shall disable output on lane 2 of the transmit path. When bit 1.9.3 is set to a zero, the PMD shall enable output on lane 2 of the transmit path.

The default value for bit 1.9.3 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

**45.2.1.8.3 PMD transmit disable 1 (1.9.2)**

When bit 1.9.2 is set to a one, the PMD shall disable output on lane 1 of the transmit path. When bit 1.9.2 is set to a zero, the PMD shall enable output on lane 1 of the transmit path.

The default value for bit 1.9.2 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

**45.2.1.8.4 PMD transmit disable 0 (1.9.1)**

When bit 1.9.1 is set to a one, the PMD shall disable output on lane 0 of the transmit path. When bit 1.9.1 is set to a zero, the PMD shall enable output on lane 0 of the transmit path.

The default value for bit 1.9.1 is zero.

NOTE—Transmission will not be enabled when this bit is set to a zero unless the global PMD transmit disable bit is also zero.

**45.2.1.8.5 Global PMD transmit disable (1.9.0)**

When bit 1.9.0 is set to a one, the PMD shall disable output on the transmit path. When bit 1.9.0 is set to a zero, the PMD shall enable output on the transmit path.

For single wavelength PMD types, transmission will be disabled when this bit is set to one. When this bit is set to zero, transmission is enabled.

For multiple wavelength PMD types, transmission will be disabled on all lanes when this bit is set to one. When this bit is set to zero, the lanes are individually controlled by their corresponding transmit disable bits 1.9.4:1.

The default value for bit 1.9.0 is zero.

**45.2.1.9 10G PMD receive signal detect register (Register 1.10)**

The assignment of bits in the 10G PMD receive signal detect register is shown in Table 45–10. The 10G PMD receive signal detect register is mandatory. PMD types that use only a single wavelength indicate the status of the receive signal detect using bit 1.10.0 and return a value of zero for bits 1.10.4:1. PMD types that use multiple wavelengths indicate the status of each lane in bits 1.10.4:1 and the logical AND of those bits in bit 1.10.0.

**Table 45–10—10G PMD receive signal detect register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
1.10.15:5	Reserved	Value always 0, writes ignored	RO
1.10.4	PMD receive signal detect 3	1 = Signal detected on receive lane 3 0 = Signal not detected on receive lane 3	RO
1.10.3	PMD receive signal detect 2	1 = Signal detected on receive lane 2 0 = Signal not detected on receive lane 2	RO
1.10.2	PMD receive signal detect 1	1 = Signal detected on receive lane 1 0 = Signal not detected on receive lane 1	RO
1.10.1	PMD receive signal detect 0	1 = Signal detected on receive lane 0 0 = Signal not detected on receive lane 0	RO
1.10.0	Global PMD receive signal detect	1 = Signal detected on receive 0 = Signal not detected on receive	RO

<sup>a</sup>RO = Read Only

**45.2.1.9.1 PMD receive signal detect 3 (1.10.4)**

When bit 1.10.4 is read as a one, a signal has been detected on lane 3 of the PMD receive path. When bit 1.10.4 is read as a zero, a signal has not been detected on lane 3 of the PMD receive path.

**45.2.1.9.2 PMD receive signal detect 2 (1.10.3)**

When bit 1.10.3 is read as a one, a signal has been detected on lane 2 of the PMD receive path. When bit 1.10.3 is read as a zero, a signal has not been detected on lane 2 of the PMD receive path.

**45.2.1.9.3 PMD receive signal detect 1 (1.10.2)**

When bit 1.10.2 is read as a one, a signal has been detected on lane 1 of the PMD receive path. When bit 1.10.2 is read as a zero, a signal has not been detected on lane 1 of the PMD receive path.

**45.2.1.9.4 PMD receive signal detect 0 (1.10.1)**

When bit 1.10.1 is read as a one, a signal has been detected on lane 0 of the PMD receive path. When bit 1.10.1 is read as a zero, a signal has not been detected on lane 0 of the PMD receive path.

**45.2.1.9.5 Global PMD receive signal detect (1.10.0)**

When bit 1.10.0 is read as a one, a signal has been detected on all the PMD receive paths. When bit 1.10.0 is read as a zero, a signal has not been detected on at least one of the PMD receive paths.

Single wavelength PMD types indicate the status of their receive path signal using this bit.

Multiple wavelength PMD types indicate the global status of the lane-by-lane signal detect indications using this bit. This bit is read as a one when all the lane signal detect indications are one; otherwise, this bit is read as a zero.

**45.2.1.10 PMA/PMD package identifier (Registers 1.14 and 1.15)**

Registers 1.14 and 1.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PMA/PMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PMA/PMD may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the package identifier is specified in 22.2.4.3.1.

**45.2.2 WIS registers**

The assignment of registers in the WIS is shown in Table 45–11. For the WIS octet fields, bit 8 of the corresponding field in the WIS frame maps to the lowest numbered bit of the field in the register.

**Table 45–11—WIS registers**

Register address	Register name
2.0	WIS control 1
2.1	WIS status 1
2.2, 2.3	WIS device identifier
2.4	WIS speed ability
2.5, 2.6	WIS devices in package
2.7	10G WIS control 2
2.8	10G WIS status 2
2.9	10G WIS test-pattern error counter
2.10 through 2.13	Reserved
2.14, 2.15	WIS package identifier
2.16 through 2.32	Reserved
2.33	10G WIS status 3
2.34 through 2.36	Reserved
2.37	10G WIS far end path block error count
2.38	Reserved
2.39 through 2.46	10G WIS J1 transmit
2.47 through 2.54	10G WIS J1 receive

**Table 45–11—WIS registers (continued)**

Register address	Register name
2.55, 2.56	10G WIS far end line BIP errors
2.57, 2.58	10G WIS line BIP errors
2.59	10G WIS path block error count
2.60	10G WIS section BIP error count
2.61 through 2.63	Reserved
2.64 through 2.71	10G WIS J0 transmit
2.72 through 2.79	10G WIS J0 receive
2.80 through 2.32 767	Reserved
2.32 768 through 2.65 535	Vendor specific

**45.2.2.1 WIS control 1 register (Register 2.0)**

The assignment of bits in the WIS control 1 register is shown in Table 45–12. The default value for each bit of the WIS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

**45.2.2.1.1 Reset (2.0.15)**

Resetting a WIS is accomplished by setting bit 2.0.15 to a one. This action shall set all WIS registers to their default states. As a consequence, this action may change the internal state of the WIS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a WIS shall return a value of one in bit 2.0.15 when a reset is in progress and a value of zero otherwise. A WIS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 2.0.15. During a reset, a WIS shall respond to reads from register bits 2.0.15 and 2.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

**45.2.2.1.2 Loopback (2.0.14)**

The WIS shall be placed in a Loopback mode of operation when bit 2.0.14 is set to a one. When bit 2.0.14 is set to a one, the WIS shall ignore all data presented to it by the PMA sublayer. When bit 2.0.14 is set to a one, the WIS shall accept data on the transmit path and return it on the receive path. For 10 Gb/s operation, the detailed behavior of the WIS during loopback is specified in 50.3.9

The default value of bit 2.0.14 is zero.

NOTE—The signal path through the WIS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the WIS circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and

**Table 45–12— WIS control 1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.0.15	Reset	1 = WIS reset 0 = Normal operation	R/W SC
2.0.14	Loopback	1 = Enable Loopback mode 0 = Disable Loopback mode	R/W
2.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
2.0.12	Reserved	Value always 0, writes ignored	R/W
2.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
2.0.10:7	Reserved	Value always 0, writes ignored	R/W
2.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
2.0.5:2	Speed selection	$\begin{matrix} \underline{5} & \underline{4} & \underline{3} & \underline{2} \\ 1 & x & x & x = \text{Reserved} \\ x & 1 & x & x = \text{Reserved} \\ x & x & 1 & x = \text{Reserved} \\ 0 & 0 & 0 & 1 = \text{Reserved} \\ 0 & 0 & 0 & 0 = 10 \text{ Gb/s} \end{matrix}$	R/W
2.0.1:0	Reserved	Value always 0, writes ignored	R/W

<sup>a</sup>R/W = Read/Write, SC = Self Clearing

reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

**45.2.2.1.3 Low power (2.0.11)**

A WIS may be placed into a low-power mode by setting bit 2.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the WIS. The behavior of the WIS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 2.0.11 is zero.

**45.2.2.1.4 Speed selection (2.0.13, 2.0.6, and 2.0.5:2)**

Speed selection bits 2.0.13 and 2.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the WIS may be selected using bits 5 through 2. The speed abilities of the WIS are advertised in the WIS speed ability register. A WIS may ignore writes to the WIS speed selection bits that select speeds it has not advertised in the WIS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.



The WIS speed selection defaults to a supported ability.

**45.2.2.2 WIS status 1 register (Register 2.1)**

The assignment of bits in the WIS status 1 register is shown in Table 45–13. All the bits in the WIS status 1 register are read only; a write to the WIS status 1 register shall have no effect.

**Table 45–13—WIS status 1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.1.15:8	Reserved	Ignore when read	RO
2.1.7	Fault	1 = Fault condition 0 = No fault condition	RO/LH
2.1.6:3	Reserved	Ignore when read	RO
2.1.2	Link status	1 = WIS link up 0 = WIS link down	RO/LL
2.1.1	Low-power ability	1 = WIS supports low-power mode 0 = WIS does not support low-power mode	RO
2.1.1:0	Reserved	Ignore when read	RO

<sup>a</sup>RO = Read Only, LH = Latching High, LL = Latching Low

**45.2.2.2.1 Fault (2.1.7)**

When read as a one, bit 2.1.7 indicates that the WIS has detected a fault condition. When read as a zero, bit 2.1.7 indicates that the WIS has not detected a fault condition. The fault bit shall be implemented with latching high behavior.

The default value of bit 2.1.7 is zero.

**45.2.2.2.2 Link status (2.1.2)**

When read as a one, bit 2.1.2 indicates that the WIS receive link is up. When read as a zero, bit 2.1.2 indicates that the WIS receive link is down. The link status bit shall be implemented with latching low behavior.

**45.2.2.2.3 Low-power ability (2.1.1)**

When read as a one, bit 2.1.1 indicates that the WIS supports the low-power feature. When read as a zero, bit 2.1.1 indicates that the WIS does not support the low-power feature. If a WIS supports the low-power feature, then it is controlled using the low-power bit in the WIS control register.

**45.2.2.3 WIS device identifier (Registers 2.2 and 2.3)**

Registers 2.2 and 2.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of WIS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A WIS may return a value of zero in each of the 32 bits of the WIS device identifier.

The format of the WIS device identifier is specified in 22.2.4.3.1.

**45.2.2.4 WIS speed ability (Register 2.4)**

The assignment of bits in the WIS speed ability register is shown in Table 45–14.

**Table 45–14— WIS speed ability register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
2.4.0	10G capable	1 = WIS is capable of operating at 10 Gb/s 0 = WIS is not capable of operating at 10 Gb/s	RO

<sup>a</sup>RO = Read Only

**45.2.2.4.1 10G capable (2.4.0)**

When read as a one, bit 2.4.0 indicates that the WIS is able to operate at a data rate of 10 Gb/s (9.58 Gb/s payload rate). When read as a zero, bit 2.4.0 indicates that the WIS is not able to operate at a data rate of 10 Gb/s (9.58 Gb/s payload rate).

**45.2.2.5 WIS devices in package (Registers 2.5 and 2.6)**

The assignment of bits in the WIS devices in package registers is shown in Table 45–15.

When read as a one, a bit in the WIS devices in package registers indicates that the associated MMD has been instantiated within the same package as other MMDs whose associated bits have been set to a one within the WIS devices in package registers. Bit 2.5.0 is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

**45.2.2.6 10G WIS control 2 register (Register 2.7)**

The assignment of bits in the 10G WIS control 2 register is shown in Table 45–16. The default value for each bit of the 10G WIS control 2 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

**45.2.2.6.1 PRBS31 receive test-pattern enable (2.7.5)**

If the WIS supports the optional PRBS31 (see 49.2.8) pattern testing advertised in bit 2.8.1 and the mandatory receive test-pattern enable bit (2.7.2) is not one, setting bit 2.7.5 to a one shall set the receive path of the WIS into the PRBS31 test-pattern mode. Setting bit 2.7.5 to a zero shall disable the PRBS31 test-pattern mode on the receive path of the WIS. The behavior of the WIS when in PRBS31 test-pattern mode is specified in 50.3.8.2

**45.2.2.6.2 PRBS31 transmit test-pattern enable (2.7.4)**

If the WIS supports the optional PRBS31 pattern testing advertised in bit 2.8.1 and the mandatory transmit test-pattern enable bit (2.7.1) is not one, then setting bit 2.7.4 to a one shall set the transmit path of the WIS into the PRBS31 test-pattern mode. Setting bit 2.7.4 to a zero shall disable the PRBS31 test-pattern mode on

**Table 45–15— WIS devices in package registers bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
2.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
2.6.13:0	Reserved	Ignore on read	RO
2.5.15:6	Reserved	Ignore on read	RO
2.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
2.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
2.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
2.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
2.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
2.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

<sup>a</sup>RO = Read Only

**Table 45–16—10G WIS control 2 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.7.15:6	Reserved	Value always 0, writes ignored	R/W
2.7.5	PRBS31 receive test-pattern enable	1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path	R/W
2.7.4	PRBS31 transmit test-pattern enable	1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path	R/W
2.7.3	Test-pattern selection	1 = Select square wave test pattern 0 = Select mixed-frequency test pattern	R/W
2.7.2	Receive test-pattern enable	1 = Enable test-pattern mode on the receive path 0 = Disable test-pattern mode on the receive path	R/W
2.7.1	Transmit test-pattern enable	1 = Enable test-pattern mode on the transmit path 0 = Disable test-pattern mode on the transmit path	R/W
2.7.0	PCS type selection	1 = Select 10GBASE-W PCS type 0 = Select 10GBASE-R PCS type	R/W

1       <sup>a</sup>R/W = Read/Write  
2  
3

4       the transmit path of the WIS. The behavior of the WIS when in PRBS31 test-pattern mode is specified in  
5       50.3.8.2  
6

#### 7       **45.2.2.6.3 Test-pattern selection (2.7.3)** 8

9       Bit 2.7.3 controls the type of pattern sent by the transmitter when in test-pattern mode. Setting bit 2.7.3 to a  
10       one shall select the square wave test pattern. Setting bit 2.7.3 to a zero shall select the mixed-frequency test  
11       pattern. The details of the test patterns are specified in Clause 50.  
12

#### 13       **45.2.2.6.4 Receive test-pattern enable (2.7.2)** 14

15       Setting bit 2.7.2 to a one shall set the receive path of the WIS into the test-pattern mode. Setting bit 2.7.2 to  
16       a zero shall disable the test-pattern mode on the receive path of the WIS. The behavior of the WIS when in  
17       test-pattern mode is specified in Clause 50.  
18

#### 19       **45.2.2.6.5 Transmit test-pattern enable (2.7.1)** 20

21       Setting bit 2.7.1 to a one shall set the transmit path of the WIS into the test-pattern mode. Setting bit 2.7.1 to  
22       a zero shall disable the test-pattern mode on the transmit path of the WIS. The behavior of the WIS when in  
23       test-pattern mode is specified in Clause 50.  
24

#### 25       **45.2.2.6.6 PCS type selection (2.7.0)** 26

27       Setting bit 2.7.0 to a one shall enable the 10GBASE-W logic and set the speed of the WIS-PMA interface to  
28       9.95328 Gb/s. Setting bit 2.7.0 to a zero shall disable the 10GBASE-W logic, set the speed of the PCS-PMA  
29       interface to 10.3125 Gb/s and bypass the data around the 10GBASE-W logic. A WIS that is only capable of  
30       supporting 10GBASE-W operation and is unable to support 10GBASE-R operation shall ignore values writ-  
31       ten to this bit and shall return a value of one when read. It is the responsibility of the STA entity to ensure  
32       that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.  
33

#### 34       **45.2.2.7 10G WIS status 2 register (Register 2.8)** 35

36       The assignment of bits in the 10G WIS status 2 register is shown in Table 45–17. All the bits in the 10G WIS  
37       status 2 register are read only; a write to the 10G WIS status 2 register shall have no effect.  
38

#### 39       **45.2.2.7.1 Device present (2.8.15:14)** 40

41       When read as <10>, bits 2.8.15:14 indicate that a device is present and responding at this register address.  
42       When read as anything other than <10>, bits 2.8.15:14 indicate that no device is present at this address or  
43       that the device is not functioning properly.  
44

#### 45       **45.2.2.7.2 PRBS31 pattern testing ability (2.8.1)** 46

47       When read as a one, bit 2.8.1 indicates that the WIS is able to support PRBS31 pattern testing. When read as  
48       a zero, bit 2.8.1 indicates that the WIS is not able to support PRBS31 pattern testing. If the WIS is able to  
49       support PRBS31 pattern testing, then the pattern generation and checking is controlled using bits 2.7.5:4.  
50  
51  
52  
53  
54

**Table 45–17—10G WIS status 2 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>															
2.8.15:14	Device present	<table border="0"> <tr> <td><u>15</u></td> <td><u>14</u></td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>= Device responding at this address</td> </tr> <tr> <td>1</td> <td>1</td> <td>= No device responding at this address</td> </tr> <tr> <td>0</td> <td>1</td> <td>= No device responding at this address</td> </tr> <tr> <td>0</td> <td>0</td> <td>= No device responding at this address</td> </tr> </table>	<u>15</u>	<u>14</u>		1	0	= Device responding at this address	1	1	= No device responding at this address	0	1	= No device responding at this address	0	0	= No device responding at this address	RO
<u>15</u>	<u>14</u>																	
1	0	= Device responding at this address																
1	1	= No device responding at this address																
0	1	= No device responding at this address																
0	0	= No device responding at this address																
2.8.13:2	Reserved	Ignore when read	RO															
2.8.1	PRBS31 pattern testing ability	1 = WIS is able to support PRBS31 pattern testing 0 = WIS is not able to support PRBS31 pattern testing	RO															
2.8.0	10GBASE-R ability	1 = WIS is able to support 10GBASE-R port types 0 = WIS is not able to support 10GBASE-R port types	RO															

<sup>a</sup>RO = Read Only

**45.2.2.7.3 10GBASE-R ability (2.8.0)**

When read as a one, bit 2.8.0 indicates that the WIS is able to bypass the WIS logic and adjust the XSBI interface speed to support 10GBASE-R port types. When read as a zero, bit 2.8.0 indicates that the WIS is not able to bypass the WIS logic and cannot support 10GBASE-R port types.

**45.2.2.8 10G WIS test-pattern error counter register (Register 2.9)**

The assignment of bits in the 10G WIS test-pattern error counter register is shown in Table 45–18. This register is only required when the PRBS31 pattern generation capability is supported.

**Table 45–18—10G WIS test-pattern error counter register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.9.15:0	Test-pattern error counter	Error counter	RO

<sup>a</sup>RO = Read Only

The test-pattern error counter is a sixteen bit counter that contains the number of errors received during a pattern test. These bits shall be reset to all zeros when the test-pattern error counter is read by the management function or upon execution of the WIS reset. These bits shall be held at all ones in the case of overflow. The test-pattern methodology is described in 49.2.8.

**45.2.2.9 WIS package identifier (Registers 2.14 and 2.15)**

Registers 2.14 and 2.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the WIS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A WIS may return a value of zero in each of the 32 bits of the WIS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the WIS package identifier is specified in 22.2.4.3.1.

**45.2.2.10 10G WIS status 3 register (Register 2.33)**

The assignment of bits in the 10G WIS status 3 register is shown in Table 45–19. All the bits in the 10G WIS status 3 register are read only; a write to the 10G WIS status 3 register shall have no effect.

**Table 45–19—10G WIS status 3 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.33.15:12	Reserved	Ignore when read	RO
2.33.11	SEF	Severely errored frame	RO/LH
2.33.10	Far end PLM-P/LCD-P	1 = Far end path label mismatch / Loss of code-group delineation 0 = No far end path label mismatch / Loss of code-group delineation	RO/LH
2.33.9	Far end AIS-P/LOP-P	1 = Far end path alarm indication signal / Path loss of pointer 0 = No far end path alarm indication signal / Path loss of pointer	RO/LH
2.33.8	Reserved	Ignore when read	RO
2.33.7	LOF	1 = Loss of frame flag raised 0 = Loss of frame flag lowered	RO/LH
2.33.6	LOS	1 = Loss of signal flag raised 0 = Loss of signal flag lowered	RO/LH
2.33.5	RDI-L	1 = Line remote defect flag raised 0 = Line remote defect flag lowered	RO/LH
2.33.4	AIS-L	1 = Line alarm indication flag raised 0 = Line alarm indication flag lowered	RO/LH
2.33.3	LCD-P	1 = Path loss of code-group delineation flag raised 0 = Path loss of code-group delineation flag lowered	RO/LH
2.33.2	PLM-P	1 = Path label mismatch flag raised 0 = Path label mismatch flag lowered	RO/LH
2.33.1	AIS-P	1 = Path alarm indication signal raised 0 = Path alarm indication signal lowered	RO/LH
2.33.0	LOP-P	1 = Loss of pointer flag raised 0 = Loss of pointer flag lowered	RO/LH

<sup>a</sup>RO = Read Only, LH = Latching High

**45.2.2.10.1 SEF (2.33.11)**

When read as a one, bit 2.33.11 indicates that the SEF flag has been raised by the WIS. When read as a zero, bit 2.33.11 indicates that the SEF flag is lowered. The SEF bit shall be implemented with latching high behavior.

The SEF functionality implemented by the WIS is described in 50.3.2.5.

**45.2.2.10.2 Far end PLM-P/LCD-P (2.33.10)**

When read as a one, bit 2.33.10 indicates that the far end path label mismatch/loss of code-group delineation flag has been raised. When read as a zero, bit 2.33.10 indicates that the far end path label mismatch/loss of code-group delineation flag is lowered. The far end PLM-P/LCD-P bit shall be implemented with latching high behavior.

The far end path label mismatch/loss of code-group delineation functionality implemented by the WIS is described in 50.3.2.5.

**45.2.2.10.3 Far end AIS-P/LOP-P (2.33.9)**

When read as a one, bit 2.33.9 indicates that the far end path alarm indication signal/path loss of pointer flag has been raised by the WIS. When read as a zero, bit 2.33.9 indicates that the far end path alarm indication signal/path loss of pointer flag is lowered. The far end AIS-P/LOP-P bit shall be implemented with latching high behavior.

The far end path alarm indication signal/path loss of pointer functionality implemented by the WIS is described in 50.3.2.5.

**45.2.2.10.4 LOF (2.33.7)**

When read as a one, bit 2.33.7 indicates that the loss of frame flag has been raised. When read as a zero, bit 2.33.7 indicates that the loss of frame flag is lowered. The LOF bit shall be implemented with latching high behavior.

The LOF functionality implemented by the WIS is described in 50.3.2.5.

**45.2.2.10.5 LOS (2.33.6)**

When read as a one, bit 2.33.6 indicates that the loss of signal flag has been raised. When read as a zero, bit 2.33.6 indicates that the loss of signal flag is lowered. The LOS bit shall be implemented with latching high behavior.

The LOS functionality implemented by the WIS is described in 50.3.2.5.

**45.2.2.10.6 RDI-L (2.33.5)**

When read as a one, bit 2.33.5 indicates that the line remote defect flag has been raised. When read as a zero, bit 2.33.5 indicates that the line remote defect flag is lowered. The RDI-L bit shall be implemented with latching high behavior.

The RDI-L functionality implemented by the WIS is described in 50.3.2.5.

**45.2.2.10.7 AIS-L (2.33.4)**

When read as a one, bit 2.33.4 indicates that the line alarm indication flag has been raised. When read as a zero, bit 2.33.4 indicates that the line alarm indication flag is lowered. The AIS-L bit shall be implemented with latching high behavior.

The AIS-L functionality implemented by the WIS is described in 50.3.2.5.

**45.2.2.10.8 LCD-P (2.33.3)**

When read as a one, bit 2.33.3 indicates that the loss of code-group delineation flag has been raised. When read as a zero, bit 2.33.3 indicates that the loss of code-group delineation flag is lowered. The LCD-P bit shall be implemented with latching high behavior.

The loss of code-group delineation functionality implemented by the WIS is described in 50.3.2.5.

**45.2.2.10.9 PLM-P (2.33.2)**

When read as a one, bit 2.33.2 indicates that the path label mismatch flag has been raised. When read as a zero, bit 2.33.2 indicates that the path label mismatch flag is lowered. The PLM-P bit shall be implemented with latching high behavior.

The PLM-P functionality implemented by the WIS is described in 50.3.2.5.

**45.2.2.10.10 AIS-P (2.33.1)**

When read as a one, bit 2.33.1 indicates that the path alarm indication signal has been raised. When read as a zero, bit 2.33.1 indicates that the path alarm indication signal is lowered. The AIS-P bit shall be implemented with latching high behavior.

The path alarm indication signal functionality implemented by the WIS is described in 50.3.2.5.

**45.2.2.10.11 LOP-P (2.33.0)**

When read as a one, bit 2.33.0 indicates that the loss of pointer flag has been raised. When read as a zero, bit 2.33.0 indicates that the loss of pointer flag is lowered. The LOP-P bit shall be implemented with latching high behavior.

The LOP-P functionality implemented by the WIS is described in 50.3.2.5.

**45.2.2.11 10G WIS far end path block error count (Register 2.37)**

The assignment of bits in the 10G WIS far end path block error count register is shown in Table 45–20.

**Table 45–20—10G WIS far end path block error count register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.37.15:0	Far end path block error count	Far end path block error count	RO

<sup>a</sup>RO = Read Only,



The 10G WIS far end path block error count is incremented by one whenever a far end path block error, defined in Annex 50A, is detected as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

**45.2.2.12 10G WIS J1 transmit (Registers 2.39 through 2.46)**

The assignment of octets in the 10G WIS J1 transmit registers is shown in Table 45–21.

**Table 45–21—10G WIS J1 transmit 0–15 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.46.15:8	J1 transmit 15	Transmitted path trace octet 15	R/W
2.46.7:0	J1 transmit 14	Transmitted path trace octet 14	R/W
2.45.15:8	J1 transmit 13	Transmitted path trace octet 13	R/W
2.45.7:0	J1 transmit 12	Transmitted path trace octet 12	R/W
2.44.15:8	J1 transmit 11	Transmitted path trace octet 11	R/W
2.44.7:0	J1 transmit 10	Transmitted path trace octet 10	R/W
2.43.15:8	J1 transmit 9	Transmitted path trace octet 9	R/W
2.43.7:0	J1 transmit 8	Transmitted path trace octet 8	R/W
2.42.15:8	J1 transmit 7	Transmitted path trace octet 7	R/W
2.42.7:0	J1 transmit 6	Transmitted path trace octet 6	R/W
2.41.15:8	J1 transmit 5	Transmitted path trace octet 5	R/W
2.41.7:0	J1 transmit 4	Transmitted path trace octet 4	R/W
2.40.15:8	J1 transmit 3	Transmitted path trace octet 3	R/W
2.40.7:0	J1 transmit 2	Transmitted path trace octet 2	R/W
2.39.15:8	J1 transmit 1	Transmitted path trace octet 1	R/W
2.39.7:0	J1 transmit 0	Transmitted path trace octet 0	R/W

<sup>a</sup>R/W = Read/Write

The first transmitted path trace octet is J1 transmit 15, which contains the delineation octet. The default value for the J1 transmit 15 octet is 137 (hexadecimal 89). The last transmitted path trace octet is J1 transmit 0. The default value for the J1 transmit 0 through 14 octets is 0. The transmitted path trace is described in 50.3.2.1.

### 45.2.2.13 10G WIS J1 receive (Registers 2.47 through 2.54)

The assignment of octets in the 10G WIS J1 receive registers is shown in Table 45–22.

**Table 45–22—10G WIS J1 receive 0–15 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.54.15:8	J1 receive 15	Received path trace octet 15	RO
2.54.7:0	J1 receive 14	Received path trace octet 14	RO
2.53.15:8	J1 receive 13	Received path trace octet 13	RO
2.53.7:0	J1 receive 12	Received path trace octet 12	RO
2.52.15:8	J1 receive 11	Received path trace octet 11	RO
2.52.7:0	J1 receive 10	Received path trace octet 10	RO
2.51.15:8	J1 receive 9	Received path trace octet 9	RO
2.51.7:0	J1 receive 8	Received path trace octet 8	RO
2.50.15:8	J1 receive 7	Received path trace octet 7	RO
2.50.7:0	J1 receive 6	Received path trace octet 6	RO
2.49.15:8	J1 receive 5	Received path trace octet 5	RO
2.49.7:0	J1 receive 4	Received path trace octet 4	RO
2.48.15:8	J1 receive 3	Received path trace octet 3	RO
2.48.7:0	J1 receive 2	Received path trace octet 2	RO
2.47.15:8	J1 receive 1	Received path trace octet 1	RO
2.47.7:0	J1 receive 0	Received path trace octet 0	RO

<sup>a</sup>RO = Read Only

The first received path trace octet is J1 receive 15. The last received path trace octet is J1 receive 0. The received path trace is described in 50.3.2.4.

**45.2.2.14 10G WIS far end line BIP errors (Registers 2.55 and 2.56)**

The assignment of octets in the 10G WIS far end line BIP errors registers is shown in Table 45–23.

**Table 45–23—10G WIS far end line BIP errors 0–1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.56.15:0	WIS far end line BIP errors 0	Least significant word of the WIS far end line BIP errors counter	RO
2.55.15:0	WIS far end line BIP errors 1	Most significant word of the WIS far end line BIP errors counter	RO

<sup>a</sup>RO = Read Only

The 10G WIS far end line BIP Errors register pair reflects the contents of the far end line BIP errors counter (as described in 50.3.11.3) that is incremented on each WIS frame by the number of far end line BIP errors reported by the far end, as described in 50.3.2.5. Whenever the most significant 16 bit register of the counter (2.55) is read, the 32 bit counter value is latched into the register pair, with the most significant bits appearing in 2.55 and the least significant 16 bits appearing in 2.56, the value being latched before the contents of 2.55 (the most significant 16 bits) are driven on the MDIO interface. A subsequent read from register 2.56 will return the least significant 16 bits of the latched value, but will not change the register contents. Writes to these registers have no effect.

**45.2.2.15 10G WIS line BIP errors (Registers 2.57 and 2.58)**

The assignment of octets in the 10G WIS line BIP errors registers is shown in Table 45–24.

**Table 45–24—10G WIS line BIP errors 0–1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.58.15:0	WIS line BIP errors 0	Least significant word of the WIS line BIP errors counter	RO
2.57.15:0	WIS line BIP errors 1	Most significant word of the WIS line BIP errors counter	RO

<sup>a</sup>RO = Read Only

The 10G WIS line BIP errors register pair reflects the contents of the line BIP errors counter (as described in 50.3.11.3) that is incremented on each WIS frame by the number of line BIP errors detected on the incoming data stream, as described in 50.3.2.5. Whenever the most significant 16 bit register of the counter (2.57) is read, the 32 bit counter value is latched into the register pair, with the most significant bits appearing in 2.57 and the least significant 16 bits appearing in 2.58, the value being latched before the contents of 2.57 (the most significant 16 bits) are driven on the MDIO interface. A subsequent read from register 2.58 will return the least significant 16 bits of the latched value, but will not change the register contents. Writes to these registers have no effect.

**45.2.2.16 10G WIS path block error count (Register 2.59)**

The assignment of bits in the 10G WIS path block error count register is shown in Table 45–25.

**Table 45–25—10G WIS path block error count register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.59.15:0	Path block error count	Path block error counter	RO

<sup>a</sup>RO = Read Only

**45.2.2.16.1 Path block error count (2.59.15:0)**

The path block error count is incremented by one whenever a B3 parity error (defined in Annex 50A) is detected, as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

**45.2.2.17 10G WIS section BIP error count (Register 2.60)**

The assignment of bits in the 10G WIS section BIP error count register is shown in Table 45–26.

**Table 45–26—10G WIS section BIP error count register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.60.15:0	Section BIP error count	Section BIP error count	RO

<sup>a</sup>RO = Read Only

**45.2.2.17.1 Section BIP error count (2.60.15:0)**

The section BIP error count is incremented by the number of section BIP errors detected within each WIS frame, as described in 50.3.2.5. The counter wraps around to zero when it is incremented beyond its maximum value of 65 535. It is cleared to zero when the WIS is reset.

**45.2.2.18 10G WIS J0 transmit (Registers 2.64 through 2.71)**

The assignment of octets in the 10G WIS J0 transmit registers is shown in Table 45–27.

**Table 45–27—10G WIS J0 transmit 0–15 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.71.15:8	J0 transmit 15	Transmitted section trace octet 15	R/W
2.71.7:0	J0 transmit 14	Transmitted section trace octet 14	R/W
2.70.15:8	J0 transmit 13	Transmitted section trace octet 13	R/W
2.70.7:0	J0 transmit 12	Transmitted section trace octet 12	R/W
2.69.15:8	J0 transmit 11	Transmitted section trace octet 11	R/W
2.69.7:0	J0 transmit 10	Transmitted section trace octet 10	R/W
2.68.15:8	J0 transmit 9	Transmitted section trace octet 9	R/W
2.68.7:0	J0 transmit 8	Transmitted section trace octet 8	R/W
2.67.15:8	J0 transmit 7	Transmitted section trace octet 7	R/W
2.67.7:0	J0 transmit 6	Transmitted section trace octet 6	R/W
2.66.15:8	J0 transmit 5	Transmitted section trace octet 5	R/W
2.66.7:0	J0 transmit 4	Transmitted section trace octet 4	R/W
2.65.15:8	J0 transmit 3	Transmitted section trace octet 3	R/W
2.65.7:0	J0 transmit 2	Transmitted section trace octet 2	R/W
2.64.15:8	J0 transmit 1	Transmitted section trace octet 1	R/W
2.64.7:0	J0 transmit 0	Transmitted section trace octet 0	R/W

<sup>a</sup>R/W = Read/Write

The J0 transmit octets allow a receiver to verify its continued connection to the WIS transmitter. The first transmitted section trace octet is J0 transmit 15, which contains the delineation octet. The default value for the J0 transmit 15 octet is 137 (hexadecimal 89). The last transmitted section trace octet is J0 transmit 0. The default value for the J0 transmit 0 through 14 octets is 0. The transmitted section trace is described in 50.3.2.3.

**45.2.2.19 10G WIS J0 receive (Registers 2.72 through 2.79)**

The assignment of octets in the 10G WIS J0 receive registers is shown in Table 45–28.

The first received section trace octet is J0 receive 15. The last received section trace octet is J0 receive 0. The J0 receive octets allow a WIS receiver to verify its continued connection to the intended transmitter. The received section trace is described in 50.3.2.4.

**Table 45–28— 10G WIS J0 receive 0–15 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
2.79.15:8	J0 receive 15	Received section trace octet 15	RO
2.79.7:0	J0 receive 14	Received section trace octet 14	RO
2.78.15:8	J0 receive 13	Received section trace octet 13	RO
2.78.7:0	J0 receive 12	Received section trace octet 12	RO
2.77.15:8	J0 receive 11	Received section trace octet 11	RO
2.77.7:0	J0 receive 10	Received section trace octet 10	RO
2.76.15:8	J0 receive 9	Received section trace octet 9	RO
2.76.7:0	J0 receive 8	Received section trace octet 8	RO
2.75.15:8	J0 receive 7	Received section trace octet 7	RO
2.75.7:0	J0 receive 6	Received section trace octet 6	RO
2.74.15:8	J0 receive 5	Received section trace octet 5	RO
2.74.7:0	J0 receive 4	Received section trace octet 4	RO
2.73.15:8	J0 receive 3	Received section trace octet 3	RO
2.73.7:0	J0 receive 2	Received section trace octet 2	RO
2.72.15:8	J0 receive 1	Received section trace octet 1	RO
2.72.7:0	J0 receive 0	Received section trace octet 0	RO

<sup>a</sup>RO = Read Only

**45.2.3 PCS registers**

The assignment of registers in the PCS is shown in Table 45–29.

**Table 45–29—PCS registers**

Register address	Register name
3.0	PCS control 1
3.1	PCS status 1
3.2, 3.3	PCS device identifier
3.4	PCS speed ability
3.5, 3.6	PCS devices in package
3.7	10G PCS control 2
3.8	10G PCS status 2
3.9 through 3.13	Reserved
3.14, 3.15	PCS package identifier
3.16 through 23	Reserved
3.24	10GBASE-X PCS status
3.25	10GBASE-X PCS test control
3.26 through 31	Reserved
3.32	10GBASE-R PCS status 1
3.33	10GBASE-R PCS status 2
3.34 through 37	10GBASE-R PCS test pattern seed A
3.38 through 41	10GBASE-R PCS test pattern seed B
3.42	10GBASE-R PCS test pattern control
3.43	10GBASE-R PCS test pattern error counter
3.44 through 3.32 767	Reserved
3.32 768 through 3.65 535	Vendor specific

**45.2.3.1 PCS control 1 register (Register 3.0)**

The assignment of bits in the PCS control 1 register is shown in Table 45–30. The default value for each bit of the PCS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

**Table 45–30—PCS control 1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
3.0.15	Reset	1 = PCS reset 0 = Normal operation	R/W SC
3.0.14	Loopback	1 = Enable Loopback mode 0 = Disable Loopback mode	R/W
3.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
3.0.12	Reserved	Value always 0, writes ignored	R/W
3.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
3.0.10:7	Reserved	Value always 0, writes ignored	R/W
3.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
3.0.5:2	Speed selection	<u>5</u> <u>4</u> <u>3</u> <u>2</u> 1 x x x = Reserved x 1 x x = Reserved x x 1 x = Reserved 0 0 0 1 = Reserved 0 0 0 0 = 10 Gb/s	R/W
3.0.1:0	Reserved	Value always 0, writes ignored	R/W

<sup>a</sup>R/W = Read/Write, SC = Self Clearing

**45.2.3.1.1 Reset (3.0.15)**

Resetting a PCS is accomplished by setting bit 3.0.15 to a one. This action shall set all PCS registers to their default states. As a consequence, this action may change the internal state of the PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PCS shall return a value of one in bit 3.0.15 when a reset is in progress and a value of zero otherwise. A PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 3.0.15. During a reset, a PCS shall respond to reads from register bits 3.0.15 and 3.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

**45.2.3.1.2 Loopback (3.0.14)**

The 10GBASE-R PCS shall be placed in a Loopback mode of operation when bit 3.0.14 is set to a one. When bit 3.0.14 is set to a one, the 10GBASE-R PCS shall accept data on the transmit path and return it on the receive path. The specific behavior of the 10GBASE-R PCS during loopback is specified in 49.2. For all other port types when operating at 10 Gb/s, the PCS loopback functionality is not applicable and writes to this bit shall be ignored and reads from this bit shall return a value of zero.

The default value of bit 3.0.14 is zero.



NOTE—The signal path through the PCS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PCS circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

**45.2.3.1.3 Low power (3.0.11)**

A PCS may be placed into a low-power mode by setting bit 3.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PCS. The behavior of the PCS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 3.0.11 is zero.

**45.2.3.1.4 Speed selection (3.0.13, 3.0.6, 3.0.5:2)**

Speed selection bits 3.0.13 and 3.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PCS may be selected using bits 5 through 2. The speed abilities of the PCS are advertised in the PCS speed ability register. A PCS may ignore writes to the PCS speed selection bits that select speeds it has not advertised in the PCS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PCS speed selection defaults to a supported ability.

**45.2.3.2 PCS status 1 register (Register 3.1)**

The assignment of bits in the PCS status 1 register is shown in Table 45–31. All the bits in the PCS status 1 register are read only; a write to the PCS status 1 register shall have no effect.

**Table 45–31—PCS status 1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
3.1.15:8	Reserved	Ignore when read	RO
3.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.1.6:3	Reserved	Ignore when read	RO
3.1.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.1.1	Low-power ability	1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO
3.1.0	Reserved	Ignore when read	RO

<sup>a</sup>RO = Read Only, LL = Latching Low

**45.2.3.2.1 Fault (3.1.7)**

When read as a one, bit 3.1.7 indicates that the PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.1.7 indicates that the PCS has not detected a fault condition. For 10 Gb/s operation, bit 3.1.7 is read as a one when either of the fault bits (3.8.11, 3.8.10) located in register 3.8 are read as a one.

**45.2.3.2.2 PCS receive link status (3.1.2)**

When read as a one, bit 3.1.2 indicates that the PCS receive link is up. When read as a zero, bit 3.1.2 indicates that the PCS receive link is down. When a 10GBASE-R or 10GBASE-W mode of operation is selected for the PCS using the PCS type selection field (3.7.1:0), this bit is a latching low version of bit 3.32.12. When a 10GBASE-X mode of operation is selected for the PCS using the PCS type selection field (3.7.1:0), this bit is a latching low version of bit 3.24.12. The receive link status bit shall be implemented with latching low behavior.

**45.2.3.2.3 Low-power ability (3.1.1)**

When read as a one, bit 3.1.1 indicates that the PCS supports the low-power feature. When read as a zero, bit 3.1.1 indicates that the PCS does not support the low-power feature. If a PCS supports the low-power feature then it is controlled using the low-power bit 3.0.11.

**45.2.3.3 PCS device identifier (Registers 3.2 and 3.3)**

Registers 3.2 and 3.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of PCS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PCS may return a value of zero in each of the 32 bits of the PCS device identifier.

The format of the PCS device identifier is specified in 22.2.4.3.1.

**45.2.3.4 PCS speed ability (Register 3.4)**

The assignment of bits in the PCS speed ability register is shown in Table 45–32.

**Table 45–32—PCS speed ability register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
3.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
3.4.0	10G capable	1 = PCS is capable of operating at 10 Gb/s 0 = PCS is not capable of operating at 10 Gb/s	RO

<sup>a</sup>RO = Read Only

**45.2.3.4.1 10G capable (3.4.0)**

When read as a one, bit 3.4.0 indicates that the PCS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 3.4.0 indicates that the PCS is not able to operate at a data rate of 10 Gb/s.

**45.2.3.5 PCS devices in package (Registers 3.5 and 3.6)**

The assignment of bits in the PCS devices in package registers is shown in Table 45–33.

**Table 45–33—PCS devices in package registers bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
3.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
3.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
3.6.13:0	Reserved	Ignore on read	RO
3.5.15:6	Reserved	Ignore on read	RO
3.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
3.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
3.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
3.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
3.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
3.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

<sup>a</sup>RO = Read Only

When read as a one, a bit in the PCS devices in package registers indicates that the associated MMD has been instantiated within the same package as other MMDs whose associated bits have been set to a one within the PCS devices in package registers. The Clause 22 registers present bit is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

**45.2.3.6 10G PCS control 2 register (Register 3.7)**

The assignment of bits in the 10G PCS control 2 register is shown in Table 45–34. The default value for each bit of the 10G PCS control 2 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

**45.2.3.6.1 PCS type selection (3.7.1:0)**

The PCS type shall be selected using bits 1 through 0. The PCS type abilities of the 10G PCS are advertised in bits 3.8.2:0. A 10G PCS shall ignore writes to the PCS type selection bits that select PCS types it has not advertised in the status register. It is the responsibility of the STA entity to ensure that mutually acceptable

**Table 45–34—10G PCS control 2 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>															
3.7.15:2	Reserved	Value always 0, writes ignored	R/W															
3.7.1:0	PCS type selection	<table border="0"> <tr> <td><u>1</u></td> <td><u>0</u></td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>= Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>= Select 10GBASE-W PCS type</td> </tr> <tr> <td>0</td> <td>1</td> <td>= Select 10GBASE-X PCS type</td> </tr> <tr> <td>0</td> <td>0</td> <td>= Select 10GBASE-R PCS type</td> </tr> </table>	<u>1</u>	<u>0</u>		1	1	= Reserved	1	0	= Select 10GBASE-W PCS type	0	1	= Select 10GBASE-X PCS type	0	0	= Select 10GBASE-R PCS type	R/W
<u>1</u>	<u>0</u>																	
1	1	= Reserved																
1	0	= Select 10GBASE-W PCS type																
0	1	= Select 10GBASE-X PCS type																
0	0	= Select 10GBASE-R PCS type																

<sup>a</sup>R/W = Read/Write

MMD types are applied consistently across all the MMDs on a particular PHY. The PCS type selection defaults to a supported ability.

**45.2.3.7 10G PCS status 2 register (Register 3.8)**

The assignment of bits in the 10G PCS status 2 register is shown in Table 45–35. All the bits in the 10G PCS status 2 register are read only; a write to the 10G PCS status 2 register shall have no effect.

**Table 45–35—10G PCS status 2 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>															
3.8.15:14	Device present	<table border="0"> <tr> <td><u>15</u></td> <td><u>14</u></td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>= Device responding at this address</td> </tr> <tr> <td>1</td> <td>1</td> <td>= No device responding at this address</td> </tr> <tr> <td>0</td> <td>1</td> <td>= No device responding at this address</td> </tr> <tr> <td>0</td> <td>0</td> <td>= No device responding at this address</td> </tr> </table>	<u>15</u>	<u>14</u>		1	0	= Device responding at this address	1	1	= No device responding at this address	0	1	= No device responding at this address	0	0	= No device responding at this address	RO
<u>15</u>	<u>14</u>																	
1	0	= Device responding at this address																
1	1	= No device responding at this address																
0	1	= No device responding at this address																
0	0	= No device responding at this address																
3.8.13:12	Reserved	Ignore when read	RO															
3.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH															
3.8.10	Receive fault	1 = Fault condition on the receive path 0 = No fault condition on the receive path	RO/LH															
3.8.9:3	Reserved	Ignore when read	RO															
3.8.2	10GBASE-W capable	1 = PCS is able to support 10GBASE-W PCS type 0 = PCS is not able to support 10GBASE-W PCS type	RO															
3.8.1	10GBASE-X capable	1 = PCS is able to support 10GBASE-X PCS type 0 = PCS is not able to support 10GBASE-X PCS type	RO															
3.8.0	10GBASE-R capable	1 = PCS is able to support 10GBASE-R PCS types 0 = PCS is not able to support 10GBASE-R PCS types	RO															

<sup>a</sup>RO = Read Only, LH = Latching High

**45.2.3.7.1 Device present (3.8.15:14)**

When read as <10>, bits 3.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 3.8.15:14 indicate that no device is present at this address or that the device is not functioning properly.

**45.2.3.7.2 Transmit fault (3.8.11)**

When read as a one, bit 3.8.11 indicates that the PCS has detected a fault condition on the transmit path. When read as a zero, bit 3.8.11 indicates that the PCS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

The default value of bit 3.8.11 is zero.

**45.2.3.7.3 Receive fault (3.8.10)**

When read as a one, bit 3.8.10 indicates that the PCS has detected a fault condition on the receive path. When read as a zero, bit 3.8.10 indicates that the PCS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 3.8.10 is zero.

**45.2.3.7.4 10GBASE-W capable (3.8.2)**

When read as a one, bit 3.8.2 indicates that the 64B/66B PCS is able to support operation in a 10GBASE-W PHY (that is, supports operation with a WIS). When read as a zero, bit 3.8.2 indicates that the 64B/66B PCS is not able to support operation with a WIS in a 10GBASE-W PHY.

NOTE—This bit does not indicate that the PCS is performing the functionality contained in the WIS. This bit indicates whether the 64B/66B PCS would be able to support a WIS if it were to be attached.

**45.2.3.7.5 10GBASE-X capable (3.8.1)**

When read as a one, bit 3.8.1 indicates that the PCS is able to support the 10GBASE-X PCS type. When read as a zero, bit 3.8.1 indicates that the PCS is not able to support the 10GBASE-X PCS type.

**45.2.3.7.6 10GBASE-R capable (3.8.0)**

When read as a one, bit 3.8.0 indicates that the PCS is able to support operation in a 10GBASE-R PHY. When read as a zero, bit 3.8.0 indicates that the PCS is not able to support operation in a 10GBASE-R PHY.

**45.2.3.8 PCS package identifier (Registers 3.14 and 3.15)**

Registers 3.14 and 3.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PCS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PCS may return a value of zero in each of the 32 bits of the PCS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the package identifier is specified in 22.2.4.3.1.

**45.2.3.9 10GBASE-X PCS status register (Register 3.24)**

The assignment of bits in the 10GBASE-X PCS status register is shown in Table 45–36. All the bits in the 10GBASE-X PCS status register are read only; a write to the 10GBASE-X PCS status register shall have no effect. A PCS device that does not implement 10GBASE-X shall return a zero for all bits in the 10GBASE-X PCS status register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits.

**Table 45–36—10GBASE-X PCS status register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
3.24.15:13	Reserved	Ignore when read	RO
3.24.12	10GBASE-X lane alignment status	1 = 10GBASE-X PCS receive lanes aligned 0 = 10GBASE-X PCS receive lanes not aligned	RO
3.24.11	Pattern testing ability	1 = 10GBASE-X PCS is able to generate test patterns 0 = 10GBASE-X PCS is not able to generate test patterns	RO
3.24.10:4	Reserved	Ignore when read	RO
3.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
3.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
3.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
3.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

<sup>a</sup>RO = Read Only

**45.2.3.9.1 10GBASE-X receive lane alignment status (3.24.12)**

When read as a one, bit 3.24.12 indicates that the 10GBASE-X PCS has synchronized and aligned all four receive lanes. When read as a zero, bit 3.24.12 indicates that the 10GBASE-X PCS has not synchronized and aligned all four receive lanes.

**45.2.3.9.2 Pattern testing ability (3.24.11)**

When read as a one, bit 3.24.11 indicates that the 10GBASE-X PCS is able to generate test patterns. When read as a zero, bit 3.24.11 indicates that the 10GBASE-X PCS is not able to generate test patterns. If the 10GBASE-X PCS is able to generate test patterns, then the functionality is controlled using the transmit test-pattern enable bit in register 3.25.

**45.2.3.9.3 Lane 3 sync (3.24.3)**

When read as a one, bit 3.24.3 indicates that the 10GBASE-X PCS receive lane 3 is synchronized. When read as a zero, bit 3.24.3 indicates that the 10GBASE-X PCS receive lane 3 is not synchronized.

**45.2.3.9.4 Lane 2 sync (3.24.2)**

When read as a one, bit 3.24.2 indicates that the 10GBASE-X PCS receive lane 2 is synchronized. When read as a zero, bit 3.24.2 indicates that the 10GBASE-X PCS receive lane 2 is not synchronized.

**45.2.3.9.5 Lane 1 sync (3.24.1)**

When read as a one, bit 3.24.1 indicates that the 10GBASE-X PCS receive lane 1 is synchronized. When read as a zero, bit 3.24.1 indicates that the 10GBASE-X PCS receive lane 1 is not synchronized.

**45.2.3.9.6 Lane 0 sync (3.24.0)**

When read as a one, bit 3.24.0 indicates that the 10GBASE-X PCS receive lane 0 is synchronized. When read as a zero, bit 3.24.0 indicates that the 10GBASE-X PCS receive lane 0 is not synchronized.

**45.2.3.10 10GBASE-X PCS test control register (Register 3.25)**

The assignment of bits in the 10GBASE-X PCS test control register is shown in Table 45–36. The default value for each bit of the 10GBASE-X PCS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

**Table 45–37—10GBASE-X PCS test control register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>												
3.25.15:3	Reserved	Value always 0, writes ignored	R/W												
3.25.2	Transmit test-pattern enable	1 = Transmit test pattern enabled 0 = Transmit test pattern not enabled	R/W												
3.25.1:0	Test pattern select	<table border="0"> <tr> <td><math>\frac{1}{1}</math></td> <td><math>\frac{0}{1}</math></td> <td>= Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>= Mixed-frequency test pattern</td> </tr> <tr> <td>0</td> <td>1</td> <td>= Low-frequency test pattern</td> </tr> <tr> <td>0</td> <td>0</td> <td>= High-frequency test pattern</td> </tr> </table>	$\frac{1}{1}$	$\frac{0}{1}$	= Reserved	1	0	= Mixed-frequency test pattern	0	1	= Low-frequency test pattern	0	0	= High-frequency test pattern	R/W
$\frac{1}{1}$	$\frac{0}{1}$	= Reserved													
1	0	= Mixed-frequency test pattern													
0	1	= Low-frequency test pattern													
0	0	= High-frequency test pattern													

<sup>a</sup>R/W = Read/Write

**45.2.3.10.1 10GBASE-X test-pattern enable (3.25.2)**

When bit 3.25.2 is set to a one, pattern testing is enabled on the transmit path. When bit 3.25.2 is set to a zero, pattern testing is disabled on the transmit path. Pattern testing is optional, and the ability of the 10GBASE-X PCS to generate test patterns is advertised by the pattern testing ability bit in register 3.24. A 10GBASE-X PCS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 3.25.2 is zero.

**45.2.3.10.2 10GBASE-X test-pattern select (3.25.1:0)**

The test pattern to be used when pattern testing is enabled using bit 3.25.2 is selected using bits 3.25.1:0. When bits 3.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 3.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 3.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

**45.2.3.11 10GBASE-R PCS status 1 register (Register 3.32)**

The assignment of bits in the 10GBASE-R PCS status 1 register is shown in Table 45–38. All the bits in the 10GBASE-R PCS status 1 register are read only; a write to the 10GBASE-R PCS status 1 register shall have no effect. A PCS device that does not implement 10GBASE-R shall return a zero for all bits in the 10GBASE-R PCS status 1 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.32 are undefined when the 10GBASE-R PCS is operating in seed test-pattern mode or PRBS31 test-pattern mode.

**Table 45–38—10GBASE-R PCS status 1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
3.32.15:13	Reserved	Ignore when read	RO
3.32.12	10GBASE-R receive link status	1 = 10GBASE-R PCS receive link up 0 = 10GBASE-R PCS receive link down	RO
3.32.11:3	Reserved	Ignore when read	RO
3.32.2	PRBS31 pattern testing ability	1 = PCS is able to support PRBS31 pattern testing 0 = PCS is not able to support PRBS31 pattern testing	RO
3.32.1	10GBASE-R PCS high BER	1 = 10GBASE-R PCS reporting a high BER 0 = 10GBASE-R PCS not reporting a high BER	RO
3.32.0	10GBASE-R PCS block lock	1 = 10GBASE-R PCS locked to received blocks 0 = 10GBASE-R PCS not locked to received blocks	RO

<sup>a</sup>RO = Read Only

**45.2.3.11.1 10GBASE-R receive link status (3.32.12)**

When read as a one, bit 3.32.12 indicates that the PCS is in a fully operational state. When read as a zero, bit 3.32.12 indicates that the PCS is not fully operational. This bit is a reflection of the state of the PCS\_status variable defined in 49.2.14.1.

**45.2.3.11.2 PRBS31 pattern testing ability (3.32.2)**

When read as a one, bit 3.32.2 indicates that the PCS is able to support PRBS31 pattern testing. When read as a zero, bit 3.32.2 indicates that the PCS is not able to support PRBS31 pattern testing. If the PCS is able to support PRBS31 pattern testing then the pattern generation and checking is controlled using bits 3.42.5:4.

**45.2.3.11.3 10GBASE-R PCS high BER (3.32.1)**

When read as a one, bit 3.32.1 indicates that the 64B/66B receiver is detecting a BER of  $\geq 10^{-4}$ . When read as a zero, bit 3.32.1 indicates that the 64B/66B receiver is detecting a BER of  $< 10^{-4}$ . This bit is a direct reflection of the state of the hi\_ber variable in the 64B/66B state machine and is defined in 49.2.13.2.2.



**45.2.3.11.4 10GBASE-R PCS block lock (3.32.0)**

When read as a one, bit 3.32.0 indicates that the 64B/66B receiver has block lock. When read as a zero, bit 3.32.0 indicates that the 64B/66B receiver has not got block lock. This bit is a direct reflection of the state of the block\_lock variable in the 64B/66B state machine and is defined in 49.2.13.2.2.

**45.2.3.12 10GBASE-R PCS status 2 register (Register 3.33)**

The assignment of bits in the 10GBASE-R PCS status 2 register is shown in Table 45–39. All the bits in the 10GBASE-R PCS status 2 register are read only; a write to the 10GBASE-R PCS status 2 register shall have no effect. A PCS device which does not implement 10GBASE-R shall return a zero for all bits in the 10GBASE-R PCS status 2 register. It is the responsibility of the STA management entity to ensure that a port type is supported by all MMDs before interrogating any of its status bits. The contents of register 3.33 are undefined when the 10GBASE-R PCS is operating in seed test-pattern mode or PRBS31 test-pattern mode.

**Table 45–39—10GBASE-R PCS status 2 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
3.33.15	Latched block lock	1 = 10GBASE-R PCS has block lock 0 = 10GBASE-R PCS does not have block lock	RO/LL
3.33.14	Latched high BER	1 = 10GBASE-R PCS has reported a high BER 0 = 10GBASE-R PCS has not reported a high BER	RO/LH
3.33.13:8	BER	BER counter	RO/NR
3.33.7:0	Errored blocks	Errored blocks counter	RO/NR

<sup>a</sup>RO = Read Only, LL = Latching Low, LH = Latching High, NR = Non Roll-over

**45.2.3.12.1 Latched block lock (3.33.15)**

When read as a one, bit 3.33.15 indicates that the 10GBASE-R PCS has achieved block lock. When read as a zero, bit 3.33.15 indicates that the 10GBASE-R PCS has lost block lock.

The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 10GBASE-R PCS block lock status bit (3.32.0).

**45.2.3.12.2 Latched high BER (3.33.14)**

When read as a one, bit 3.33.14 indicates that the 10GBASE-R PCS has detected a high BER. When read as a zero, bit 3.33.14 indicates that the 10GBASE-R PCS has not detected a high BER.

The latched high BER bit shall be implemented with latching high behavior.

This bit is a latching high version of the 10GBASE-R PCS high BER status bit (3.32.1).

**45.2.3.12.3 BER(3.33.13:8)**

The BER counter is a six bit count as defined by the ber\_count variable in 49.2.14.2. These bits shall be reset to all zeros when the BER count is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow.

**45.2.3.12.4 Errored blocks (3.33.7:0)**

The errored blocks counter is an eight bit count defined by the errored\_block\_count counter specified in 49.2.14.2. These bits shall be reset to all zeros when the errored blocks count is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow.

**45.2.3.13 10GBASE-R PCS test pattern seed A (Registers 3.34 through 3.37)**

The assignment of bits in the 10GBASE-R PCS test pattern seed A registers is shown in Table 45–40. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. For each seed register, seed bits are assigned to register bits in order with the lowest numbered seed bit for that register being assigned to register bit 0.

**Table 45–40—10GBASE-R PCS test pattern seed A 0-3 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
3.37.15:10	Reserved	Value always 0, writes ignored	R/W
3.37.9:0	Test pattern seed A 3	Test pattern seed A bits 48-57	R/W
3.36.15:0	Test pattern seed A 2	Test pattern seed A bits 32-47	R/W
3.35.15:0	Test pattern seed A 1	Test pattern seed A bits 16-31	R/W
3.34.15:0	Test pattern seed A 0	Test pattern seed A bits 0-15	R/W

<sup>a</sup>R/W = Read/Write

The A seed for the pseudo random test pattern is held in registers 3.34 through 3.37. The test-pattern methodology is described in 49.2.8.

**45.2.3.14 10GBASE-R PCS test pattern seed B (Registers 3.38 through 3.41)**

The assignment of bits in the 10GBASE-R PCS test pattern seed B registers is shown in Table 45–41. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. For each seed register, seed bits are assigned to register bits in order with the lowest numbered seed bit for that register being assigned to register bit 0.

The B seed for the pseudo random test pattern is held in registers 3.38 through 3.41. The test-pattern methodology is described in 49.2.8.

**Table 45–41—10GBASE-R PCS test pattern seed B 0-3 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
3.41.15:10	Reserved	Value always 0, writes ignored	R/W
3.41.9:0	Test pattern seed B 3	Test pattern seed B bits 48-57	R/W
3.40.15:0	Test pattern seed B 2	Test pattern seed B bits 32-47	R/W
3.39.15:0	Test pattern seed B 1	Test pattern seed B bits 16-31	R/W
3.38.15:0	Test pattern seed B 0	Test pattern seed B bits 0-15	R/W

<sup>a</sup>R/W = Read/Write

**45.2.3.15 10GBASE-R PCS test-pattern control register (Register 3.42)**

The assignment of bits in the 10GBASE-R PCS test-pattern control register is shown in Table 45–42. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode or may function as defined for 10GBASE-R. The test-pattern methodology is described in 49.2.8.

**Table 45–42—10GBASE-R PCS test-pattern control register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
3.42.15:6	Reserved	Value always 0, writes ignored	R/W
3.42.5	PRBS31 receive test-pattern enable	1 = Enable PRBS31 test-pattern mode on the receive path 0 = Disable PRBS31 test-pattern mode on the receive path	R/W
3.42.4	PRBS31 transmit test-pattern enable	1 = Enable PRBS31 test-pattern mode on the transmit path 0 = Disable PRBS31 test-pattern mode on the transmit path	R/W
3.42.3	Transmit test-pattern enable	1 = Enable transmit test pattern 0 = Disable transmit test pattern	R/W
3.42.2	Receive test-pattern enable	1 = Enable receive test-pattern testing 0 = Disable receive test-pattern testing	R/W
3.42.1	Test-pattern select	1 = Square wave test pattern 0 = Pseudo random test pattern	R/W
3.42.0	Data pattern select	1 = Zeros data pattern 0 = LF data pattern	R/W

<sup>a</sup>R/W = Read/Write

**45.2.3.15.1 PRBS31 receive test-pattern enable (3.42.5)**

If the PCS supports the optional PRBS31 pattern testing advertised in bit 3.32.2 and the mandatory receive test-pattern enable bit (3.42.2) is not one, setting bit 3.32.2 to a one shall set the receive path of the PCS into

the PRBS31 test-pattern mode. The number of errors received during a PRBS31 pattern test are recorded in register 3.43. Setting bit 3.32.2 to a zero shall disable the PRBS31 test-pattern mode on the receive path of the PCS. The behavior of the PCS when in PRBS31 test-pattern mode is specified in Clause 49.

**45.2.3.15.2 PRBS31 transmit test-pattern enable (3.42.4)**

If the PCS supports the optional PRBS31 pattern testing advertised in bit 3.32.2 and the mandatory transmit test-pattern enable bit (3.42.3) is not one, then setting bit 3.42.4 to a one shall set the transmit path of the PCS into the PRBS31 test-pattern mode. Setting bit 3.42.4 to a zero shall disable the PRBS31 test-pattern mode on the transmit path of the PCS. The behavior of the PCS when in PRBS31 test-pattern mode is specified in Clause 49.

**45.2.3.15.3 Transmit test-pattern enable (3.42.3)**

When bit 3.42.3 is set to a one, pattern testing is enabled on the transmit path. When bit 3.42.3 is set to a zero, pattern testing is disabled on the transmit path.

The default value for bit 3.42.3 is zero.

**45.2.3.15.4 Receive test-pattern enable (3.42.2)**

When bit 3.42.2 is set to a one, pattern testing is enabled on the receive path. When bit 3.42.2 is set to a zero, pattern testing is disabled on the receive path.

The default value for bit 3.42.2 is zero.

**45.2.3.15.5 Test-pattern select (3.42.1)**

When bit 3.42.1 is set to a one, the square wave test pattern is used for pattern testing. When bit 3.42.1 is set to a zero, the pseudo random test pattern is used for pattern testing.

The default value for bit 3.42.1 is zero.

**45.2.3.15.6 Data pattern select (3.42.0)**

When bit 3.42.0 is set to a one, the zeros data pattern is used for pattern testing. When bit 3.42.0 is set to a zero, the LF data pattern is used for pattern testing.

The default value for bit 3.42.1 is zero.

**45.2.3.16 10GBASE-R PCS test-pattern error counter register (Register 3.43)**

The assignment of bits in the 10GBASE-R PCS test-pattern error counter register is shown in Table 45–43. This register is only required when the 10GBASE-R capability is supported. If both 10GBASE-R and 10GBASE-W capability is supported, then this register may either ignore writes and return zeros for reads when in 10GBASE-W mode, or may function as defined for 10GBASE-R.

**Table 45–43—10GBASE-R PCS test-pattern error counter register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
3.43.15:0	Test-pattern error counter	Error counter	RO

<sup>a</sup>RO = Read Only

The test-pattern error counter is a sixteen bit counter that contains the number of errors received during a pattern test. These bits shall be reset to all zeros when the test-pattern error counter is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow. The test-pattern methodology is described in 49.2.12. This counter will count either block errors or bit errors dependent on the test mode (see 49.2.12).

**45.2.4 PHY XS registers**

The assignment of registers in the PHY XS is shown in Table 45–44.

**Table 45–44—PHY XS registers**

Register address	Register name
4.0	PHY XS control 1
4.1	PHY XS status 1
4.2, 4.3	PHY XS device identifier
4.4	PHY XS speed ability
4.5, 4.6	PHY XS devices in package
4.7	Reserved
4.8	PHY XS status 2
4.9 through 4.13	Reserved
4.14, 4.15	PHY XS package identifier
4.16 through 4.23	Reserved
4.24	10G PHY XGXS lane status
4.25	10G PHY XGXS test control
4.26 through 4.32 767	Reserved
4.32 768 through 4.65 535	Vendor specific

**45.2.4.1 PHY XS control 1 register (Register 4.0)**

The assignment of bits in the PHY XS control 1 register is shown in Table 45–45. The default value for each bit of the PHY XS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

**45.2.4.1.1 Reset (4.0.15)**

Resetting a PHY XS is accomplished by setting bit 4.0.15 to a one. This action shall set all PHY XS registers to their default states. As a consequence, this action may change the internal state of the PHY XS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the

**Table 45–45—PHY XS control 1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
4.0.15	Reset	1 = PHY XS reset 0 = Normal operation	R/W SC
4.0.14	Loopback	1 = Enable Loopback mode 0 = Disable Loopback mode	R/W
4.0.13	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
4.0.12	Reserved	Value always 0, writes ignored	R/W
4.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
4.0.10:7	Reserved	Value always 0, writes ignored	R/W
4.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
4.0.5:2	Speed selection	$\begin{matrix} \underline{5} & \underline{4} & \underline{3} & \underline{2} \\ 1 & x & x & x = \text{Reserved} \\ x & 1 & x & x = \text{Reserved} \\ x & x & 1 & x = \text{Reserved} \\ 0 & 0 & 0 & 1 = \text{Reserved} \\ 0 & 0 & 0 & 0 = 10 \text{ Gb/s} \end{matrix}$	R/W
4.0.1:0	Reserved	Value always 0, writes ignored	R/W

<sup>a</sup>R/W = Read/Write, SC = Self Clearing

same package. This bit is self-clearing, and a PHY XS shall return a value of one in bit 4.0.15 when a reset is in progress and a value of zero otherwise. A PHY XS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 4.0.15. During a reset, a PHY XS shall respond to reads from register bits 4.0.15 and 4.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

**45.2.4.1.2 Loopback (4.0.14)**

The PHY XS shall be placed in a Loopback mode of operation when bit 4.0.14 is set to a one. When bit 4.0.14 is set to a one, the PHY XS shall accept data on the receive path and return it on the transmit path. The direction of the loopback path for the PHY XS is opposite to all other MMD loopbacks.

The loopback function is optional. A device’s ability to perform the loopback function is advertised in the loopback ability bit of the related speed-dependent status register. A PHY XS that is unable to perform the loopback function shall ignore writes to this bit and return a value of zero when read. For 10 Gb/s operation, the loopback functionality is detailed in 48.3.3 and the loopback ability bit is specified in the 10G PHY XGXS Lane status register.

The default value of bit 4.0.14 is zero.

NOTE—The signal path through the PHY XS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the PHY XS circuitry as is practical. The intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

**45.2.4.1.3 Low power (4.0.11)**

A PHY XS may be placed into a low-power mode by setting bit 4.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PHY XS. The behavior of the PHY XS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 4.0.11 is zero.

**45.2.4.1.4 Speed selection (4.0.13, 4.0.6, 4.0.5:2)**

Speed selection bits 4.0.13 and 4.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the PHY XS may be selected using bits 5 through 2. The speed abilities of the PHY XS are advertised in the PHY XS speed ability register. A PHY XS may ignore writes to the PHY XS speed selection bits that select speeds it has not advertised in the PHY XS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The PHY XS speed selection defaults to a supported ability.

**45.2.4.2 PHY XS status 1 register (Register 4.1)**

The assignment of bits in the PHY XS status 1 register is shown in Table 45–46. All the bits in the PHY XS status 1 register are read only; a write to the PHY XS status 1 register shall have no effect.

**Table 45–46—PHY XS status 1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
4.1.15:8	Reserved	Ignore when read	RO
4.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
4.1.6:3	Reserved	Ignore when read	RO
4.1.2	PHY XS transmit link status	1 = The PHY XS transmit link is up 0 = The PHY XS transmit link is down	RO/LL
4.1.1	Low-power ability	1 = PHY XS supports low-power mode 0 = PHY XS does not support low-power mode	RO
4.1.0	Reserved	Ignore when read	RO

<sup>a</sup>RO = Read Only, LL = Latching Low

**45.2.4.2.1 Fault (4.1.7)**

When read as a one, bit 4.1.7 indicates that the PHY XS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 4.1.7 indicates that the PHY XS has not detected a fault condition. Bit 4.1.7 is set to a one when either of the fault bits (4.8.11, 4.8.10) located in register 4.8 are set to a one.

**45.2.4.2.2 PHY XS transmit link status (4.1.2)**

When read as a one, bit 4.1.2 indicates that the PHY XS transmit link is aligned. When read as a zero, bit 4.1.2 indicates that the PHY XS transmit link is not aligned. The transmit link status bit shall be implemented with latching low behavior.

For 10 Gb/s operation, bit 4.1.2 is a latching low version of bit 4.24.12.

**45.2.4.2.3 Low-power ability (4.1.1)**

When read as a one, bit 4.1.1 indicates that the PHY XS supports the low-power feature. When read as a zero, bit 4.1.1 indicates that the PHY XS does not support the low-power feature. If a PHY XS supports the low-power feature then it is controlled using the low-power bit in the PHY XS control register.

**45.2.4.3 PHY XS device identifier (Registers 4.2 and 4.3)**

Registers 4.2 and 4.3 provide a 32-bit value, which may constitute a unique identifier for a PHY XS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PHY XS may return a value of zero in each of the 32 bits of the PHY XS device identifier.

The format of the PHY XS device identifier is specified in 22.2.4.3.1.

**45.2.4.4 PHY XS speed ability (Register 4.4)**

The assignment of bits in the PHY XS speed ability register is shown in Table 45–47.

**Table 45–47—PHY XS speed ability register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
4.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
4.4.0	10G capable	1 = PHY XS is capable of operating at 10 Gb/s 0 = PHY XS is not capable of operating at 10 Gb/s	RO

<sup>a</sup>RO = Read Only

**45.2.4.4.1 10G capable (4.4.0)**

When read as a one, bit 4.4.0 indicates that the PHY XS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 4.4.0 indicates that the PHY-XS is not able to operate at a data rate of 10 Gb/s.

**45.2.4.5 PHY XS devices in package (Registers 4.5 and 4.6)**

The assignment of bits in the PHY XS devices in package registers is shown in Table 45–48.



**Table 45–48—PHY XS devices in package registers bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
4.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
4.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
4.6.13:0	Reserved	Ignore on read	RO
4.5.15:6	Reserved	Ignore on read	RO
4.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
4.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
4.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
4.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
4.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
4.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

<sup>a</sup>RO = Read Only

When read as a one, a bit in the PHY XS devices in package registers indicates that the associated MMD has been instantiated within the same package as other MMDs whose associated bits have been set to a one within the PHY XS devices in package registers. The Clause 22 registers present bit is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

**45.2.4.6 PHY XS status 2 register (Register 4.8)**

The assignment of bits in the PHY XS status 2 register is shown in Table 45–49. All the bits in the PHY XS status 2 register are read only; a write to the PHY XS status 2 register shall have no effect.

**45.2.4.6.1 Device present (4.8.15:14)**

When read as <10>, bits 4.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 4.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

**45.2.4.6.2 Transmit fault (4.8.11)**

When read as a one, bit 4.8.11 indicates that the PHY XS has detected a fault condition on the transmit path. When read as a zero, bit 4.8.11 indicates that the PHY XS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

**Table 45–49—PHY XS status 2 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
4.8.15:14	Device present	$\begin{matrix} \underline{15} & \underline{14} \\ 1 & 0 & = \text{Device responding at this address} \\ 1 & 1 & = \text{No device responding at this address} \\ 0 & 1 & = \text{No device responding at this address} \\ 0 & 0 & = \text{No device responding at this address} \end{matrix}$	RO
4.8.13:12	Reserved	Ignore when read	RO
4.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
4.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
4.8.9:0	Reserved	Ignore when read	RO

<sup>a</sup>RO = Read Only, LH = Latching High

The default value for bit 4.8.11 is zero.

**45.2.4.6.3 Receive fault (4.8.10)**

When read as a one, bit 4.8.10 indicates that the PHY XS has detected a fault condition on the receive path. When read as a zero, bit 4.8.10 indicates that the PHY XS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 4.8.10 is zero.

**45.2.4.7 PHY XS package identifier (Registers 4.14 and 4.15)**

Registers 4.14 and 4.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the PHY XS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A PHY XS may return a value of zero in each of the 32 bits of the PHY XS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the PHY XS package identifier is specified in 22.2.4.3.1.

**45.2.4.8 10G PHY XGXS lane status register (Register 4.24)**

The assignment of bits in the 10G PHY XGXS lane status register is shown in Table 45–50. All the bits in the 10G PHY XGXS lane status register are read only; a write to the 10G PHY XGXS lane status register shall have no effect.

**Table 45–50—10G PHY XGXS lane status register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
4.24.15:13	Reserved	Ignore when read	RO
4.24.12	PHY XGXS lane alignment status	1 = PHY XGXS transmit lanes aligned 0 = PHY XGXS transmit lanes not aligned	RO
4.24.11	Pattern testing ability	1 = PHY XGXS is able to generate test patterns 0 = PHY XGXS is not able to generate test patterns	RO
4.24.10	PHY XGXS loopback ability	1 = PHY XGXS has the ability to perform a loopback function 0 = PHY XGXS does not have the ability to perform a loopback function	RO
4.24.9:4	Reserved	Ignore when read	RO
4.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
4.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
4.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
4.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

<sup>a</sup>RO = Read Only**45.2.4.8.1 PHY XGXS transmit lane alignment status (4.24.12)**

When read as a one, bit 4.24.12 indicates that the PHY XGXS has synchronized and aligned all four transmit lanes. When read as a zero, bit 4.24.12 indicates that the PHY XGXS has not synchronized and aligned all four transmit lanes.

**45.2.4.8.2 Pattern testing ability (4.24.11)**

When read as a one, bit 4.24.11 indicates that the 10G PHY XGXS is able to generate test patterns. When read as a zero, bit 4.24.11 indicates that the 10G PHY XGXS is not able to generate test patterns. If the 10G PHY XGXS is able to generate test patterns, then the functionality is controlled using the transmit test-pattern enable bit in register 4.25.

**45.2.4.8.3 PHY XS loopback ability (4.24.10)**

When read as a one, bit 4.24.10 indicates that the PHY XGXS is able to perform the loopback function. When read as a zero, bit 4.24.10 indicates that the PHY XGXS is not able to perform the loopback function. If a 10G PHY XGXS is able to perform the loopback function, then it is controlled using the PHY XGXS loopback bit 4.0.14.

**45.2.4.8.4 Lane 3 sync (4.24.3)**

When read as a one, bit 4.24.3 indicates that the 10G PHY XGXS transmit lane 3 is synchronized. When read as a zero, bit 4.24.3 indicates that the 10G PHY XGXS transmit lane 3 is not synchronized.

**45.2.4.8.5 Lane 2 sync (4.24.2)**

When read as a one, bit 4.24.2 indicates that the 10G PHY XGXS transmit lane 2 is synchronized. When read as a zero, bit 4.24.2 indicates that the 10G PHY XGXS transmit lane 2 is not synchronized.

**45.2.4.8.6 Lane 1 sync (4.24.1)**

When read as a one, bit 4.24.1 indicates that the 10G PHY XGXS transmit lane 1 is synchronized. When read as a zero, bit 4.24.1 indicates that the 10G PHY XGXS transmit lane 1 is not synchronized.

**45.2.4.8.7 Lane 0 sync (4.24.0)**

When read as a one, bit 4.24.0 indicates that the 10G PHY XGXS transmit lane 0 is synchronized. When read as a zero, bit 4.24.0 indicates that the 10G PHY XGXS transmit lane 0 is not synchronized.

**45.2.4.9 10G PHY XGXS test control register (Register 4.25)**

The assignment of bits in the 10G PHY XGXS test control register is shown in Table 45–51. The default value for each bit of the 10G PHY XGXS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

**Table 45–51—10G PHY XGXS test control register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>												
4.25.15:3	Reserved	Value always 0, writes ignored	R/W												
4.25.2	Receive test-pattern enable	1 = Receive test pattern enabled 0 = Receive test pattern not enabled	R/W												
4.25.1:0	Test-pattern select	<table style="border: none;"> <tr> <td style="padding-right: 10px;"><math>\frac{1}{1}</math></td> <td style="padding-right: 10px;"><math>\frac{0}{1}</math></td> <td>= Reserved</td> </tr> <tr> <td style="padding-right: 10px;"><math>\frac{1}{0}</math></td> <td style="padding-right: 10px;"><math>\frac{0}{0}</math></td> <td>= Mixed-frequency test pattern</td> </tr> <tr> <td style="padding-right: 10px;"><math>\frac{0}{1}</math></td> <td style="padding-right: 10px;"><math>\frac{1}{0}</math></td> <td>= Low-frequency test pattern</td> </tr> <tr> <td style="padding-right: 10px;"><math>\frac{0}{0}</math></td> <td style="padding-right: 10px;"><math>\frac{1}{1}</math></td> <td>= High-frequency test pattern</td> </tr> </table>	$\frac{1}{1}$	$\frac{0}{1}$	= Reserved	$\frac{1}{0}$	$\frac{0}{0}$	= Mixed-frequency test pattern	$\frac{0}{1}$	$\frac{1}{0}$	= Low-frequency test pattern	$\frac{0}{0}$	$\frac{1}{1}$	= High-frequency test pattern	R/W
$\frac{1}{1}$	$\frac{0}{1}$	= Reserved													
$\frac{1}{0}$	$\frac{0}{0}$	= Mixed-frequency test pattern													
$\frac{0}{1}$	$\frac{1}{0}$	= Low-frequency test pattern													
$\frac{0}{0}$	$\frac{1}{1}$	= High-frequency test pattern													

<sup>a</sup>R/W = Read/Write

**45.2.4.9.1 10G PHY XGXS test-pattern enable (4.25.2)**

When bit 4.25.2 is set to a one, pattern testing is enabled on the receive path. When bit 4.25.2 is set to a zero, pattern testing is disabled on the receive path. Pattern testing is optional, and the ability of the 10G PHY XGXS to generate test patterns is advertised by the pattern testing ability bit in register 4.24. A 10G PHY XGXS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 4.25.2 is zero.

**45.2.4.9.2 10G PHY XGXS test-pattern select (4.25.1:0)**

The test pattern to be used when pattern testing is enabled using bit 4.25.2 is selected using bits 4.25.1:0. When bits 4.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 4.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 4.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

**45.2.5 DTE XS registers**

The assignment of registers in the DTE XS is shown in Table 45–52.

**Table 45–52—DTE XS registers**

Register address	Register name
5.0	DTE XS control 1
5.1	DTE XS status 1
5.2, 5.3	DTE XS device identifier
5.4	DTE XS speed ability
5.5, 5.6	DTE XS devices in package
5.7	Reserved
5.8	DTE XS status 2
5.9 through 5.13	Reserved
5.14, 5.15	DTE XS package identifier
5.16 through 5.23	Reserved
5.24	10G DTE XGXS lane status
5.25	10G DTE XGXS test control
5.26 through 5.32 767	Reserved
5.32 768 through 5.65 535	Vendor specific

**45.2.5.1 DTE XS control 1 register (Register 5.0)**

The assignment of bits in the DTE XS control 1 register is shown in Table 45–53. The default value for each bit of the DTE XS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

**Table 45–53—DTE XS control 1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
5.0.15	Reset	1 = DTE XS reset 0 = Normal operation	R/W SC
5.0.14	Loopback	1 = Enable Loopback mode 0 = Disable Loopback mode	R/W
5.0.13	Speed selection	1 = Operation at 10 Gbp/s and above 0 = Unspecified	R/W
5.0.12	Reserved	Value always 0, writes ignored	R/W
5.0.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
5.0.10:7	Reserved	Value always 0, writes ignored	R/W
5.0.6	Speed selection	1 = Operation at 10 Gb/s and above 0 = Unspecified	R/W
5.0.5:2	Speed selection	$\begin{matrix} \underline{5} & \underline{4} & \underline{3} & \underline{2} \\ 1 & x & x & x = \text{Reserved} \\ x & 1 & x & x = \text{Reserved} \\ x & x & 1 & x = \text{Reserved} \\ 0 & 0 & 0 & 1 = \text{Reserved} \\ 0 & 0 & 0 & 0 = 10 \text{ Gb/s} \end{matrix}$	R/W
5.0.1:0	Reserved	Value always 0, writes ignored	R/W

<sup>a</sup>R/W = Read/Write, SC = Self Clearing

**45.2.5.1.1 Reset (5.0.15)**

Resetting a DTE XS is accomplished by setting bit 5.0.15 to a one. This action shall set all DTE XS registers to their default states. As a consequence, this action may change the internal state of the DTE XS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a DTE XS shall return a value of one in bit 5.0.15 when a reset is in progress and a value of zero otherwise. A DTE XS is not required to accept a write transaction to any of its registers until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 5.0.15. During a reset, a DTE XS shall respond to reads to register bits 5.0.15 and 5.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

**45.2.5.1.2 Loopback (5.0.14)**

The DTE XS shall be placed in a Loopback mode of operation when bit 5.0.14 is set to a one. When bit 5.0.14 is set to a one, the DTE XS shall accept data on the transmit path and return it on the receive path. For 10 Gb/s operation, the specific behavior of a DTE XS during loopback is specified in 48.3.3.

The default value of bit 5.0.14 is zero.

NOTE—The signal path through the DTE XS that is exercised in the Loopback mode of operation is implementation specific, but it is recommended that the signal path encompass as much of the DTE XS circuitry as is practical. The

intention of providing this Loopback mode of operation is to permit a diagnostic or self-test function to perform the transmission and reception of a PDU, thus testing the transmit and receive data paths. Other loopback signal paths may be enabled using loopback controls within other MMDs.

**45.2.5.1.3 Low power (5.0.11)**

A DTE XS may be placed into a low-power mode by setting bit 5.0.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the DTE XS. The behavior of the DTE XS in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 5.0.11 is zero.

**45.2.5.1.4 Speed selection (5.0.13, 5.0.6, 5.0.5:2)**

Speed selection bits 5.0.13 and 5.0.6 shall both be written as a one. Any attempt to change the bits to an invalid setting shall be ignored. These two bits are set to one in order to make them compatible with Clause 22.

The speed of the DTE XS may be selected using bits 5 through 2. The speed abilities of the DTE XS are advertised in the DTE XS speed ability register. A DTE XS may ignore writes to the DTE XS speed selection bits that select speeds it has not advertised in the DTE XS speed ability register. It is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs on a particular PHY.

The DTE XS speed selection defaults to a supported ability.

**45.2.5.2 DTE XS status 1 register (Register 5.1)**

The assignment of bits in the DTE XS status 1 register is shown in Table 45–54. All the bits in the DTE XS status 1 register are read only; a write to the DTE XS status 1 register shall have no effect.

**Table 45–54—DTE XS status 1 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
5.1.15:8	Reserved	Ignore when read	RO
5.1.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
5.1.6:3	Reserved	Ignore when read	RO
5.1.2	DTE XS receive link status	1 = The DTE XS receive link is up 0 = The DTE XS receive link is down	RO/LL
5.1.1	Low-power ability	1 = DTE XS supports low-power mode 0 = DTE XS does not support low-power mode	RO
5.1.0	Reserved	Ignore when read	RO

<sup>a</sup>RO = Read Only, LL = Latching Low

**45.2.5.2.1 Fault (5.1.7)**

When read as a one, bit 5.1.7 indicates that the DTE XS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 5.1.7 indicates that the DTE XS has not detected a fault condition. Bit 5.1.7 is set to a one when either of the fault bits (5.8.11, 5.8.10) located in register 5.8 are set to a one.

**45.2.5.2.2 DTE XS receive link status (5.1.2)**

When read as a one, bit 5.1.2 indicates that the DTE XS receive link is aligned. When read as a zero, bit 5.1.2 indicates that the DTE XS receive link is not aligned. The receive link status bit shall be implemented with latching low behavior.

For 10 Gb/s operation, this bit is a latching low version of bit 5.24.12.

**45.2.5.2.3 Low-power ability (5.1.1)**

When read as a one, bit 5.1.1 indicates that the DTE XS supports the low-power feature. When read as a zero, bit 5.1.1 indicates that the DTE XS does not support the low-power feature. If a DTE XS supports the low-power feature then it is controlled using the low-power bit in the DTE XS control register.

**45.2.5.3 DTE XS device identifier (Registers 5.2 and 5.3)**

Registers 5.2 and 5.3 provide a 32-bit value, which may constitute a unique identifier for a DTE XS. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A DTE XS may return a value of zero in each of the 32 bits of the DTE XS device identifier.

The format of the DTE XS device identifier is specified in 22.2.4.3.1

**45.2.5.4 DTE XS speed ability (Register 5.4)**

The assignment of bits in the DTE XS speed ability register is shown in Table 45–55.

**Table 45–55— DTE XS speed ability register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
5.4.15:1	Reserved for future speeds	Value always 0, writes ignored	RO
5.4.0	10G capable	1 = DTE XS is capable of operating at 10 Gb/s 0 = DTE XS is not capable of operating at 10 Gb/s	RO

<sup>a</sup>RO = Read Only

**45.2.5.4.1 10G capable (5.4.0)**

When read as a one, bit 5.4.0 indicates that the DTE XS is able to operate at a data rate of 10 Gb/s. When read as a zero, bit 5.4.0 indicates that the DTE XS is not able to operate at a data rate of 10 Gb/s.

**45.2.5.5 DTE XS devices in package (Registers 5.5 and 5.6)**

The assignment of bits in the DTE XS devices in package registers is shown in Table 45–56.



**Table 45–56—DTE XS devices in package registers bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
5.6.15	Vendor specific device 2 present	1 = Vendor specific device 2 present in package 0 = Vendor specific device 2 not present in package	RO
5.6.14	Vendor specific device 1 present	1 = Vendor specific device 1 present in package 0 = Vendor specific device 1 not present in package	RO
5.6.13:0	Reserved	Ignore on read	RO
5.5.15:6	Reserved	Ignore on read	RO
5.5.5	DTE XS present	1 = DTE XS present in package 0 = DTE XS not present in package	RO
5.5.4	PHY XS present	1 = PHY XS present in package 0 = PHY XS not present in package	RO
5.5.3	PCS present	1 = PCS present in package 0 = PCS not present in package	RO
5.5.2	WIS present	1 = WIS present in package 0 = WIS not present in package	RO
5.5.1	PMD/PMA present	1 = PMA/PMD present in package 0 = PMA/PMD not present in package	RO
5.5.0	Clause 22 registers present	1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	RO

<sup>a</sup>RO = Read Only

When read as a one, a bit in the DTE XS devices in package registers indicates that the associated MMD has been instantiated within the same package as other MMDs whose associated bits have been set to a one within the DTE XS devices in package registers. The Clause 22 registers present bit is used to indicate that Clause 22 functionality has been implemented within a Clause 45 electrical interface device. The definition of the term package is vendor specific and could be a chip, module, or other similar entity.

**45.2.5.6 DTE XS status 2 register (Register 5.8)**

The assignment of bits in the DTE XS status 2 register is shown in Table 45–57. All the bits in the DTE XS status 2 register are read only; a write to the DTE XS status 2 register shall have no effect.

**45.2.5.6.1 Device present (5.8.15:14)**

When read as <10>, bits 5.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 5.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

**45.2.5.6.2 Transmit fault (5.8.11)**

When read as a one, bit 5.8.11 indicates that the DTE XS has detected a fault condition on the transmit path. When read as a zero, bit 5.8.11 indicates that the DTE XS has not detected a fault condition on the transmit path. The transmit fault bit shall be implemented with latching high behavior.

**Table 45–57—DTE XS status 2 register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
5.8.15:14	Device present	$\begin{matrix} \underline{15} & \underline{14} \\ 1 & 0 \\ 1 & 1 \\ 0 & 1 \\ 0 & 0 \end{matrix}$ = Device responding at this address = No device responding at this address = No device responding at this address = No device responding at this address	RO
5.8.13:12	Reserved	Ignore when read	RO
5.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
5.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
5.8.9:0	Reserved	Ignore when read	RO

<sup>a</sup>RO = Read Only, LH = Latching High

The default value of bit 5.8.11 is zero.

**45.2.5.6.3 Receive fault (5.8.10)**

When read as a one, bit 5.8.10 indicates that the DTE XS has detected a fault condition on the receive path. When read as a zero, bit 5.8.10 indicates that the DTE XS has not detected a fault condition on the receive path. The receive fault bit shall be implemented with latching high behavior.

The default value of bit 5.8.10 is zero.

**45.2.5.7 DTE XS package identifier (Registers 5.14 and 5.15)**

Registers 5.14 and 5.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the DTE XS is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A DTE XS may return a value of zero in each of the 32 bits of the DTE XS package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the DTE XS package identifier is specified in 22.2.4.3.1.

**45.2.5.8 10G DTE XGXS lane status register (Register 5.24)**

The assignment of bits in the 10G DTE XGXS lane status register is shown in Table 45–58. All the bits in the 10G DTE XGXS lane status register are read only; a write to the 10G DTE XGXS lane status register shall have no effect.

**Table 45–58—10G DTE XGXS lane status register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>
5.24.15:13	Reserved	Ignore when read	RO
5.24.12	DTE XGXS lane alignment status	1 = DTE XGXS receive lanes aligned 0 = DTE XGXS receive lanes not aligned	RO
5.24.11	Pattern testing ability	1 = DTE XGXS is able to generate test patterns 0 = DTE XGXS is not able to generate test patterns	RO
5.24.10:4	Reserved	Ignore when read	RO
5.24.3	Lane 3 sync	1 = Lane 3 is synchronized 0 = Lane 3 is not synchronized	RO
5.24.2	Lane 2 sync	1 = Lane 2 is synchronized 0 = Lane 2 is not synchronized	RO
5.24.1	Lane 1 sync	1 = Lane 1 is synchronized 0 = Lane 1 is not synchronized	RO
5.24.0	Lane 0 sync	1 = Lane 0 is synchronized 0 = Lane 0 is not synchronized	RO

<sup>a</sup>RO = Read Only**45.2.5.8.1 DTE XGXS receive lane alignment status (5.24.12)**

When read as a one, bit 5.24.12 indicates that the DTE XGXS has synchronized and aligned all four receive lanes. When read as a zero, bit 5.24.12 indicates that the DTE XGXS has not synchronized and aligned all four receive lanes.

**45.2.5.8.2 Pattern testing ability (5.24.11)**

When read as a one, bit 5.24.11 indicates that the 10G DTE XGXS is able to generate test patterns. When read as a zero, bit 5.24.11 indicates that the 10G DTE XGXS is not able to generate test patterns. If the 10G DTE XGXS is able to generate test patterns then the functionality is controlled using the transmit test-pattern enable bit in register 5.25.

**45.2.5.8.3 Lane 3 sync (5.24.3)**

When read as a one, bit 5.24.3 indicates that the XGXS receive lane 3 is synchronized. When read as a zero, bit 5.24.3 indicates that the XGXS receive lane 3 is not synchronized.

**45.2.5.8.4 Lane 2 sync (5.24.2)**

When read as a one, bit 5.24.2 indicates that the XGXS receive lane 2 is synchronized. When read as a zero, bit 5.24.2 indicates that the XGXS receive lane 2 is not synchronized.

**45.2.5.8.5 Lane 1 sync (5.24.1)**

When read as a one, bit 5.24.1 indicates that the XGXS receive lane 1 is synchronized. When read as a zero, bit 5.24.1 indicates that the XGXS receive lane 1 is not synchronized.

**45.2.5.8.6 Lane 0 sync (5.24.0)**

When read as a one, bit 5.24.0 indicates that the XGXS receive lane 0 is synchronized. When read as a zero, bit 5.24.0 indicates that the XGXS receive lane 0 is not synchronized.

**45.2.5.9 10G DTE XGXS test control register (Register 5.25)**

The assignment of bits in the 10G DTE XGXS test control register is shown in Table 45–59. The default value for each bit of the 10G DTE XGXS test control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

**Table 45–59—10G DTE XGXS test control register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>												
5.25.15:3	Reserved	Value always 0, writes ignored	R/W												
5.25.2	Transmit test-pattern enable	1 = Transmit test pattern enabled 0 = Transmit test pattern not enabled	R/W												
5.25.1:0	Test-pattern select	<table border="0"> <tr> <td><math>\frac{1}{1}</math></td> <td><math>\frac{0}{1}</math></td> <td>= Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>= Mixed-frequency test pattern</td> </tr> <tr> <td>0</td> <td>1</td> <td>= Low-frequency test pattern</td> </tr> <tr> <td>0</td> <td>0</td> <td>= High-frequency test pattern</td> </tr> </table>	$\frac{1}{1}$	$\frac{0}{1}$	= Reserved	1	0	= Mixed-frequency test pattern	0	1	= Low-frequency test pattern	0	0	= High-frequency test pattern	R/W
$\frac{1}{1}$	$\frac{0}{1}$	= Reserved													
1	0	= Mixed-frequency test pattern													
0	1	= Low-frequency test pattern													
0	0	= High-frequency test pattern													

<sup>a</sup>R/W = Read/Write

**45.2.5.9.1 10G DTE XGXS test-pattern enable (5.25.2)**

When bit 5.25.2 is set to a one, pattern testing is enabled on the transmit path. When bit 5.25.2 is set to a zero, pattern testing is disabled on the transmit path. Pattern testing is optional, and the ability of the 10G DTE XGXS to generate test patterns is advertised by the pattern testing ability bit in register 5.24. A 10G DTE XGXS that does not support the generation of test patterns shall ignore writes to this bit and always return a value of zero. The default of bit 5.25.2 is zero.

**45.2.5.9.2 10G DTE XGXS test-pattern select (5.25.1:0)**

The test pattern to be used when pattern testing is enabled using bit 5.25.2 is selected using bits 5.25.1:0. When bits 5.25.1:0 are set to <10>, the mixed-frequency test pattern shall be selected for pattern testing. When bits 5.25.1:0 are set to <01>, the low-frequency test pattern shall be selected for pattern testing. When bits 5.25.1:0 are set to <00>, the high-frequency test pattern shall be selected for pattern testing. The test patterns are defined in Annex 48A.

**45.2.6 Vendor specific MMD 1 registers**

The assignment of registers in the vendor specific MMD 1 is shown in Table 45–60. A vendor specific MMD may have a device address of either 30 or 31. It is recommended that the device address is configurable and that the configuration is performed by some means other than via the MDIO.

**Table 45–60—Vendor specific MMD 1 registers**

Register address	Register name
30.0, 30.1	Vendor specific
30.2, 30.3	Vendor specific MMD 1 device identifier
30.4 through 30.7	Vendor specific
30.8	Vendor specific MMD 1 status register
30.9 through 30.13	Vendor specific
30.14, 30.15	Vendor specific MMD 1 package identifier
30.16 through 30.65 535	Vendor specific

**45.2.6.1 Vendor specific MMD 1 device identifier (Registers 30.2 and 30.3)**

Registers 30.2 and 30.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of vendor specific device. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific device may return a value of zero in each of the 32 bits of the vendor specific MMD 1 device identifier.

The format of the vendor specific MMD 1 device identifier is specified in 22.2.4.3.1.

**45.2.6.2 Vendor specific MMD 1 status register (Register 30.8)**

The assignment of bits in the vendor specific MMD 1 status register is shown in Table 45–61. All the bits in the vendor specific MMD 1 status register are read only; a write to the vendor specific MMD 1 status register shall have no effect.

**45.2.6.2.1 Device present (30.8.15:14)**

When read as <10>, bits 30.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 30.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

**45.2.6.3 Vendor specific MMD 1 package identifier (Registers 30.14 and 30.15)**

Registers 30.14 and 30.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the vendor specific MMD 1 is instantiated within. The identifier shall be composed of

**Table 45–61—Vendor specific MMD 1 status register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>															
30.8.15:14	Device present	<table border="0"> <tr> <td><u>15</u></td> <td><u>14</u></td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>= Device responding at this address</td> </tr> <tr> <td>1</td> <td>1</td> <td>= No device responding at this address</td> </tr> <tr> <td>0</td> <td>1</td> <td>= No device responding at this address</td> </tr> <tr> <td>0</td> <td>0</td> <td>= No device responding at this address</td> </tr> </table>	<u>15</u>	<u>14</u>		1	0	= Device responding at this address	1	1	= No device responding at this address	0	1	= No device responding at this address	0	0	= No device responding at this address	RO
<u>15</u>	<u>14</u>																	
1	0	= Device responding at this address																
1	1	= No device responding at this address																
0	1	= No device responding at this address																
0	0	= No device responding at this address																
30.8.13:0	Reserved	Ignore when read	RO															

<sup>a</sup>RO = Read Only

the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific MMD 1 may return a value of zero in each of the 32 bits of the vendor specific MMD 1 package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the vendor specific MMD 1 package identifier is specified in 22.2.4.3.1.

**45.2.7 Vendor specific MMD 2 registers**

The assignment of registers in the vendor specific MMD 2 is shown in Table 45–62. A vendor specific MMD may have a device address of either 30 or 31. It is recommended that the device address is configurable and that the configuration is performed by some means other than via the MDIO.

**Table 45–62—Vendor specific MMD 2 registers**

Register address	Register name
31.0, 31.1	Vendor specific
31.2, 31.3	Vendor specific MMD 2 device identifier
31.4 through 31.7	Vendor specific
31.8	Vendor specific MMD 2 status register
31.9 through 31.13	Vendor specific
31.14, 30.15	Vendor specific MMD 2 package identifier
31.16 through 31.65 535	Vendor specific

**45.2.7.1 Vendor specific MMD 2 device identifier (Registers 31.2 and 31.3)**

Registers 31.2 and 31.3 provide a 32-bit value, which may constitute a unique identifier for a particular type of vendor specific device. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the device manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific device may return a value of zero in each of the 32 bits of the vendor specific MMD 2 device identifier.

The format of the vendor specific MMD 2 device identifier is specified in 22.2.4.3.1.

**45.2.7.2 Vendor specific MMD 2 status register (Register 31.8)**

The assignment of bits in the vendor specific MMD 2 status register is shown in Table 45–63. All the bits in the vendor specific MMD 2 status register are read only; a write to the vendor specific MMD status register shall have no effect.

**Table 45–63—Vendor specific MMD 2 status register bit definitions**

Bit(s)	Name	Description	R/W <sup>a</sup>															
31.8.15:14	Device present	<table border="0"> <tr> <td><u>15</u></td> <td><u>14</u></td> <td>= Device responding at this address</td> </tr> <tr> <td>1</td> <td>0</td> <td>= No device responding at this address</td> </tr> <tr> <td>1</td> <td>1</td> <td>= No device responding at this address</td> </tr> <tr> <td>0</td> <td>1</td> <td>= No device responding at this address</td> </tr> <tr> <td>0</td> <td>0</td> <td>= No device responding at this address</td> </tr> </table>	<u>15</u>	<u>14</u>	= Device responding at this address	1	0	= No device responding at this address	1	1	= No device responding at this address	0	1	= No device responding at this address	0	0	= No device responding at this address	RO
<u>15</u>	<u>14</u>	= Device responding at this address																
1	0	= No device responding at this address																
1	1	= No device responding at this address																
0	1	= No device responding at this address																
0	0	= No device responding at this address																
31.8.13:0	Reserved	Ignore when read	RO															

<sup>a</sup>RO = Read Only

**45.2.7.2.1 Device present (31.8.15:14)**

When read as <10>, bits 31.8.15:14 indicate that a device is present and responding at this register address. When read as anything other than <10>, bits 31.8.15:14 indicate that no device is present at this register address or that the device is not functioning properly.

**45.2.7.3 Vendor specific MMD 2 package identifier (Registers 31.14 and 31.15)**

Registers 31.14 and 31.15 provide a 32-bit value, which may constitute a unique identifier for a particular type of package that the vendor specific MMD is instantiated within. The identifier shall be composed of the 3rd through 24th bits of the Organizationally Unique Identifier (OUI) assigned to the package manufacturer by the IEEE, plus a six-bit model number, plus a four-bit revision number. A vendor specific MMD may return a value of zero in each of the 32 bits of the package identifier.

A non-zero package identifier may be returned by one or more MMDs in the same package. The package identifier may be the same as the device identifier.

The format of the vendor specific MMD 2 package identifier is specified in 22.2.4.3.1.

**45.3 Management frame structure**

The MDIO interface frame structure is compatible with the one defined in 22.2.4.5 such that the two systems can co-exist on the same MDIO bus. The electrical specification for the MDIO interface is incompatible to that defined in 22.2.4.5; therefore, if the two systems are to co-exist on the same bus, a voltage translation device is required (see Annex 45A). The extensions that are used for MDIO indirect register accesses are specified in Table 45–64.

**Table 45–64—Extensions to Management Frame Format for Indirect Access**

Frame	Management frame fields						ADDRESS / DATA	IDLE
	PRE	ST	OP	PRTAD	DEVAD	TA		
Address	1...1	00	00	PPPPP	EEEEEE	10	AAAAAAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEEE	10	DDDDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEEE	Z0	DDDDDDDDDDDDDDDDDD	Z
Post-read-increment-address	1...1	00	10	PPPPP	EEEEEE	Z0	DDDDDDDDDDDDDDDDDD	Z

Each MMD shall implement a sixteen bit address register that stores the address of the register to be accessed by data transaction frames. The address register shall be overwritten by address frames. At power up or device reset, the contents of the address register are undefined.

Write, read, and post-read-increment-address frames shall access the register whose address is stored in the address register. Write and read frames shall not modify the contents of the address register.

Upon receiving a post-read-increment-address frame and having completed the read operation, the MMD shall increment the address register by one. For the case where the MMD’s address register contains 65 535, the MMD shall not increment the address register.

Implementations that incorporate several MMDs within a single component shall implement separate address registers so that the MMD’s address registers operate independently of one another.

**45.3.1 IDLE (idle condition)**

The idle condition on MDIO is a high-impedance state. All three state drivers shall be disabled and the MMD’s pull-up resistor will pull the MDIO line to a one.

**45.3.2 PRE (preamble)**

At the beginning of each transaction, the station management entity shall send a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC to provide the MMD with a pattern that it can use to establish synchronization. An MMD shall observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.



### 45.3.3 ST (start of frame)

The start of frame for indirect access cycles is indicated by the <00> pattern. This pattern assures a transition from the default one and identifies the frame as an indirect access. Frames that contain the ST=<01> pattern defined in Clause 22 shall be ignored by the devices specified in Clause 45.

### 45.3.4 OP (operation code)

The operation code field indicates the type of transaction being performed by the frame. A <00> pattern indicates that the frame payload contains the address of the register to access. A <01> pattern indicates that the frame payload contains data to be written to the register whose address was provided in the previous address frame. A <11> pattern indicates that the frame is read operation. A <10> pattern indicates that the frame is a post-read-increment-address operation.

### 45.3.5 PRTAD (port address)

The port address is five bits, allowing 32 unique port addresses. The first port address bit to be transmitted and received is the MSB of the address. A station management entity must have a priori knowledge of the appropriate port address for each port to which it is attached, whether connected to a single port or to multiple ports.

### 45.3.6 DEVAD (device address)

The device address is five bits, allowing 32 unique MMDs per port. The first device address bit transmitted and received is the MSB of the address.

### 45.3.7 TA (turnaround)

The turnaround time is a 2 bit time spacing between the device address field and the data field of a management frame to avoid contention during a read transaction. For a read or post-read-increment-address transaction, both the STA and the MMD shall remain in a high-impedance state for the first bit time of the turnaround. The MMD shall drive a zero bit during the second bit time of the turnaround of a read or post-read-increment-address transaction. During a write or address transaction, the STA shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround. Figure 22–13 shows the behavior of the MDIO signal during the turnaround field of a read or post-read-increment-address transaction.

### 45.3.8 ADDRESS / DATA

The address/data field is 16 bits. For an address cycle, it contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, the field contains the data to be written to the register. For a read or post-read-increment-address frame, the field contains the contents of the register. The first bit transmitted and received shall be bit 15.

## 45.4 Electrical interface

### 45.4.1 Electrical specification

The electrical characteristics of the MDIO interface are shown in Table 45–65. The MDIO uses signal levels that are compatible with devices operating at a nominal supply voltage of 1.2V.

NOTE—It is possible to implement the MDIO electrical interface using open drain buffers and a weak resistive pull up to a  $V_{DD}$  of 1.2V.

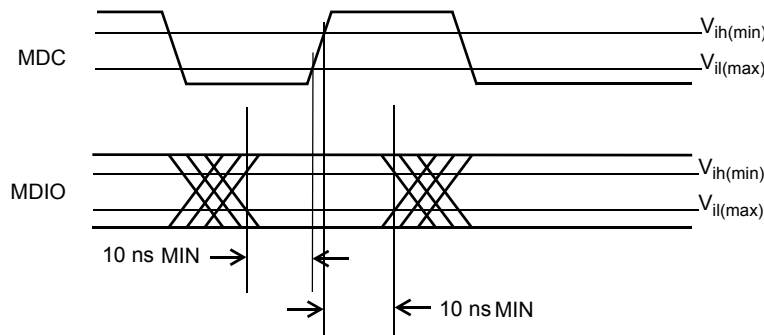
**Table 45–65—MDIO electrical interface characteristics**

Symbol	Parameter	Condition	Min.	Max.
V <sub>IH</sub>	Input high voltage		0.84V	1.5V
V <sub>IL</sub>	Input low voltage		-0.3V	0.36V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> = -100uA	1.0V	1.5V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 100uA	-0.3V	0.2V
I <sub>OH</sub> <sup>a</sup>	Output high current	V <sub>I</sub> = 1.0V		-4mA
I <sub>OL</sub>	Output low current	V <sub>I</sub> = 0.2V	+4mA	
C <sub>i</sub>	Input capacitance			10pF
C <sub>L</sub>	Bus loading			470pF

<sup>a</sup>I<sub>OH</sub> parameter is not applicable to open drain drivers.

**45.4.2 Timing specification**

MDIO is a bidirectional signal that can be sourced by the Station Management Entity (STA) or the MMD. When the STA sources the MDIO signal, the STA shall provide a minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC, as shown in Figure 45–3, measured at the MMD.

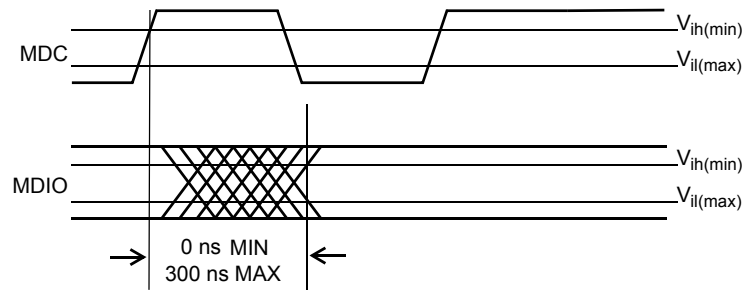


**Figure 45–3—MDIO sourced by STA**

When the MDIO signal is sourced by the MMD, it is sampled by the STA synchronously with respect to the rising edge of MDC. The clock to output delay from the MMD, as measured at the STA, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in Figure 45–4.

The timing specification for the MDC signal is given in 22.2.2.11.

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**Figure 45-4—MDIO sourced by MMD**

**45.5 Protocol Implementation Conformance Statement (PICS) proforma for Clause 45, MDIO interface<sup>1</sup>**

**45.5.3 Introduction**

The supplier of a protocol implementation that is claimed to conform to Clause 45, MDIO interface, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

**45.5.4 Identification**

**45.5.4.1 Implementation identification**

Supplier <sup>1</sup>	
Contact point for enquiries about the PICS <sup>1</sup>	
Implementation Name(s) and Version(s) <sup>1,3</sup>	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) <sup>2</sup>	
NOTES	
1—Required for all implementations.	
2—May be completed as appropriate in meeting the requirements for the identification.	
3—The terms Name and Version should be interpreted appropriately to correspond with a supplier’s terminology (e.g., Type, Series, Model).	

**45.5.4.2 Protocol summary**

Identification of protocol standard	IEEE Std 802.3ae-2002, Clause 45, Management Data Input/Output (MDIO) Interface
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ae-2002.)	

Date of Statement	
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<sup>1</sup>Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose any may further publish the completed PICS.

**45.5.4.3 Major capabilities/options**

Item	Feature	Subclause	Value/Comment	Status	Support
*PMA	Implementation of PMA/PMD MMD	45.2.1		O	Yes [ ] No [ ]
*WIS	Implementation of WIS MMD	45.2.2		O	Yes [ ] No [ ]
*PCS	Implementation of PCS MMD	45.2.3		O	Yes [ ] No [ ]
*PX	Implementation of PHY XS MMD	45.2.4		O	Yes [ ] No [ ]
*DX	Implementation of DTE XS MMD	45.2.5		O	Yes [ ] No [ ]
*VSA	Implementation of Vendor Specific MMD 1	45.2.6		O	Yes [ ] No [ ]
*VSB	Implementation of Vendor Specific MMD 2	45.2.7		O	Yes [ ] No [ ]

**45.5.5 PICS proforma tables for the Management Data Input Output (MDIO) interface**

**45.5.5.1 MDIO signal functional specifications**

Item	Feature	Subclause	Value/Comment	Status	Support
SF1	MDC min high/low time	45.4.2	160 ns	M	Yes [ ] No [ ]
SF2	MDC min period	45.4.2	400 ns	M	Yes [ ] No [ ]
SF3	MDIO uses three-state drivers	45.4.1		M	Yes [ ] No [ ]

**45.5.5.2 PMA/PMD MMD options**

Item	Feature	Subclause	Value/Comment	Status	Support
*ALB	Implementation of PMA loop-back function	45.2.1.1.4		PMA:O	Yes [ ] No [ ] N/A [ ]
*PLF	Implementation of fault detection	45.2.1.7		PMA:O	Yes [ ] No [ ] N/A [ ]
*PTD	Implementation of transmit disable function	45.2.1.8		PMA:O	Yes [ ] No [ ] N/A [ ]

**45.5.5.3 PMA/PMD management functions**

Item	Feature	Subclause	Value/Comment	Status	Support
MM1	Device responds to all register addresses for that device	45.2		PMA:M	Yes [ ] N/A [ ]
MM2	Writes to undefined and read-only registers have no effect	45.2		PMA:M	Yes [ ] N/A [ ]
MM3	Operation is not affected by writes to reserved and unsupported bits.	45.2		PMA:M	Yes [ ] N/A [ ]
MM4	Reserved and unsupported bits return a value of zero	45.2		PMA:M	Yes [ ] N/A [ ]
MM5	Latching low bits remain low until after they have been read via the management interface	45.2		PMA:M	Yes [ ] N/A [ ]
MM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PMA:M	Yes [ ] N/A [ ]
MM7	Latching high bits remain high until after they have been read via the management interface	45.2		PMA:M	Yes [ ] N/A [ ]
MM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PMA:M	Yes [ ] N/A [ ]
MM9	Action on reset	45.2.1.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PMA:M	Yes [ ] N/A [ ]
MM10	Return 1 until reset completed	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM11	Control and management interfaces are restored to operation within 0.5 s of reset	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM12	Responds to reads of bit 15 during reset	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM13	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.1.1.2		PMA:M	Yes [ ] N/A [ ]
MM14	Speed selection bits 13 and 6 are written as one	45.2.1.1.3		PMA:M	Yes [ ] N/A [ ]
MM15	Invalid writes to speed selection bits are ignored	45.2.1.1.3		PMA:M	Yes [ ] N/A [ ]
MM16	PMA is set into Loopback mode when bit 0 is set to a one	45.2.1.1.4		PMA*ALB:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MM17	PMA transmit data is returned on receive path when in loopback	45.2.1.1.4		PMA*ALB:M	Yes [ ] N/A [ ]
MM18	PMA ignores writes to this bit if it does not support loopback.	45.2.1.1.4		PMA*!ALB:M	Yes [ ] N/A [ ]
MM19	PMA returns a value of zero when read if it does not support loopback.	45.2.1.1.4		PMA*!ALB:M	Yes [ ] N/A [ ]
MM20	Writes to status 1 register have no effect	45.2.1.2		PMA:M	Yes [ ] N/A [ ]
MM21	Receive link status implemented with latching low behavior	45.2.1.2.2		PMA:M	Yes [ ] N/A [ ]
MM22	Unique identifier is composed of OUI, model number and revision	45.2.1.3		PMA:M	Yes [ ] N/A [ ]
MM23	10G PMA/PMD type is selected using bits 2:0	45.2.1.6.1		PMA:M	Yes [ ] N/A [ ]
MM24	10G PMA/PMD ignores writes to type selection bits that select types that it has not advertised	45.2.1.6.1		PMA:M	Yes [ ] N/A [ ]
MM25	Writes to the status 2 register have no effect	45.2.1.7		PMA:M	Yes [ ] N/A [ ]
MM26	PMA/PMD returns a value of zero for transmit fault if it is unable to detect a transmit fault	45.2.1.7.4		PMA:M	Yes [ ] N/A [ ]
MM27	Transmit fault is implemented using latching high behavior	45.2.1.7.4		PMA*PLF:M	Yes [ ] N/A [ ]
MM28	PMA/PMD returns a value of zero for receive fault if it is unable to detect a receive fault	45.2.1.7.5		PMA*!PLF:M	Yes [ ] N/A [ ]
MM29	Receive fault is implemented using latching high behavior	45.2.1.7.5		PMA*PLF:M	Yes [ ] N/A [ ]
MM30	Writes to register 9 are ignored by device that does not implement transmit disable	45.2.1.8		PMA*!PTD:M	Yes [ ] N/A [ ]
MM31	Single wavelength device uses lane zero for transmit disable	45.2.1.8		PMA*PTD:M	Yes [ ] N/A [ ]
MM32	Single wavelength device ignores writes to bits 1 – 4 and returns a value of zero for them	45.2.1.8		PMA*PTD:M	Yes [ ] N/A [ ]
MM33	Setting bit 4 to a one disables transmission on lane 3	45.2.1.8.1		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM34	Setting bit 4 to a zero enables transmission on lane 3	45.2.1.8.1		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MM35	Setting bit 3 to a one disables transmission on lane 2	45.2.1.8.2		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM36	Setting bit 3 to a zero enables transmission on lane 2	45.2.1.8.2		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM37	Setting bit 2 to a one disables transmission on lane 1	45.2.1.8.3		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM38	Setting bit 2 to a zero enables transmission on lane 1	45.2.1.8.3		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM39	Setting bit 1 to a one disables transmission on lane 0	45.2.1.8.4		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM40	Setting bit 1 to a zero enables transmission on lane 0	45.2.1.8.4		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM41	Setting bit 0 to a one disables transmission	45.2.1.8.5		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM42	Setting bit 0 to a zero enables transmission	45.2.1.8.5	Only is all lane transmit disables are zero	PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM43	Unique identifier is composed of OUI, model number and revision	45.2.1.10		PMA:M	Yes [ ] N/A [ ]

**45.5.5.4 WIS options**

Item	Feature	Subclause	Value/Comment	Status	Support
*WPT	Implementation of PRBS31 pattern testing	45.2.2		WIS:O	Yes [ ] No [ ] N/A [ ]

**45.5.5.5 WIS management functions**

Item	Feature	Subclause	Value/Comment	Status	Support
WM1	Device responds to all register addresses for that device	45.2		WIS:M	Yes [ ] N/A [ ]
WM2	Writes to undefined and read-only registers have no effect	45.2		WIS:M	Yes [ ] N/A [ ]



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Item	Feature	Subclause	Value/Comment	Status	Support
WM3	Operation is not affected by writes to reserved and unsupported bits.	45.2		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM4	Reserved and unsupported bits return a value of zero	45.2		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM5	Latching low bits remain low until after they have been read via the management interface	45.2		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM7	Latching high bits remain high until after they have been read via the management interface	45.2		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM9	Action on reset	45.2.2.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM10	Return 1 until reset completed	45.2.2.1.1		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM11	Reset completes within 0.5 s	45.2.2.1.1		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM12	Responds to reads of bits 2.0.15 and 2.8.15:14 during reset	45.2.2.1.1		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM13	Loopback mode	45.2.2.1.2	Whenever bit 2.0.14 is set to a one	WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM14	Data received from PMA ignored during loopback	45.2.2.1.2		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM15	Transmit data returned on receive path during loopback	45.2.2.1.2		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM16	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.2.1.3		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM17	Speed selection bits 13 and 6 are written as one	45.2.2.1.4		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM18	Invalid writes to speed selection bits are ignored	45.2.2.1.4		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM19	Writes to status 1 register have no effect	45.2.2.2		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>
WM20	Fault bit implemented using latching high behavior	45.2.2.2.1		WIS:M	Yes [ <input type="checkbox"/> N/A [ <input type="checkbox"/>

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Item	Feature	Subclause	Value/Comment	Status	Support
WM21	Link status bit implemented using latching low behavior	45.2.2.2.2		WIS:M	Yes [ ] N/A [ ]
WM22	Unique identifier is composed of OUI, model number and revision	45.2.2.3		WIS:M	Yes [ ] N/A [ ]
WM23	Setting bit 2.7.5 to a one enables PRBS31 receive pattern testing if bit 2.8.1 is a one and bit 2.7.2 is not a one	45.2.2.6.1		WIS* WPT:M	Yes [ ] N/A [ ]
WM24	Setting bit 2.7.5 to a zero disables PRBS31 receive pattern testing	45.2.2.6.1		WIS* WPT:M	Yes [ ] N/A [ ]
WM25	Setting bit 2.7.4 to a one enables PRBS31 transmit pattern testing if bit 2.8.1 is a one and bit 2.7.1 is not a one	45.2.2.6.2		WIS* WPT:M	Yes [ ] N/A [ ]
WM26	Setting bit 2.7.4 to a zero disables PRBS31 transmit pattern testing	45.2.2.6.2		WIS* WPT:M	Yes [ ] N/A [ ]
WM27	Setting bit 3 to one selects the square wave test pattern	45.2.2.6.3		WIS:M	Yes [ ] N/A [ ]
WM28	Setting bit 3 to zero selects the pseudo random test pattern	45.2.2.6.3		WIS:M	Yes [ ] N/A [ ]
WM29	Setting bit 2 to one enables receive pattern testing	45.2.2.6.4		WIS:M	Yes [ ] N/A [ ]
WM30	Setting bit 2 to zero disables receive pattern testing	45.2.2.6.4		WIS:M	Yes [ ] N/A [ ]
WM31	Setting bit 1 to one enables transmit pattern testing	45.2.2.6.5		WIS:M	Yes [ ] N/A [ ]
WM32	Setting bit 1 to zero disables transmit pattern testing	45.2.2.6.5		WIS:M	Yes [ ] N/A [ ]
WM33	Setting bit 0 to a one enables 10GBASE-W logic and sets interface speed	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM34	Setting bit 0 to a zero disables 10GBASE-W logic, sets interface speed. and bypasses data	45.2.2.6.6		WIS:O	Yes [ ] N/A [ ]
WM35	Writes to bit are ignored by WIS not capable of supporting 10GBASE-R	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM36	Bit returns one when read if WIS is not capable of supporting 10GBASE-R	45.2.2.6.6		WIS:M	Yes [ ] N/A [ ]
WM37	Writes to status 2 register have no effect	45.2.2.7		WIS:M	Yes [ ] N/A [ ]
WM38	Counter is reset to all zeros when read or reset	45.2.2.8		WIS* WPT:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
WM39	Counter is held at all ones at overflow	45.2.2.8		WIS* WPT:M	Yes [ ] N/A [ ]
WM40	Unique identifier is composed of OUI, model number and revision	45.2.2.9		WIS:M	Yes [ ] N/A [ ]
WM41	Writes to Status 3 register have no effect	45.2.2.10		WIS:M	Yes [ ] N/A [ ]
WM42	SEF bit implemented using latching high behavior	45.2.2.10.1		WIS:M	Yes [ ] N/A [ ]
WM43	Far end PLM-P/LCD-P bit implemented using latching high behavior	45.2.2.10.2		WIS:M	Yes [ ] N/A [ ]
WM44	Far end AIS-P/LOP-P bit implemented using latching high behavior	45.2.2.10.3		WIS:M	Yes [ ] N/A [ ]
WM45	LOF bit implemented using latching high behavior	45.2.2.10.4		WIS:M	Yes [ ] N/A [ ]
WM46	LOS bit implemented using latching high behavior	45.2.2.10.5		WIS:M	Yes [ ] N/A [ ]
WM47	RDI-L bit implemented using latching high behavior	45.2.2.10.6		WIS:M	Yes [ ] N/A [ ]
WM48	AIS-L bit implemented using latching high behavior	45.2.2.10.7		WIS:M	Yes [ ] N/A [ ]
WM49	LCD-P bit implemented using latching high behavior	45.2.2.10.8		WIS:M	Yes [ ] N/A [ ]
WM50	PLM-P bit implemented using latching high behavior	45.2.2.10.9		WIS:M	Yes [ ] N/A [ ]
WM51	AIS-P bit implemented using latching high behavior	45.2.2.10.10		WIS:M	Yes [ ] N/A [ ]
WM52	LOP-P bit implemented using latching high behavior	45.2.2.10.11		WIS:M	Yes [ ] N/A [ ]

**45.5.5.6 PCS options**

Item	Feature	Subclause	Value/Comment	Status	Support
*CR	Implementation of 10GBASE-R PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*CX	Implementation of 10GBASE-X PCS	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]
*XP	Implementation of 10GBASE-X pattern testing	45.2.3		PCS* CX:O	Yes [ ] No [ ] N/A [ ]
*PPT	Implementation of PRBS31 pattern testing	45.2.3		PCS:O	Yes [ ] No [ ] N/A [ ]

**45.5.5.7 PCS management functions**

Item	Feature	Subclause	Value/Comment	Status	Support
RM1	Device responds to all register addresses for that device	45.2		PCS:M	Yes [ ] N/A [ ]
RM2	Writes to undefined and read-only registers have no effect	45.2		PCS:M	Yes [ ] N/A [ ]
RM3	Operation is not affected by writes to reserved and unsupported bits	45.2		PCS:M	Yes [ ] N/A [ ]
RM4	Reserved and unsupported bits return a value of zero	45.2		PCS:M	Yes [ ] N/A [ ]
RM5	Latching low bits remain low until after they have been read via the management interface	45.2		PCS:M	Yes [ ] N/A [ ]
RM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PCS:M	Yes [ ] N/A [ ]
RM7	Latching high bits remain high until after they have been read via the management interface	45.2		PCS:M	Yes [ ] N/A [ ]
RM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PCS:M	Yes [ ] N/A [ ]
RM9	Action on reset	45.2.3.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PCS:M	Yes [ ] N/A [ ]
RM10	Return 1 until reset completed	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM11	Reset completes within 0.5 s	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM12	Device responds to reads of register bits 3.0.15 and 3.5.15:14 during reset	45.2.3.1.1		PCS:M	Yes [ ] N/A [ ]
RM13	Loopback mode	45.2.3.1.2	Whenever bit 3.0.14 is set to a one	PCS:M	Yes [ ] N/A [ ]
RM14	Transmit data is returned on the receive path during loopback	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM15	Writes to loopback bit are ignored when operating at 10 Gb/s with port type selections other than 10GBASE-R	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM16	Loopback bit returns zero when operating at 10 Gb/s with port type selections other than 10GBASE-R	45.2.3.1.2		PCS:M	Yes [ ] N/A [ ]
RM17	Device responds to transactions necessary to exit low-power mode while in low- power state	45.2.3.1.3		PCS:M	Yes [ ] N/A [ ]
RM18	Speed selection bits 13 and 6 are written as one	45.2.3.1.4		PCS:M	Yes [ ] N/A [ ]
RM19	Invalid writes to speed selection bits are ignored	45.2.3.1.4		PCS:M	Yes [ ] N/A [ ]
RM20	Writes to PCS status 1 register have no effect	45.2.3.2		PCS:M	Yes [ ] N/A [ ]
RM21	Receive link status implemented using latching low behavior	45.2.3.2.2		PCS:M	Yes [ ] N/A [ ]
RM22	Unique identifier is composed of OUI, model number and revision	45.2.3.3		PCS:M	Yes [ ] N/A [ ]
RM23	PCS type is selected using bits 1 through 0	45.2.3.6.1		PCS:M	Yes [ ] N/A [ ]
RM24	Writes to the type selection bits that select types that have not been advertised are ignored	45.2.3.6.1		PCS:M	Yes [ ] N/A [ ]
RM25	Writes to PCS status 2 register have no effect	45.2.3.7		PCS:M	Yes [ ] N/A [ ]
RM26	Transmit fault implemented with latching high behavior	45.2.3.7.3		PCS:M	Yes [ ] N/A [ ]
RM27	Receive fault implemented with latching high behavior	45.2.3.7.2		PCS:M	Yes [ ] N/A [ ]
RM28	Unique identifier is composed of OUI, model number and revision	45.2.3.8		PCS:M	Yes [ ] N/A [ ]
RM29	Writes to 10GBASE-X PCS status register have no effect	45.2.3.9		PCS* CX:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM30	Register returns zero if the PCS does not implement the 10GBASE-X port type	45.2.3.9		PCS* !CX:M	Yes [ ] N/A [ ]
RM31	Writes to bit are ignored and reads return a value of zero	45.2.3.10.1		PCS* PX:M	Yes [ ] N/A [ ]
RM32	Setting the bits to <10> selects the mixed frequency pattern	45.2.3.10.2		PCS* PX:M	Yes [ ] N/A [ ]
RM33	Setting the bits to <01> selects the low-frequency pattern	45.2.3.10.2		PCS* PX:M	Yes [ ] N/A [ ]
RM34	Setting the bits to <00> selects the high-frequency pattern	45.2.3.10.2		PCS* PX:M	Yes [ ] N/A [ ]
RM35	Writes to 10GBASE-R PCS status 1 register have no effect	45.2.3.11		PCS* CR:M	Yes [ ] N/A [ ]
RM36	Reads from 10GBASE-R PCS status 1 register return zero for PCS that does not support 10GBASE-R	45.2.3.11		PCS* CR:M	Yes [ ] N/A [ ]
RM37	Writes to 10GBASE-R PCS status 2 register have no effect	45.2.3.12		PCS* CR:M	Yes [ ] N/A [ ]
RM38	Reads from 10GBASE-R PCS status 2 register return zero for PCS that does not support 10GBASE-R	45.2.3.12		PCS* CR:M	Yes [ ] N/A [ ]
RM39	Latched block lock implemented with latching low behavior	45.2.3.12.1		PCS* CR:M	Yes [ ] N/A [ ]
RM40	Latched high BER implemented with latching high behavior	45.2.3.12.2		PCS* CR:M	Yes [ ] N/A [ ]
RM41	BER counter clears to zero on read or reset	45.2.3.12.3		PCS* CR:M	Yes [ ] N/A [ ]
RM42	BER counter holds at all ones at overflow	45.2.3.12.3		PCS* CR:M	Yes [ ] N/A [ ]
RM43	Errored blocks counter implemented as a non roll over counter	45.2.3.12.4		PCS* CR:M	Yes [ ] N/A [ ]
RM44	Errored blocks counter clears to zero on read	45.2.3.12.4		PCS* CR:M	Yes [ ] N/A [ ]
RM45	Setting bit 3.42.5 to a one enables PRBS31 receive pattern testing if bit 3.32.2 is a one and bit 3.42.2 is not a one	45.2.3.15.1		PCS* PPT:M	Yes [ ] N/A [ ]
RM46	Setting bit 3.42.5 to a zero disables PRBS31 receive pattern testing	45.2.3.15.1		PCS* PPT:M	Yes [ ] N/A [ ]
RM47	Setting bit 3.42.4 to a one enables PRBS31 transmit pattern testing if bit 3.32.2 is a one and bit 3.42.3 is not a one	45.2.3.15.2		PCS* PPT:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
RM48	Setting bit 3.42.4 to a zero disables PRBS31 transmit pattern testing	45.2.3.15.2		PCS* PPT:M	Yes [ ] N/A [ ]
RM49	Test-pattern error counter clears to zero on read or reset	45.2.3.16		PCS* CR:M	Yes [ ] N/A [ ]
RM50	Test-pattern error counter holds at all ones at overflow	45.2.3.16		PCS* CR:M	Yes [ ] N/A [ ]

**45.5.5.8 PHY XS options**

Item	Feature	Subclause	Value/Comment	Status	Support
*PL	Implementation of loopback	45.2.4		PX:O	Yes [ ] No [ ] N/A [ ]
*PT	Implementation of pattern testing	45.2.4		PX:O	Yes [ ] No [ ] N/A [ ]

**45.5.5.9 PHY XS management functions**

Item	Feature	Subclause	Value/Comment	Status	Support
PM1	Device responds to all register addresses for that device	45.2		PX:M	Yes [ ] N/A [ ]
PM2	Writes to undefined and read-only registers have no effect	45.2		PX:M	Yes [ ] N/A [ ]
PM3	Operation is not affected by writes to reserved and unsupported bits	45.2		PX:M	Yes [ ] N/A [ ]
PM4	Reserved and unsupported bits return a value of zero	45.2		PX:M	Yes [ ] N/A [ ]
PM5	Latching low bits remain low until after they have been read via the management interface	45.2		PX:M	Yes [ ] N/A [ ]
PM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PX:M	Yes [ ] N/A [ ]
PM7	Latching high bits remain high until after they have been read via the management interface	45.2		PX:M	Yes [ ] N/A [ ]
PM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PX:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
PM9	Action on reset	45.2.4.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PX:M	Yes [ ] N/A [ ]
PM10	Return 1 until reset completed	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM11	Reset completes within 0.5 s	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM12	Device responds to reads of bits 4.0.15 and 4.8.15:14 during reset	45.2.4.1.1		PX:M	Yes [ ] N/A [ ]
PM13	Loopback mode	45.2.4.1.2	Whenever bit 4.0.14 is set to a one	PX*PL:M	Yes [ ] N/A [ ]
PM14	Receive data is returned on transmit path during loopback	45.2.4.1.2		PX*PL:M	Yes [ ] N/A [ ]
PM15	Writes to loopback bit are ignored and reads return zero	45.2.4.1.2		PX*!PL:M	Yes [ ] N/A [ ]
PM16	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.4.1.3		PX:M	Yes [ ] N/A [ ]
PM17	Speed selection bits 13 and 6 are written as one	45.2.4.1.4		PX:M	Yes [ ] N/A [ ]
PM18	Invalid writes to speed selection bits are ignored	45.2.4.1.4		PX:M	Yes [ ] N/A [ ]
PM19	Writes to status 1 register have no effect	45.2.4.2		PX:M	Yes [ ] N/A [ ]
PM20	Transmit link status implemented using latching low behavior	45.2.4.2.2		PX:M	Yes [ ] N/A [ ]
PM21	Unique identifier is composed of OUI, model number and revision	45.2.4.3		PX:M	Yes [ ] N/A [ ]
PM22	Writes to status 2 register have no effect	45.2.4.6		PX:M	Yes [ ] N/A [ ]
PM23	Transmit fault implemented with latching high behavior	45.2.4.6.2		PX:M	Yes [ ] N/A [ ]
PM24	Receive fault implemented with latching high behavior	45.2.4.6.3		PX:M	Yes [ ] N/A [ ]
PM25	Unique identifier is composed of OUI, model number and revision	45.2.4.7		PX:M	Yes [ ] N/A [ ]
PM26	Writes to 10G PHY XGXS Lane status register have no effect	45.2.4.8		PX:M	Yes [ ] N/A [ ]
PM27	Writes to bit are ignored and reads return a value of zero	45.2.4.9.1		PX*!PT:M	Yes [ ] N/A [ ]



Item	Feature	Subclause	Value/Comment	Status	Support
PM28	Setting the bits to <10> selects the mixed frequency pattern	45.2.4.9.2		PX*PT:M	Yes [ ] N/A [ ]
PM29	Setting the bits to <01> selects the low-frequency pattern	45.2.4.9.2		PX*PT:M	Yes [ ] N/A [ ]
PM30	Setting the bits to <00> selects the high-frequency pattern	45.2.4.9.2		PX*PT:M	Yes [ ] N/A [ ]

**45.5.5.10 DTE XS options**

Item	Feature	Subclause	Value/Comment	Status	Support
*DT	Implementation of pattern testing	45.2.5		DX:O	Yes [ ] No [ ] N/A [ ]

**45.5.5.11 DTE XS management functions**

Item	Feature	Subclause	Value/Comment	Status	Support
DM1	Device responds to all register addresses for that device	45.2		DX:M	Yes [ ] N/A [ ]
DM2	Writes to undefined and read-only registers have no effect	45.2		DX:M	Yes [ ] N/A [ ]
DM3	Operation is not affected by writes to reserved and unsupported bits	45.2		DX:M	Yes [ ] N/A [ ]
DM4	Reserved and unsupported bits return a value of zero	45.2		DX:M	Yes [ ] N/A [ ]
DM5	Latching low bits remain low until after they have been read via the management interface	45.2		DX:M	Yes [ ] N/A [ ]
DM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	DX:M	Yes [ ] N/A [ ]
DM7	Latching high bits remain high until after they have been read via the management interface	45.2		DX:M	Yes [ ] N/A [ ]
DM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	DX:M	Yes [ ] N/A [ ]
DM9	Action on reset	45.2.5.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	DX:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
DM10	Return 1 until reset completed	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM11	Reset completes within 0.5 s	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM12	Device responds to reads of bits 5.0.15 and 5.8.15:14 during reset	45.2.5.1.1		DX:M	Yes [ ] N/A [ ]
DM13	Loopback mode	45.2.5.1.2	Whenever bit 5.0.14 is set to a one	DX:M	Yes [ ] N/A [ ]
DM14	Transmit data is returned on receive path during loopback	45.2.5.1.2		DX:M	Yes [ ] N/A [ ]
DM15	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.5.1.3		DX:M	Yes [ ] N/A [ ]
DM16	Speed selection bits 13 and 6 are written as one	45.2.5.1.4		DX:M	Yes [ ] N/A [ ]
DM17	Invalid writes to speed selection bits are ignored	45.2.5.1.4		DX:M	Yes [ ] N/A [ ]
DM18	Writes to status 1 register have no effect	45.2.5.2		DX:M	Yes [ ] N/A [ ]
DM19	Receive link status implemented using latching low behavior	45.2.5.2.2		DX:M	Yes [ ] N/A [ ]
DM20	Unique identifier is composed of OUI, model number and revision	45.2.5.3		DX:M	Yes [ ] N/A [ ]
DM21	Writes to status 2 register have no effect	45.2.5.6		DX:M	Yes [ ] N/A [ ]
DM22	Transmit fault implemented with latching high behavior	45.2.5.6.2		DX:M	Yes [ ] N/A [ ]
DM23	Receive fault implemented with latching high behavior	45.2.5.6.3		DX:M	Yes [ ] N/A [ ]
DM24	Unique identifier is composed of OUI, model number and revision	45.2.5.7		DX:M	Yes [ ] N/A [ ]
DM25	Writes to 10G DTE XGXS Lane status register have no effect	45.2.5.8		DX:M	Yes [ ] N/A [ ]
DM26	Writes to bit are ignored and reads return a value of zero	45.2.5.9.1		DX*!DT:M	Yes [ ] N/A [ ]
DM27	Setting the bits to <10> selects the mixed frequency pattern	45.2.5.9.2		DX*DT:M	Yes [ ] N/A [ ]
DM28	Setting the bits to <01> selects the low-frequency pattern	45.2.5.9.2		DX*DT:M	Yes [ ] N/A [ ]
DM29	Setting the bits to <00> selects the high-frequency pattern	45.2.5.9.2		DX*DT:M	Yes [ ] N/A [ ]

**45.5.5.12 Vendor specific MMD 1 management functions**

Item	Feature	Subclause	Value/Comment	Status	Support
VSA1	Device responds to all register addresses for that device	45.2		VSA:M	Yes [ ] N/A [ ]
VSA2	Writes to undefined and read-only registers have no effect	45.2		VSA:M	Yes [ ] N/A [ ]
VSA3	Operation is not affected by writes to reserved and unsupported bits	45.2		VSA:M	Yes [ ] N/A [ ]
VSA4	Reserved and unsupported bits return a value of zero	45.2		VSA:M	Yes [ ] N/A [ ]
VSA5	Unique identifier is composed of OUI, model number and revision	45.2.6.1		VSA:M	Yes [ ] N/A [ ]
VSA6	Writes to status register have no effect	45.2.6.2		VSA:M	Yes [ ] N/A [ ]
VSA7	Unique identifier is composed of OUI, model number and revision	45.2.6.3		VSA:M	Yes [ ] N/A [ ]

**45.5.5.13 Vendor specific MMD 2 management functions**

Item	Feature	Subclause	Value/Comment	Status	Support
VSB1	Device responds to all register addresses for that device	45.2		VSB:M	Yes [ ] N/A [ ]
VSB2	Writes to undefined and read-only registers have no effect	45.2		VSB:M	Yes [ ] N/A [ ]
VSB3	Operation is not affected by writes to reserved and unsupported bits	45.2		VSB:M	Yes [ ] N/A [ ]
VSB4	Reserved and unsupported bits return a value of zero	45.2		VSB:M	Yes [ ] N/A [ ]
VSB5	Unique identifier is composed of OUI, model number and revision	45.2.7.1		VSB:M	Yes [ ] N/A [ ]
VSB6	Writes to status register have no effect	45.2.7.2		VSB:M	Yes [ ] N/A [ ]
VSB7	Unique identifier is composed of OUI, model number and revision	45.2.7.3		VSB:M	Yes [ ] N/A [ ]

**45.5.5.14 Management frame structure**

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Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Device has implemented sixteen bit address register	45.3		M	Yes [ ]
MF2	Address register is overwritten by address frames	45.3		M	Yes [ ]
MF3	Write, read, and post-read-increment-address frames access the register whose address is held in the address register	45.3		M	Yes [ ]
MF4	Write and read frames do not modify the address register	45.3		M	Yes [ ]
MF5	Post-read-increment-address frames increment the address register by one unless the address register contains 65 535	45.3		M	Yes [ ]
MF6	Components containing several MMDs implement separate address registers	45.3		M	Yes [ ]
MF7	Tri state drivers are disabled during idle	45.3.1		M	Yes [ ]
MF8	STA sources 32 contiguous ones at the beginning of each transaction	45.3.2		M	Yes [ ]
MF9	MMD observes 32 contiguous ones at the beginning of each transaction	45.3.2		M	Yes [ ]
MF10	Frames containing ST=<01> sequence are ignored	45.3.3		M	Yes [ ]
MF11	STA tri state driver is high impedance during first bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF12	MMD tri state driver is high impedance during first bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF13	MMD tri state driver drives a zero bit during second bit of TA during read or post-read-increment-address frames	45.3.7		M	Yes [ ]
MF14	STA tri state driver drives a one bit followed by a zero bit for the TA during write or address frames	45.3.7		M	Yes [ ]
MF15	First bit transmitted and received is bit 15	45.3.8		M	Yes [ ]

**45.5.5.15 Signal timing characteristics**

Item	Feature	Subclause	Value/Comment	Status	Support
ST1	MDIO setup and hold time	45.4.2	Setup min = 10 ns; Hold min = 10 ns per	M	Yes [ ]
ST2	MDIO clock to output delay	45.4.2	Min = 0 ns; Max = 300 ns per	M	Yes [ ]

**45.5.5.16 Electrical characteristics**

Item	Feature	Subclause	Value/Comment	Status	Support
EC1	$V_{OH}$	45.4.1	$\geq 1.0V$ ( $I_{OH} = -100 \mu A$ ) $\leq 1.5V$ ( $I_{OH} = -100 \mu A$ )	M	Yes [ ]
EC2	$V_{OL}$	45.4.1	$\geq -0.3V$ ( $I_{OL} = 100 \mu A$ ) $\leq 0.2V$ ( $I_{OL} = 100 \mu A$ )	M	Yes [ ]
EC3	$V_{IH}$	45.4.1	$0.84V \leq V_{IH} \leq 1.5V$	M	Yes [ ]
EC4	$V_{IL}$	45.4.1	$-0.3 \leq V_{IL} \leq 0.36V$	M	Yes [ ]
EC5	Input capacitance for MDIO	45.4.1	$\leq 10pF$	M	Yes [ ]
EC6	Bus loading	45.4.1	$\leq 470pF$	M	Yes [ ]
EC7	$I_{OH}$	45.4.1	$\leq -4mA$ at $V_I = 1.0V$	M	Yes [ ]
EC8	$I_{OL}$	45.4.1	$\geq +4mA$ at $V_I = 0.2V$	M	Yes [ ]

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## **48. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X**

### **48.1 Overview**

This clause specifies the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer that are common to a family of 10 Gb/s Physical Layer implementations, collectively known as 10GBASE-X. The 10GBASE-LX4 PMD described in Clause 53 and 10GBASE-CX4 described in Clause 54 are members of the 10GBASE-X PHY family. The term 10GBASE-X is used when referring to issues common to any of the variants within this family.

The 10GBASE-X PCS and PMA sublayers are also utilized by the XGXS specified in Clause 47.

10GBASE-X PCS and PMA sublayers map the interface characteristics of the PMD sublayer (including MDI) to the services expected by the Reconciliation Sublayer (RS) and the logical and electrical characteristics of the 10 Gigabit Media Independent Interface (XGMII). Although the XGMII is optional, it is used as the basis for the definition of the 10GBASE-X PCS and PMA sublayers.

10GBASE-X assumes the use of the MDIO interface and register set for communication between PHY and Station Management (STA) entities, see Clause 45.

10GBASE-X has the following characteristics:

- a) The capability of supporting 10 Gb/s operation at the XGMII and RS
- b) Clock references embedded in all data and control code-groups
- c) Data paths consisting of independent serial links called lanes
- d) Independent four-lane-wide transmit and receive data paths
- e) Simple signal mapping to the XGMII and RS
- f) Full duplex operation
- g) Shared technology with other 10 Gb/s interfaces
- h) Shared functionality with other 10 Gb/s Ethernet blocks

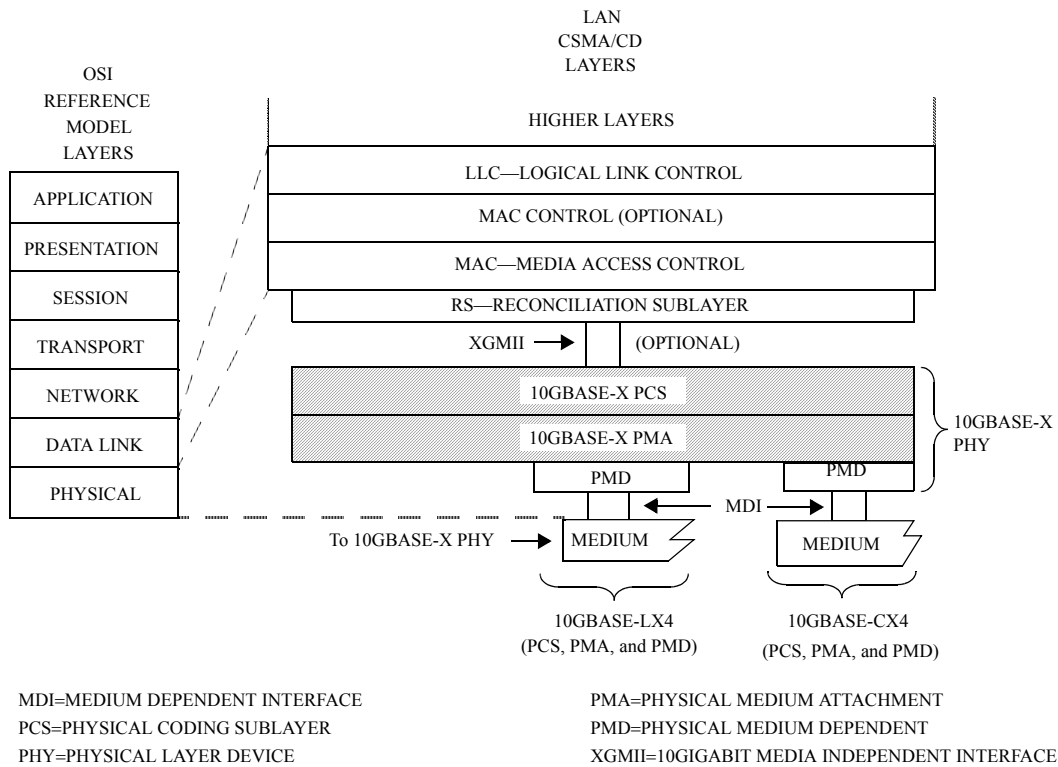
#### **48.1.1 Objectives**

The following are the objectives of 10GBASE-X:

- a) Support the IEEE 802.3 MAC
- b) Provide a data rate of 10 Gb/s at the XGMII
- c) Support cable plants using optical fiber compliant with second edition of ISO/IEC 11801: 1995
- d) Support a BER objective of  $10^{-12}$
- e) Support the optional XAUI
- f) Support link fault and error indications

### 48.1.2 Relationship of 10GBASE-X to other standards

Figure 48–1 depicts the relationships among the 10GBASE-X sublayers (shown shaded), the IEEE 802.3 MAC and RS, and the IEEE 802.2 LLC.



**Figure 48–1—10GBASE-X PCS and PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE CSMA/CD LAN Model**

### 48.1.3 Summary of 10GBASE-X sublayers

The following provides an overview of the 10GBASE-X sublayers.<sup>7</sup>

#### 48.1.3.1 Physical Coding Sublayer (PCS)

The interface between the PCS and the RS is the XGMII as specified in Clause 46. The 10GBASE-X PCS provides services to the XGMII in a manner analogous to how the 1000BASE-X PCS provides services to the 1000 Mb/s GMII.

The 10GBASE-X PCS provides all services required by the XGMII and in support of the 10GBASE-X PMA, including:

- Encoding of 32 XGMII data bits and 4 XGMII control bits to four parallel lanes conveying 10-bit code-groups each, for communication with the underlying PMA.
- Decoding of four PMA parallel lanes, conveying 10-bit code-groups each, to 32 XGMII data bits and 4 XGMII control bits.
- Synchronization of code-groups on each lane to determine code-group boundaries.

<sup>7</sup> The 10GBASE-X PHY consists of that portion of the Physical Layer between the MDI and XGMII consisting of the PCS, PMA, and PMD sublayers. The 10GBASE-X PHY is roughly analogous to the 1000BASE-X PHY.



- d) Deskew of received code-groups from all lanes to an alignment pattern.
- e) Support of the MDIO interface and register set as specified in Clause 45 to report status and enable control of the PCS.
- f) Conversion of XGMII Idle control characters to (from) a randomized sequence of code-groups to enable serial lane synchronization, clock rate compensation and lane-to-lane alignment.
- g) Clock rate compensation protocol.
- h) Link Initialization based on the transmission and reception of the Idle sequence.
- i) Link status reporting for fault conditions.

#### 48.1.3.2 Physical Medium Attachment (PMA) sublayer

The PMA provides a medium-independent means for the PCS to support the use of a range of serial-bit-oriented physical media. The 10GBASE-X PMA performs the following functions:

- a) Mapping of transmit and receive code-groups between the PCS and PMA via the PMA service interface.
- b) Serialization (deserialization) of code-groups for transmission (reception) on the underlying serial PMD.
- c) Clock recovery from the code-groups supplied by the PMD.
- d) Mapping of transmit and receive bits between the PMA and PMD via the PMD service interface.
- e) Direct passing of signal\_detect from the PMD to the PCS through the PMA via the PMD and PMA service interfaces.

#### 48.1.3.3 Physical Medium Dependent (PMD) sublayer

10GBASE-X supports the PMD sublayer and MDI specified in Clause 53. The 10GBASE-LX4 PMD and 10GBASE-CX4 performs the following functions:

- a) Transmission of quad serial bit streams on the underlying medium.
- b) Reception of quad serial bit streams on the underlying medium.

#### 48.1.4 Rate of operation

The 10GBASE-X PCS and PMA support the 10 Gb/s MAC data rate. The line rate of each of four PMA lanes is 3.125 GBaud  $\pm$  100 ppm.

#### 48.1.5 Allocation of functions

PCS and PMA functions directly map onto the 10GBASE-X PMD, MDI and medium which attach, in turn, to another 10GBASE-X PHY. In addition, 10GBASE-X PCS and PMA functions embodied in the XGXS described in Clause 47 may be used to attach to alternate 10 Gb/s PHYs such as 10GBASE-R or 10GBASE-W.

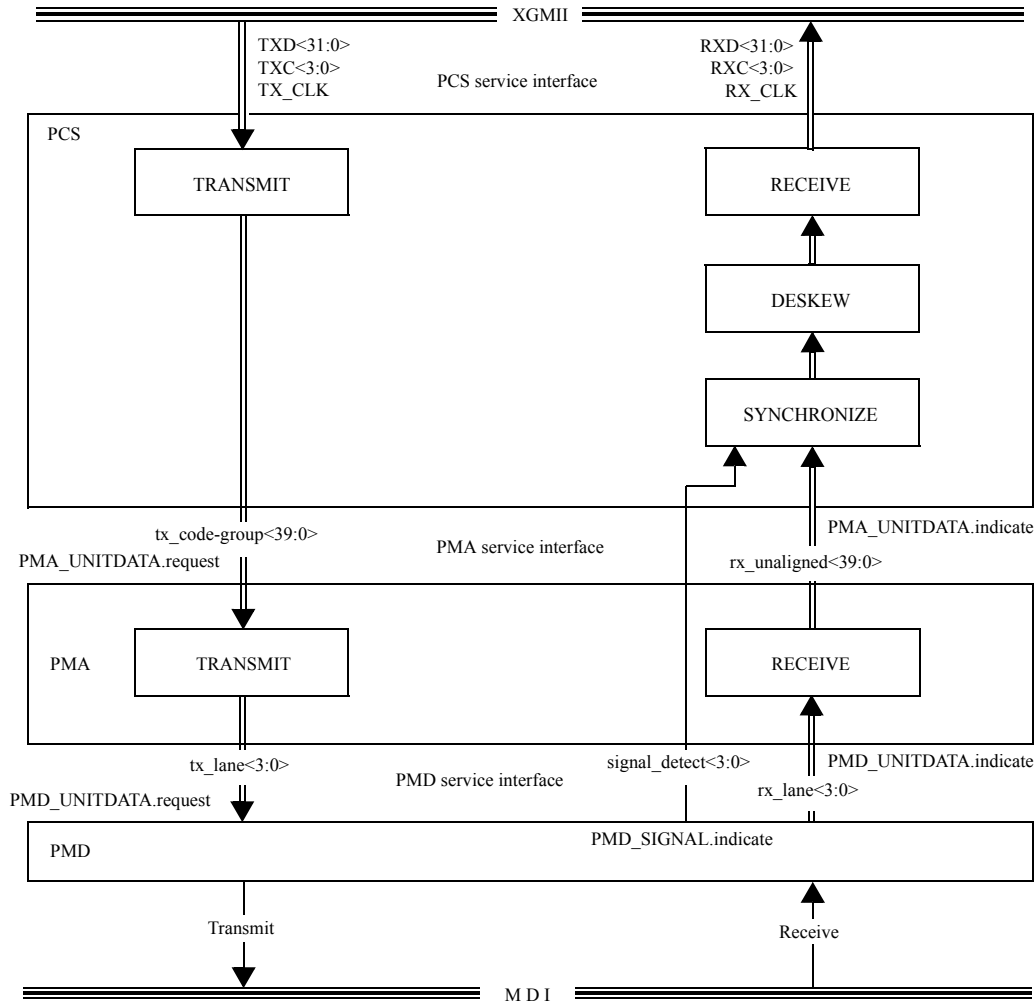
The longer interconnect distances afforded through the specification of a self-clocked serial architecture enable significant implementation flexibility while imposing a requirement on those implementations to ensure sufficient signal fidelity over the link. The implementer of this standard is expected to meet the required specifications in this and related clauses through implementation methods not specified by this standard.

#### 48.1.6 Inter-sublayer interfaces

There are a number of interfaces employed by 10GBASE-X. Some (such as the PMA service interface) use an abstract service model to define the operation of the interface. Figure 48–2 depicts the relationship and mapping of the services provided by all of the interfaces relevant to 10GBASE-X.

Multiple optional physical instantiations of the PCS service interface have been defined. One is the XGMII described in Clause 46. The other is the interface to the XGXS described in Clause 47.

Physical instantiations of the 10GBASE-X PMA and PMD service interfaces are not defined in this standard.



**Figure 48–2—Functional block diagram**

### 48.1.7 Functional block diagram

Figure 48–2 provides a functional block diagram of the 10GBASE-X PHY.

### 48.1.8 Special symbols

- /x/ The code-group x is represented by preceding and following slash characters.
- ||y|| Four code-groups, one each in lanes 0 through 3 inclusive, synchronous to each other and arranged in a column identified by the value y, is represented by preceding and following double bar characters.

## 48.2 Physical Coding Sublayer (PCS)

### 48.2.1 PCS service interface (XGMII)

The PCS service interface allows the 10GBASE-X PCS to transfer information to and from the PCS client. The PCS client is the RS defined in Clause 46, or the XGXS defined in Clause 47. An instantiation of the PCS service interface is the XGMII defined in Clause 46.

In the transmit direction, the 10GBASE-X PCS accepts packets from the PCS client on the XGMII. Due to the continuously signaled nature of the underlying PMA, and the encoding performed by the PCS, the 10GBASE-X PCS maps XGMII data and control characters into a code-group stream. In the receive direction, the PCS decodes the code-group stream received from the PMA, maps the code-groups to XGMII data and control characters and forwards the character stream to the XGMII to the PCS client for further processing.

### 48.2.2 Functions within the PCS

The PCS includes the Transmit, Receive, Synchronization, and Deskew processes for 10GBASE-X. The PCS shields the RS (and MAC) from the specific nature of the underlying channel.

When communicating with the XGMII, the PCS uses, in each direction, 32 data signals (TXD <31:0> and RXD <31:0>), four control signals (TXC <3:0> and RXC <3:0>), and a clock (TX\_CLK and RX\_CLK).

When communicating with the PMA, the PCS uses the data signals tx\_code-group <39:0> in the transmit direction and rx\_unaligned <39:0> in the receive direction. Each set of data signals conveys four lanes of 10-bit code-groups. At the PMA service interface, code-group alignment, lane-to-lane deskew, and provision for PHY clock rate compensation are made possible by embedding special non-data code-groups in the idle stream. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

The tx\_code-group and rx\_unaligned signals are organized into four lanes in a manner similar to that of the XGMII. On transmit, the first PCS code-group is aligned to lane 0, the second to lane 1, the third to lane 2, the fourth to lane 3, then repeating with the fifth to lane 0, etc. This lane-oriented organization extends through the PMA to the PMD service interface. (See Table 48–1.)

**Table 48–1—Transmit and receive lane associations**

Lane	XGMII TXD RXD	XGMII TXC RXC	PMA tx_code-group rx_unaligned	PMD tx_lane rx_lane
0	<7:0>	<0>	<9:0>	<0>
1	<15:8>	<1>	<19:10>	<1>
2	<23:16>	<2>	<29:20>	<2>
3	<31:24>	<3>	<39:30>	<3>

The PCS Transmit process continuously generates code-groups based upon the TXD <31:0> and TXC <3:0> signals on the XGMII, sending them to the PMA service interface via the PMA\_UNITDATA.request primitive.

The PCS Synchronization process continuously accepts unaligned and unsynchronized code-groups via the PMA\_UNITDATA.indicate primitive, obtains 10-bit code-group synchronization, and conveys synchronized 10-bit code-groups to the PCS Deskew process via the SYNC\_UNITDATA.indicate message. The PCS Synchronization process sets the lane\_sync\_status <3:0> flags to indicate whether the PMA is functioning dependably (as well as can be determined without exhaustive error-rate analysis).

The PCS Deskew process continuously accepts synchronized code-groups via the SYNC\_UNITDATA.indicate message, aligns the code-groups to remove skew between the lanes that has been introduced by the link, and conveys aligned and synchronized code-groups to the PCS Receive process via the ALIGN\_UNITDATA.indicate message. The PCS Deskew process asserts the align\_status flag to indicate that the PCS has successfully deskewed and aligned code-groups on all PCS lanes. The PCS Deskew process attempts deskew and alignment whenever the align\_status flag is de-asserted. The PCS Deskew process is otherwise idle.

The PCS Receive process continuously accepts code-groups from the PMA service interface via the ALIGN\_UNITDATA.indicate message. The PCS Receive process monitors these code-groups and generates RXD and RXC on the XGMII. All code-groups received that represent idle are replaced with Idle characters prior to forwarding to the XGMII.

The PCS Transmit and Receive processes provide support for Link status reporting, which supports the transmit fault and receive fault conditions.

All PCS processes are described in detail in the state diagrams in 48.2.6.2.

### **48.2.3 Use of code-groups**

The transmission code used by the PCS, referred to as 8B/10B, is identical to that specified in Clause 36. The PCS maps XGMII characters into 10-bit code-groups, and vice versa, using the 8B/10B block coding scheme. Implicit in the definition of a code-group is an establishment of code-group boundaries by a PCS Synchronization process. The 8B/10B transmission code as well as the rules by which the PCS ENCODE and DECODE functions generate, manipulate, and interpret code-groups are specified in 36.2.4. A 10GBASE-X PCS shall meet the requirements specified in 36.2.4.1 through 36.2.4.6, 36.2.4.8, and 36.2.4.9. PCS lanes are independent of one another. All code-group rules specified in 36.2.4 are applicable to each lane. The mapping of XGMII characters to PCS code-groups is specified in Table 48–2. The mapping of PCS code-groups to XGMII characters is specified in Table 48–3.

Figure 48–3 illustrates the mapping of an example XGMII character stream into a PCS code-group stream.

The relationship of code-group bit positions to XGMII, PCS and PMA constructs and PMD bit transmission order, exemplified for lane 0, is illustrated in Figure 48–4.

XGMII																	
T/RXD<7:0>	I	I	S	Dp	D	D	D	---	D	D	D	D	I	I	I	I	I
T/RXD<15:8>	I	I	Dp	Dp	D	D	D	---	D	D	D	T	I	I	I	I	I
T/RXD<23:16>	I	I	Dp	Dp	D	D	D	---	D	D	D	I	I	I	I	I	I
T/RXD<31:24>	I	I	Dp	Ds	D	D	D	---	D	D	D	I	I	I	I	I	I

PCS																		
LANE 0	K	R	S	Dp	D	D	D	---	D	D	D	D	A	R	R	K	K	R
LANE 1	K	R	Dp	Dp	D	D	D	---	D	D	D	T	A	R	R	K	K	R
LANE 2	K	R	Dp	Dp	D	D	D	---	D	D	D	K	A	R	R	K	K	R
LANE 3	K	R	Dp	Ds	D	D	D	---	D	D	D	K	A	R	R	K	K	R

Legend:  
 Dp represents a data character containing the preamble pattern  
 Ds represents a data character containing the SFD pattern

Figure 48–3—XGMII character stream to PCS code-group stream mapping example

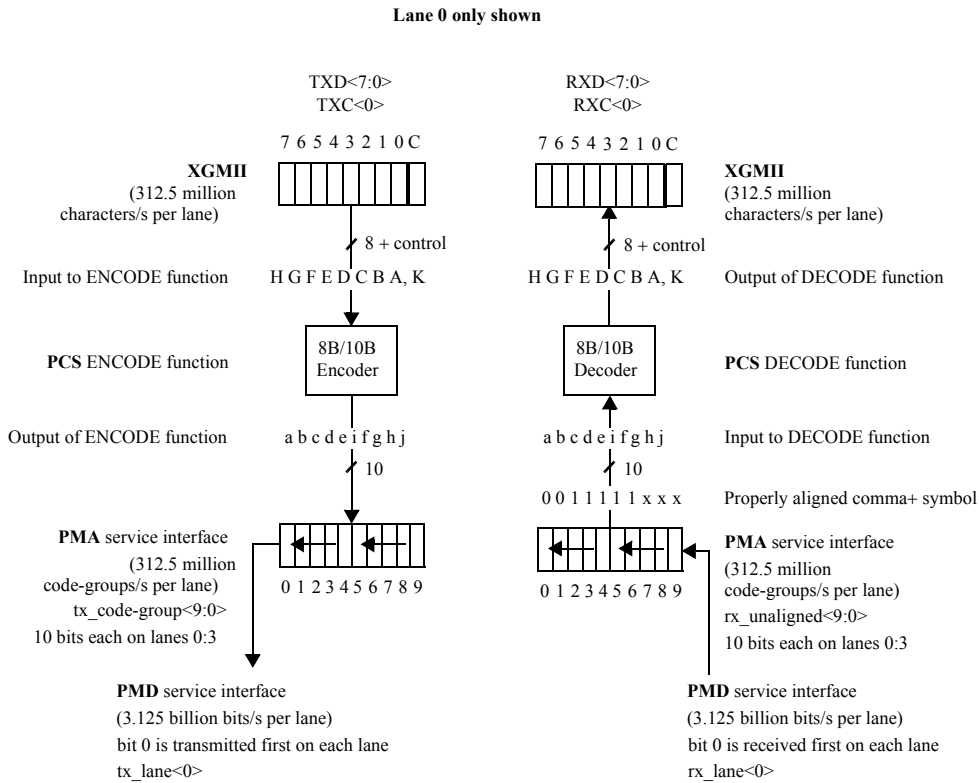


Figure 48–4—PCS reference diagram

#### 48.2.4 Ordered\_sets and special code-groups

10GBASE-X PCS ordered\_sets consist of combinations of special and data code-groups (defined as a column of code-groups). All ordered\_sets are four code-groups in length and begin in lane 0. In addition to ordered\_sets, the PCS defines several special code-groups for control purposes. Ordered\_sets and special code-groups provide the following capabilities:

- a) PCS Synchronization process ability to obtain bit and code-group synchronization
- b) Packet delineation
- c) Synchronization between the transmitter and receiver circuits at opposite ends of a link
- d) Deskew of received code-groups from all serial lanes to an alignment pattern
- e) Clock rate compensation protocol
- f) Link status reporting protocol
- g) Column fill
- h) Error indication

Table 48–4 lists the defined ordered\_sets and special code-groups.

**Table 48–2—XGMII character to PCS code-group mapping**

XGMII TXC	XGMII TXD	PCS code-group	Description
0	00 through FF	Dxx.y	Normal data transmission
1	07	K28.0 or K28.3 or K28.5	Idle in   I
1	07	K28.5	Idle in   T
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	Other value in Table 36-2	See Table 36-2	Reserved XGMII character
1	Any other value	K30.7	Invalid XGMII character

NOTE—Values in TXD column are in hexadecimal.

##### 48.2.4.1 Data (/D/)

A data code-group, when not used to distinguish or convey information for a defined ordered\_set, conveys one octet of data between the XGMII and the PCS. Any data code-group can be followed by any other data code-group. Data code-groups are encoded and decoded but not interpreted by the PCS.

##### 48.2.4.2 Idle (||I||)

Idle ordered\_sets (||I||) are transmitted in full columns continuously and repetitively whenever the XGMII is idle (TXD <31:0>=0x07070707 and TXC <3:0>=0xF). ||I|| provides a continuous fill pattern to establish and maintain lane synchronization, perform lane-to-lane deskew and perform PHY clock rate compensation. ||I|| is emitted from, and interpreted by, the PCS.

**Table 48–3—PCS code-group to XGMII character mapping**

XGMII RXC	XGMII RXD	PCS code-group	Description
0	00 through FF	Dxx.y	Normal data reception
1	07	K28.0 or K28.3 or K28.5	Idle in   I
1	07	K28.5	Idle in   T
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	FE	Invalid code-group	Received code-group
1	See Table 36-2	Other valid code-group	Received reserved code-group
NOTE—Values in RXD column are in hexadecimal.			

A sequence of ||I|| ordered\_sets consists of one or more consecutively transmitted ||K||, ||R|| or ||A|| ordered\_sets, as defined in Table 48–4. Rules for ||I|| ordered\_set sequencing shall be as follows:

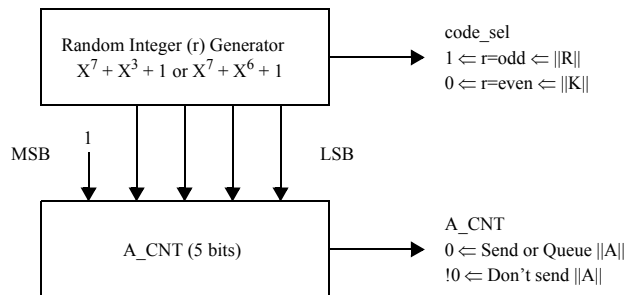
- ||I|| sequencing starts with the first column following a ||T||.
- The first ||I|| following ||T|| alternates between ||A|| or ||K|| except if an ||A|| is to be sent and less than r [see item d)] columns have been sent since the last ||A||, a ||K|| is sent instead.
- ||R|| is chosen as the second ||I|| following ||T||.
- Each ||A|| is sent after r non-||A|| columns where r is a uniform randomly distributed number between 16 and 31, inclusive. The corresponding minimum spacing of 16 non-||A|| columns between two ||A|| columns provides a theoretical 85-bit deskew capability.
- When not sending an ||A||, either ||K|| or ||R|| is sent with a random uniform distribution between the two.
- Whenever sync\_status=OK, all ||I|| received during idle are translated to XGMII Idle control characters for transmission over the XGMII. All other ||I|| received during idle are mapped directly to XGMII data or control characters on a lane by lane basis.

The purpose of randomizing the ||I|| sequence is to reduce 10GBASE-X electromagnetic interference (EMI) during idle. The randomized ||I|| sequence produces no discrete spectrum. Both ||A|| spacing as well as ||K||, ||R||, or ||A|| selection shall be based on the generation of a random integer r generated by a PRBS based on one of the 7th order polynomials listed in Figure 48–5. ||A|| spacing is set to the next generated value of r. The rate of generation of r is once per column, 312.5 MHz ± 100 ppm. Once the ||A|| spacing count goes to zero (A\_CNT=0), ||A|| is selected for transmission at the next opportunity during the Idle sequence. ||K|| and ||R|| selection follows the value of code\_sel, which is continuously set according to the even or odd value of r. The method of generating the random integer r is left to the implementer. PCS Idle randomizer logic is illustrated in Figure 48–5

**Table 48–4—Defined ordered\_sets and special code-groups**

Code	Ordered_Set	Number of code-groups	Encoding
I	<b>Idle</b>		<b>Substitute for XGMII Idle</b>
K	Sync column	4	/K28.5/K28.5/K28.5/K28.5/
R	Skip column	4	/K28.0/K28.0/K28.0/K28.0/
A	Align column	4	/K28.3/K28.3/K28.3/K28.3/
	<b>Encapsulation</b>		
S	Start column	4	/K27.7/Dx.y/Dx.y/Dx.y/ <sup>a</sup>
T	Terminate column	4	Terminate code-group in any lane
T <sub>0</sub>	Terminate in Lane 0	4	/K29.7/K28.5/K28.5/K28.5/
T <sub>1</sub>	Terminate in Lane 1	4	/Dx.y/K29.7/K28.5/K28.5/ <sup>a</sup>
T <sub>2</sub>	Terminate in Lane 2	4	/Dx.y/Dx.y/K29.7/K28.5/ <sup>a</sup>
T <sub>3</sub>	Terminate in Lane 3	4	/Dx.y/Dx.y/Dx.y/K29.7/ <sup>a</sup>
	<b>Control</b>		
/E/	Error code-group	1	/K30.7/
	<b>Link Status</b>		
Q	Sequence ordered_set	4	/K28.4/Dx.y/Dx.y/Dx.y/ <sup>a</sup>
LF	Local Fault signal	4	/K28.4/D0.0/D0.0/D1.0/
RF	Remote Fault signal	4	/K28.4/D0.0/D0.0/D2.0/
Qrsvd	Reserved	4	!  LF   and !  RF
	<b>Reserved</b>		
Fsig	Signal ordered_set	4	/K28.2/Dx.y/Dx.y/Dx.y/ <sup>a,b</sup>

<sup>a</sup>Dx.y/ indicates any data code-group.  
<sup>b</sup>Reserved for INCITS T11.



**Figure 48–5—PCS idle randomizer**



**48.2.4.2.1 Sync ||K||**

Code-group synchronization is the process by which the receiver detects code-group boundaries in the incoming bit stream of each lane. The detection of the comma pattern in the incoming bit stream identifies a code-group boundary. The proper alignment of a comma used for code-group synchronization is depicted in Figure 48–4. The Sync or ||K|| ordered\_set included in the PCS Idle sequence guarantees a sufficient frequency of commas in each lane. The comma pattern is defined in 36.2.4.9. The Sync ordered\_set is defined in Table 48–4. /K/ code-groups are interpreted per lane by the PCS Synchronization process which is described in 48.2.6.2.2. Detection of both comma+ and comma- variants of /K/ shall be required.

**48.2.4.2.2 Align ||A||**

Skew is introduced between lanes by both active and passive elements of a 10GBASE-X link. The PCS deskew function compensates for all lane-to-lane skew observed at the receiver. The Align or ||A|| ordered\_set consists of a unique special code-group, also known as Align or /A/ in each lane. /A/ is not used in any other ordered\_set. The definition of a 10GBASE-X ordered\_set guarantees that /A/ code-groups are simultaneously initiated on all lanes at the transmitter, resulting in minimal lane-to-lane skew at the transmitter. The Align ordered\_set is defined in Table 48–4. Allowable skew for all link elements shall be as specified in Table 48–5.

**Table 48–5—Skew budget**

Skew Source	#	Skew	Total Skew
PMA Tx	1	1 UI <sup>a</sup>	1 UI
PCB	2	1 UI	2 UI
Medium	1	<18 UI	<18 UI
PMA Rx <sup>b</sup>	1	20 UI	20 UI
Total			<41 UI
<sup>a</sup> UI represents unit interval. For 10GBASE-X, 1 UI = 320 ps. <sup>b</sup> Includes deserialization function, physical deserializer skew and clock boundary transition.			

**48.2.4.2.3 Skip ||R||**

The 10GBASE-X PHY allows for multiple clock domains along a single link. The Skip or ||R|| ordered\_set is included in the PCS Idle sequence to allow for clock rate compensation for the case of multiple clock domains. Clock rate compensation may be performed via insertion or removal of either Idle characters in the unencoded data stream or ||R|| in the encoded Idle stream. Any ||R|| may be removed. ||R|| may be inserted anywhere in the Idle stream with the exception of the first column following ||T||.

When clock compensation is done in the unencoded data stream, rules for idle insertion and deletion shall be as follows:

- Idle insertion or deletion occurs in groups of four Idle characters.
- Idle characters are added following idle or ordered\_sets.
- Idle characters are not added while data is being received.
- When deleting idles, the minimum IPG of five characters is maintained.

- e) Sequence ordered\_sets are deleted to adapt between clock rates.
- f) Sequence ordered\_set deletion occurs only when two consecutive sequence ordered\_sets have been received and deletes only one of the two.
- g) Only idles are inserted for clock compensation.

The disparity of the /R/ code-group is neutral, allowing its removal or insertion without affecting the current running disparity of the serial stream. The correct current running disparity version of /R/ must be inserted in each lane during Skip insertion (see Table 36-2). The Skip ordered\_set is defined in Table 48-4.

#### 48.2.4.3 Encapsulation

The Start and Terminate ordered\_sets correspond to columns containing the XGMII Start and Terminate control characters, respectively.

##### 48.2.4.3.1 Start ||S||

The Start or ||S|| ordered\_set directly maps to the XGMII Start control character in lane 0 followed by any three data characters in XGMII lanes 1 through 3. Normally, the three data characters will be the preamble pattern, but the PCS neither checks nor alters their contents. ||S|| indicates to the PCS that a packet has been initiated. The Start ordered\_set is defined in Table 48-4.

##### 48.2.4.3.2 Terminate ||T||

The Terminate or ||T|| ordered\_set directly maps to the XGMII Terminate control character located in any lane, preceded by data characters if Terminate is not in lane 0, and followed by Idle characters if Terminate is not in lane 3. ||T|| indicates to the PCS that a packet has been terminated. All XGMII control characters following ||T|| are translated by the PCS until the recognition of the next XGMII Start control character. The PCS considers the MAC interpacket gap (IPG) to have begun with the reception of ||T||. The Terminate ordered\_set is defined in Table 48-4.

Unrecognized running disparity errors which propagate to any Idle code-groups in ||T|| or to the column following ||T|| are indicated as /E/ in the preceding column in the same lane in which the errors were recognized. All ||I|| ordered\_sets are selected to ensure that propagated code violations are recognized and not propagated further.

The cvtx\_terminate function is used to convert all XGMII Idle control characters in the same column as the XGMII Terminate control character to /K/ code-groups. The cvrx\_terminate function is used to convert all /K/ code-groups in ||T|| to XGMII Idle control characters.

##### 48.2.4.4 Error /E/

The Error code-group is directly mapped to the XGMII Error control character. /E/ may also be generated by the PCS client to indicate a transmission error to its peer entity or deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability. Error is signaled per lane since code-violations are detected on a per lane basis. The Error code-group is defined in Table 48-4.

The presence of /E/ or any invalid code-group on the medium denotes an error condition. 10GBASE-X elements that detect code-group violations shall replace the invalid code-group with /E/ prior to retransmission.

#### 48.2.4.5 Link status

Link status reporting uses the Sequence ordered-set to transport the transmit fault and receive fault link status conditions.

##### 48.2.4.5.1 Sequence ||Q||

The Sequence or ||Q|| ordered\_set directly maps to the XGMII Sequence control character on lane 0 followed by three data characters in XGMII lanes 1 through 3. ||Q|| indicates to the PCS that a link status message has been initiated. The PCS Receive process may also initiate Sequence ordered-sets upon detection of a link status condition. Sequence ordered-sets are always sent over the PMA service interface in the column that follows an ||A|| ordered-set. The Sequence ordered-sets do not otherwise interfere with the randomized ||I|| sequence. Sequence ordered-sets corresponding to Local Fault signal and Remote Fault signal are specified in Table 48–4.

#### 48.2.5 Management function requirements

The 10GBASE-X PCS supports a set of required and optional management objects to permit it to be controlled by the Station Management entity (STA). Access to management objects within the 10GBASE-X sublayer is accomplished by means of a set of registers within the MDIO register space as defined in 45.2.4 and 45.2.5. The details of the register bit allocations and general usage are given in Clause 45. Table 48–6, Table 48–8, and Table 48–8 describe how the PCS state diagram variables map to management register bits. If an MDIO interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

**Table 48–6—State diagram variable to management register mapping for PCS**

State diagram variable	Management Register Bit
reset	3.0.15 Reset
sync_status	3.24.12 10GBASE-X lane alignment status
lane_sync_status<3>	3.24.3 Lane 3 sync
lane_sync_status<2>	3.24.2 Lane 2 sync
lane_sync_status<1>	3.24.1 Lane 1 sync
lane_sync_status<0>	3.24.0 Lane 0 sync

**Table 48–7—State diagram variable to management register mapping for PHY XS**

State diagram variable	Management Register Bit
reset	4.0.15 Reset
align_status	4.8.10 Receive local fault
sync_status	4.24.12 PHY XGXS lane alignment status
lane_sync_status<3>	4.24.3 Lane 3 sync
lane_sync_status<2>	4.24.2 Lane 2 sync
lane_sync_status<1>	4.24.1 Lane 1 sync
lane_sync_status<0>	4.24.0 Lane 0 sync

**Table 48–8—State diagram variable to management register mapping for DTE XS**

State diagram variable	Management Register Bit
reset	5.0.15 Reset
align_status	5.8.10 Receive local fault
sync_status	5.24.12 PHY XGXS lane alignment status
lane_sync_status<3>	5.24.3 Lane 3 sync
lane_sync_status<2>	5.24.2 Lane 2 sync
lane_sync_status<1>	5.24.1 Lane 1 sync
lane_sync_status<0>	5.24.0 Lane 0 sync

### 48.2.6 Detailed functions and state diagrams

The body of this clause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams in this clause follows the conventions in 21.5. State diagram variables follow the conventions of 21.5.2 except when the variable has a default value. Variables in a state diagram with default values evaluate to the variable default in each state where the variable value is not explicitly set.

Timeless states are employed as an editorial convenience to facilitate the distribution of transition conditions from prior states. No actions are taken within these states. Exit conditions are evaluated for timeless states. There is one timeless state. It is PCS Receive state RECEIVE.

#### 48.2.6.1 State variables

##### 48.2.6.1.1 Notation conventions

$/x/$

Denotes the constant code-group specified in 48.2.6.1.2 (valid code-groups must follow the rules of running disparity as per 36.2.4.5 and 36.2.4.6).

$[/x/]$

Denotes the latched received value of the constant code-group ( $/x/$ ) specified in 48.2.6.1.2 and conveyed by the SYNC\_UNITDATA.indicate message described in 48.2.6.1.6.

$||y||$

Denotes the column of constant code-groups in lanes 0 through 3, inclusively, specified in 48.2.6.1.2 (valid code-groups must follow the rules of running disparity as per 36.2.4.5 and 36.2.4.6).

$[[y]]$

Denotes the latched received value of the column of constant code-groups in lanes 0 through 3, inclusively ( $||y||$ ), specified in 48.2.6.1.2 and conveyed by the SYNC\_UNITDATA.indicate message described in 48.2.6.1.6 or the ALIGN\_UNITDATA.indicate message described in 48.2.6.1.6.

**48.2.6.1.2 Constants****/A/**

The /K28.3/ code-group used in the Idle Align function specified in 48.2.4.2.2.

**||A||**

The column of four identical Idle Align code-groups corresponding to the Idle Align function specified in 48.2.4.2.2.

**/COMMA/**

The set of special code-groups which include a comma as specified in 36.2.4.9 and listed in Table 36-2.

**/D/**

The set of 256 code-groups corresponding to valid data, as specified in 48.2.4.1 and listed in Table 36-1.

**||D||**

The column of four Data code-groups present during packet reception.

**/Dx.y/**

One of the set of 256 code-groups corresponding to valid data, as specified in 48.2.4.1 and listed in Table 36-1.

**/E/**

The /K30.7/ code-group corresponding to the Error function specified in 48.2.4.4.

**||I||**

The column of four identical Idle code-groups corresponding to the Idle function specified in 48.2.4.2. Also used to represent the corresponding XGMII control characters.

**||IDLE||**

Alias for ||I||.

**/INVALID/**

The set of invalid data or special code-groups, as specified in 36.2.4.6.

**/K/**

The /K28.5/ code-group used in the Idle Sync function specified in 48.2.4.2.1. Also used in the Terminate function specified in 48.2.4.3.2.

**||K||**

The column of four identical Idle Sync code-groups corresponding to the Idle Sync function specified in 48.2.4.2.1.

**/Kx.y/**

One of the set of 12 code-groups corresponding to valid special code-groups, as specified in Table 36-2.

**LFAULT**

A vector of bits RXD<31:0> and RXC<3:0> containing a Local Fault sequence ordered\_set. The Local Fault sequence ordered\_set is defined in 46.3.4.

**||Q||**

The column of four code-groups corresponding to the Sequence function specified in 48.2.4.5.1. Also used to represent the corresponding set of XGMII control and data characters.

**/R/**

The /K28.0/ code-group used for the Idle Skip function specified in 48.2.4.2.3.

- ||R||  
The column of four identical Idle Skip code-groups corresponding to the Idle Skip function specified in 48.2.4.2.3.
- ||S||  
The column of code-groups including the Start code-group as specified in 48.2.4.3.1. Also used to represent the corresponding set of XGMII control and data characters.
- ||T||  
The column of code-groups including the Terminate code-group as specified in 48.2.4.3.2. Also used to represent the corresponding XGMII control and data characters.

#### 48.2.6.1.3 Variables

- align\_column** <39:0>  
A vector of bits represented by the most recently received column of aligned 10-bit code-groups on all four lanes from the PCS Deskew process. For lane 0, the element **align\_column** <0> corresponds to the least recently received (oldest) **rx\_bit** of the code-group; **align\_column** <9> corresponds to the most recently received (newest) **rx\_bit** of the code-group. The same bit aging is applicable to the bits in **align\_column** <39:10> with respect to **rx\_lane** <3:1>. Code-group to lane assignment is specified in Table 48–1.
- align\_status**  
A parameter set by the PCS Deskew process to reflect the status of the lane-to-lane code-group alignment.  
Values: FAIL; The deskew process is not complete.  
OK; All lanes are synchronized and aligned.
- code\_sel**  
A boolean derived from a uniformly distributed random integer *r* generated by a PRBS based on a 7th order polynomial.  
Values: 0; LSB of random number is zero.  
1; LSB of random number is one.
- deskew\_error**  
A boolean used by the PCS Deskew process to indicate that a lane-to-lane alignment error has been detected.  
Values: FALSE; /A/ not recognized in any lane or recognized in all lanes simultaneously.  
TRUE; /A/ recognized in fewer than all lanes.
- enable\_calign**  
A boolean that indicates the enabling and disabling of code-group comma alignment. The code-group boundary may be changed whenever code-group comma alignment is enabled. This process is known as code-group alignment.  
Values: FALSE; Code-group alignment is disabled.  
TRUE; Code-group alignment is enabled.
- enable\_deskew**  
A boolean that indicates the enabling and disabling of the deskew process. Code-groups may be discarded whenever deskew is enabled. This process is known as code-group slipping.  
Values: FALSE; Deskew is disabled.  
TRUE; Deskew is enabled.

**IDLE**

A vector of bits RXD<31:0> and RXC<3:0> containing Idle. Idle is defined in Table 46-4.

**lane\_sync\_status <3:0>**

A parameter set by the PCS Synchronization process to reflect the status of the link for each lane as viewed by the receiver. lane\_sync\_status <n> represents lane\_sync\_status on lane n where n=0:3.

Values: FAIL; The receiver is not synchronized to the code-group boundary.  
OK; The receiver is synchronized to the code-group boundary.

**next\_ifg**

Controls the ||IDLE|| pattern immediately following the next frame. It is used to ensure an equal and deterministic presence of both ||A|| and ||K||

Values: A; The first ||IDLE|| following the end of the next frame will be ||A||.  
K; The first ||IDLE|| following the end of the next frame will be ||K||.

**reset**

Condition that is true until such time as the power supply for the device that contains the PCS has reached the operating region. The condition is also true when the device has low-power mode set via Control register bit 4.0.11 or 5.0.11. The condition is also true when a reset request is detected via Control register bit 4.0.15 or 5.0.15.

Values: FALSE; The device is completely powered and has not been reset (default).  
TRUE; The device has not been completely powered or has been reset.

NOTE—Reset evaluates to its default value in each state where it is not explicitly set.

**RX**

Alias for RXD <31:0> and RXC <3:0> representing the XGMII Receive Data and Control signals.

**RXC <3:0>**

Receive Control signals of the XGMII as specified in Clause 46. Set by the PCS Receive process.

**RXD <31:0>**

Receive Data signals of the XGMII as specified in Clause 46. Set by the PCS Receive process.

**rx\_lane <3:0>**

A vector of bits representing the serial lanes used to convey data from the PMD to the PMA via the PMD\_UNITDATA.indicate service primitive as specified in Clause 53.

Bit values: ZERO; Data bit is a logical zero.  
ONE; Data bit is a logical one.

**rx\_unaligned <39:0>**

A vector of bits represented by the most recently received column of unaligned 10-bit code-groups on all four lanes from the PMA. For lane 0, the element rx\_unaligned <0> is the least recently received (oldest) rx\_bit from the PMD; rx\_unaligned <9> is the most recently received (newest) rx\_bit from the PMD. The same bit aging is applicable to the bits in rx\_unaligned <39:10> with respect to rx\_lane <3:1>. Code-group to lane assignment is specified in Table 48-1.

signal\_detect <3:0>

A parameter set continuously and directly from the PMD\_SIGNAL.indicate(signal\_detect <3:0>) primitive to reflect the status of the incoming link signal for each lane. Used by the PCS Synchronization process to validate the data received on rx\_unaligned <39:0>. Signal\_detect <n> represents signal\_detect on lane n where n=0:3.

Values: FAIL; A signal is not present on the lane.  
OK; A signal is present on the lane.

sync\_code-group <39:0>

A vector of bits represented by the most recently received column of unaligned 10-bit code-groups on all four lanes from the PCS Synchronization process. For lane 0, the element sync\_code-group <0> corresponds to the least recently received (oldest) rx\_bit; sync\_code-group <9> corresponds to the most recently received (newest) rx\_bit. The same bit aging is applicable to the bits in sync\_code-group<39:10> with respect to rx\_lane <3:1>. Code-group to lane assignment is specified in Table 48–1.

sync\_status

A boolean that represents the following behavior: For all n in lane\_sync\_status<n>.

Values: FAIL; At least one lane is not in sync.  
OK; All lanes are in sync.

TQMSG

A vector of bits representing the last link status message received over the XGMII once the link status message is recognized. Used by the PCS Transmit process to load tx\_code-group <39:0>.

tx\_code-group <39:0>

A vector of bits representing a column of four aligned 10-bit code-groups which has been prepared for transmission by the PCS Transmit process. This vector is conveyed to the PMA as the parameter of a PMA\_UNITDATA.request(tx\_lane <3:0>) service primitive. For lane 0, the element tx\_code-group <0> is the first tx\_bit transmitted; tx\_code-group <9> is the last tx\_bit transmitted. The same bit aging is applicable to the bits in tx\_code-group <39:10> with respect to tx\_lane <3:1>. Code-group to lane assignment is specified in Table 48–1.

TX

Alias for either TXD <31:0> and TXC <3:0> representing the XGMII Transmit Data and Control signals, or the Local Fault ordered\_set as defined in 46.3.4 when a fault condition is detected on the transmit path.

TXC <3:0>

Transmit Control signals of the XGMII as specified in Clause 46. Interpreted by the PCS Transmit process.

TXD <31:0>

Transmit Data signals of the XGMII as specified in Clause 46. Interpreted by the PCS Transmit process.

tx\_lane <3:0>

A vector of bits representing the serial lanes used to convey data from the PMA to the PMD via the PMD\_UNITDATA.request service primitive as specified in Clause 53.

Bit values: ZERO; Data bit is a logical zero.  
ONE; Data bit is a logical one.



**48.2.6.1.4 Functions****check\_end**

Prescient Terminate function used by the PCS Receive process to set the RXD<31:0> and RXC<3:0> signals to indicate Error if a running disparity error was propagated to any Idle code-groups in ||T||, or to the column following ||T||. The XGMII Error control character is returned in all lanes less than n in ||T||, where n identifies the specific Terminate ordered-set ||T<sub>n</sub>||, for which a running disparity error or any code-groups other than /A/ or /K/ are recognized in the column following ||T||. The XGMII Error control character is also returned in all lanes greater than n in the column prior to ||T||, where n identifies the specific Terminate ordered-set ||T<sub>n</sub>||, for which a running disparity error or any code group other than /K/ is recognized in the corresponding lane of ||T||. For all other lanes the value set previously is retained.

**cvrx\_terminate**

Conversion function used by the PCS Receive process when Terminate is indicated to convert all /K/ code-groups to Idle control characters signaled via RX. Conversion is performed for all lanes.

**cvtx\_terminate**

Conversion function used by the PCS Transmit process when Terminate is indicated to convert all Idle control characters signaled via TX to /K/ code-groups. Conversion is performed for all lanes.

**DECODE ([[y]])**

Consists of four independent synchronous processes, one each per lane. In the PCS Receive process, this function takes as its arguments the latched value of align\_column ([[y]]) and the current running disparity, and returns XGMII RX as specified in 48.2.3 and 48.2.4. When decoding ||T||, the returned XGMII RX value is further modified by the cvrx\_terminate and check\_end functions, the result of the check\_end function takes priority over the result of the cvrx\_terminate function. DECODE also updates the current running disparity per the running disparity rules outlined in 36.2.4.4.

**ENCODE(TX)**

Consists of four independent synchronous processes, one each per lane. In the PCS Transmit process, this function takes as its argument the XGMII TX signals and the current running disparity for each lane, and returns four corresponding 10-bit code-groups as specified in 48.2.3 and 48.2.4. When encoding ||T||, the XGMII TX values are modified by the result of the cvtx\_terminate function. ENCODE also updates the current running disparity per Tables 36-1 or 36-2.

**Q\_det**

Function to determine the need to transmit sequence ordered\_sets. If TX=||Q|| then Q\_det is set to true and TQMSG is set to the result of ENCODE(TX). Q\_det remains true until set to false by the PCS transmit source state diagram. In the event that this function and the state diagram both attempt to modify Q\_det, the setting of Q\_det by this function to true will take priority.

**signal\_detectCHANGE <3:0>**

In the PCS Synchronization process, this function monitors the signal\_detect parameter on a per lane basis for a state change. The function is set upon state change detection, which is required to detect signal\_detect changes which occur asynchronously to PUDI. signal\_detectCHANGE <n> represents signal\_detectCHANGE on lane n where n=0:3.

Values: TRUE; The output of this function changes to true when the function detects a change in signal\_detect and stays true until the false condition is satisfied.  
FALSE; The output of this function changes to false when the LOSS\_OF\_SYNC state of the PCS synchronization state diagram is entered.

### 48.2.6.1.5 Counters

#### A\_CNT

A 5-bit down counter used to control Align code-group spacing. Loaded with a value between 16 and 31, inclusive, by a uniformly distributed random integer  $r$  generated by a PRBS based on a 7th order polynomial as described in 48.2.4.2. A\_CNT is decremented once per PUDR. The count remains at zero until  $\|A\|$  is transmitted, at which time a new value is loaded.

#### good\_cgs

A 2-bit consecutive valid code-groups received counter.

### 48.2.6.1.6 Messages

#### AUDI( $\|y\|$ )

Alias for ALIGN\_UNITDATA.indicate(parameters).

#### ALIGN\_UNITDATA.indicate([align\_column <39:0>])

A signal sent by the PCS Deskew process to the PCS Receive process conveying the latched value of the indicated column of code-groups over each lane ( $\|y\|$ ) (see 48.2.6.2.3).

#### PMA\_UNITDATA.indicate(rx\_unaligned <39:0>)

A signal sent by the PMA Receive process to the PCS Synchronization process conveying the next code-group set received over each lane of the medium (see 48.3.2.2).

#### PMA\_UNITDATA.request(tx\_code-group <39:0>)

A signal sent by the PCS Transmit process conveying the next code-group set for all lanes ready for transmission over the medium (see 48.3.2.1).

#### PMD\_SIGNAL.indicate(signal\_detect <3:0>)

Indicates the status of the incoming link signal. A signal mapped to the PMD\_SIGNAL.indicate(SIGNAL\_DETECT) service primitive specified in Clause 53. signal\_detect <n> is set to the same value for all lanes  $n$  where  $n=0:3$ .

Values: FAIL; A signal is not present on the lane.  
OK; A signal is present on the lane.

#### PUDI

Alias for PMA\_UNITDATA.indicate(parameters).

#### PUDR

Alias for PMA\_UNITDATA.request(parameters).

#### SUDI

Alias for SYNC\_UNITDATA.indicate(parameters).

#### SYNC\_UNITDATA.indicate(sync\_code-group <39:0>)

A signal sent by the PCS Synchronization process to the PCS Deskew process conveying code-groups over each lane (see 48.2.6.2.2).

### 48.2.6.2 State diagrams

#### 48.2.6.2.1 Transmit

The PCS shall implement its Transmit process as depicted in Figure 48–6, including compliance with the associated state variables as specified in 48.2.6.1. This state machine makes exactly one transition for each transmitted ordered\_set that is processed.

The Transmit Source process determines whether XGMII data and control information should be passed through to the PMA for serialization or converted before passing to the PMA. In all cases, XGMII data and control information is encoded before it is passed to the PMA. Data and control information may be sourced either directly from the XGMII or generated by the PCS depending on whether packet or Idle is being sourced by the XGMII. The recognition of the XGMII Start, Terminate, Idle and Sequence control characters is used to determine whether packet, Idle, or link status is being sourced by the XGMII.

The detection of a link status condition including the receipt of link status messages over the XGMII causes the PCS Transmit process to generate link status messages interspersed in an Idle sequence.

The PCS Transmit process continuously sources tx\_code-group<39:0> to the PMA. The Transmit process determines the proper code-group to source on each lane based on running disparity requirements.

#### 48.2.6.2.2 Synchronization

The PCS shall implement four Synchronization processes as depicted in Figure 48–7 including compliance with the associated state variables as specified in 48.2.6.1. The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. Failure of the underlying channel typically causes the PMA client to suspend normal actions. A Synchronization process operates independently on each lane, and synchronization is complete only when synchronization is acquired on all lanes. The synchronization process described in the following paragraphs applies to each lane.

The PCS Synchronization process continuously accepts code-groups via the PMA\_UNITDATA.indicate primitive and conveys received code-groups to the PCS Deskew process via the SYNC\_UNITDATA.indicate message.

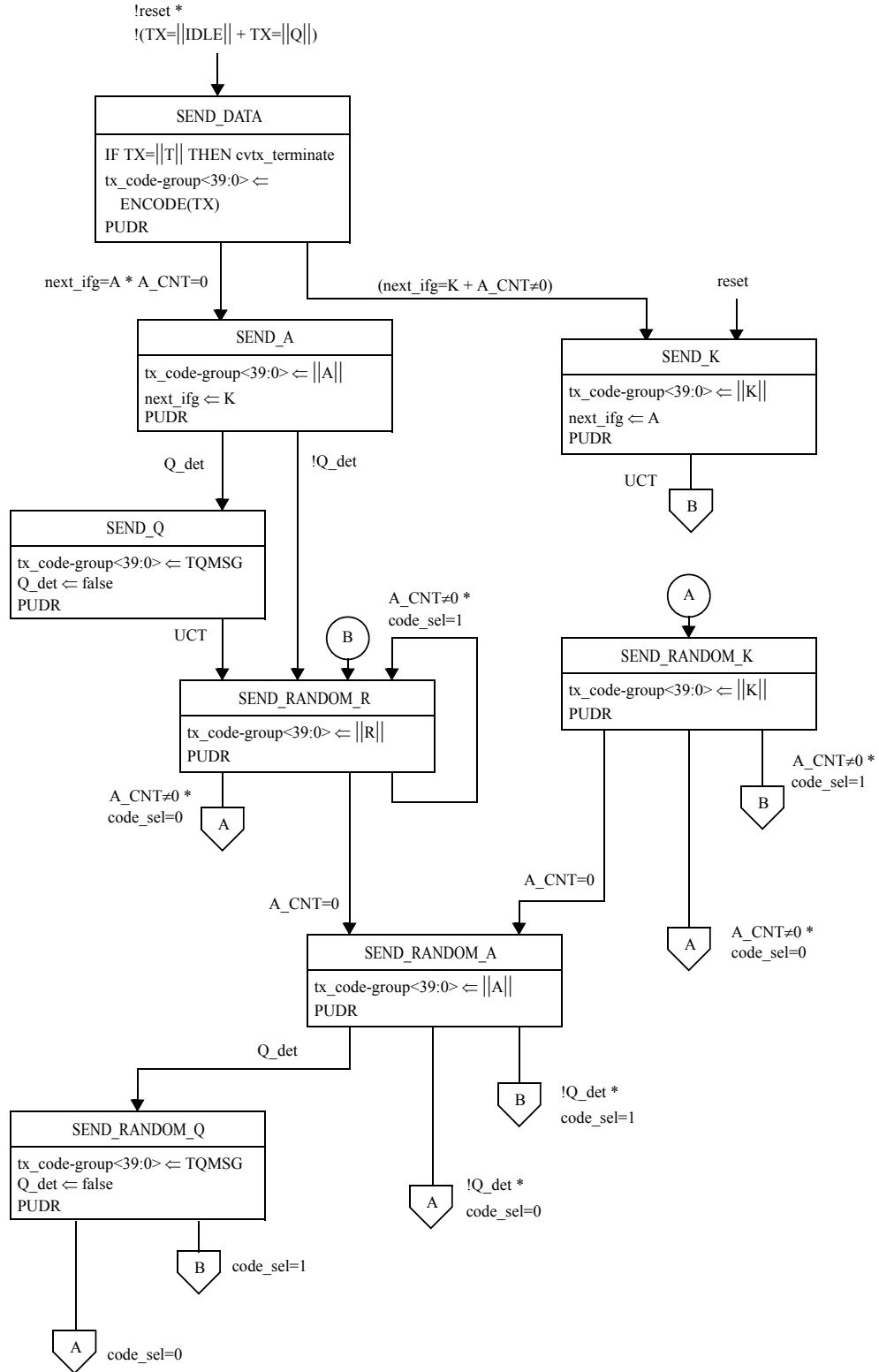
When in the LOSS\_OF\_SYNC state, the PCS may attempt to realign its current code-group boundary to one which coincides with the code-group boundary defined by a comma (see 36.2.4.9). This process is referred to in this document as code-group alignment.

Once synchronization is acquired, the Synchronization process tests received code-groups in sets of four code-groups and employs multiple sub-states, effecting hysteresis, to move between the SYNC\_ACQUIRED\_1 and LOSS\_OF\_SYNC states. The Synchronization process sets the lane\_sync\_status <3:0> flags to indicate whether the PMA is functioning dependably (as well as can be determined without exhaustive error-rate analysis). Whenever any PMA lane is not operating dependably, as indicated by the setting of lane\_sync\_status <3:0>, the align\_status flag is set to FAIL.

#### 48.2.6.2.3 Deskew

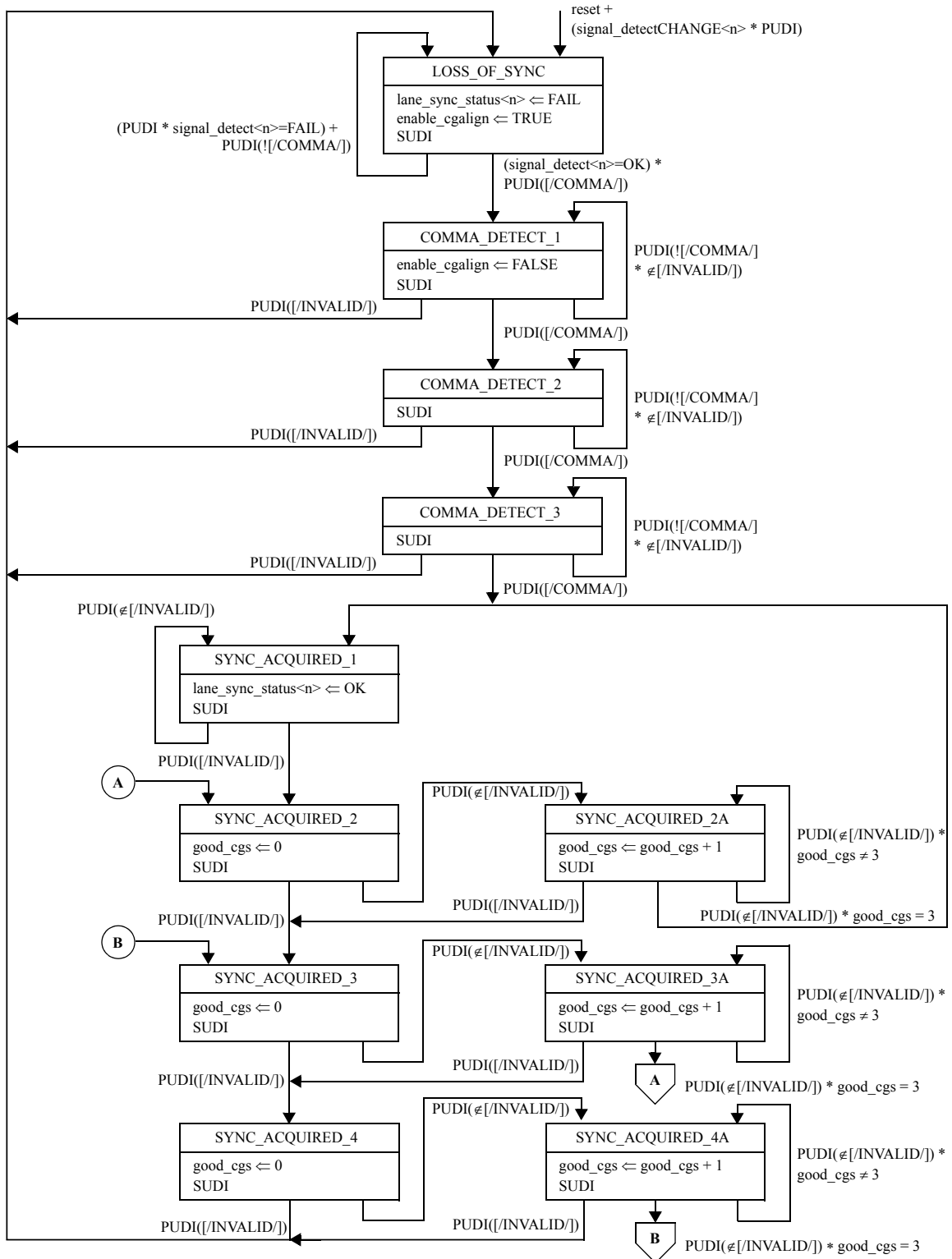
The PCS shall implement the Deskew process as depicted in Figure 48–8 including compliance with the associated state variables as specified in 48.2.6.1. The Deskew process is responsible for determining whether the underlying receive channel is capable of presenting coherent data to the XGMII. The Deskew process asserts the align\_status flag to indicate that the PCS has successfully deskewed and aligned code-groups on all lanes. The Deskew process attempts deskew and alignment whenever the align\_status flag is de-asserted. The Deskew process is otherwise idle. Whenever the align\_status flag is set to FAIL the condition is indicated as a link\_status=FAIL condition in the status register bit 4.1.2 or 5.1.2.

Once alignment is acquired, the Deskew process tests received columns and employs multiple sub-states, effecting hysteresis, to move between the ALIGN\_ACQUIRED\_1 and LOSS\_OF\_ALIGNMENT states. These states monitor the link for continued alignment, tolerate alignment inconsistencies due to a reasonably low BER, and restart the Deskew process if alignment can not be reliably maintained.



NOTE—The state machine makes exactly one transition for each transmit code-group processed.

**Figure 48–6—PCS transmit source state diagram**



NOTE— lane\_sync\_status<n>, signal\_detect<n> and signal\_detectCHANGE<n>, refer to the number of the received lane n where n=0:3

Figure 48-7—PCS synchronization state diagram

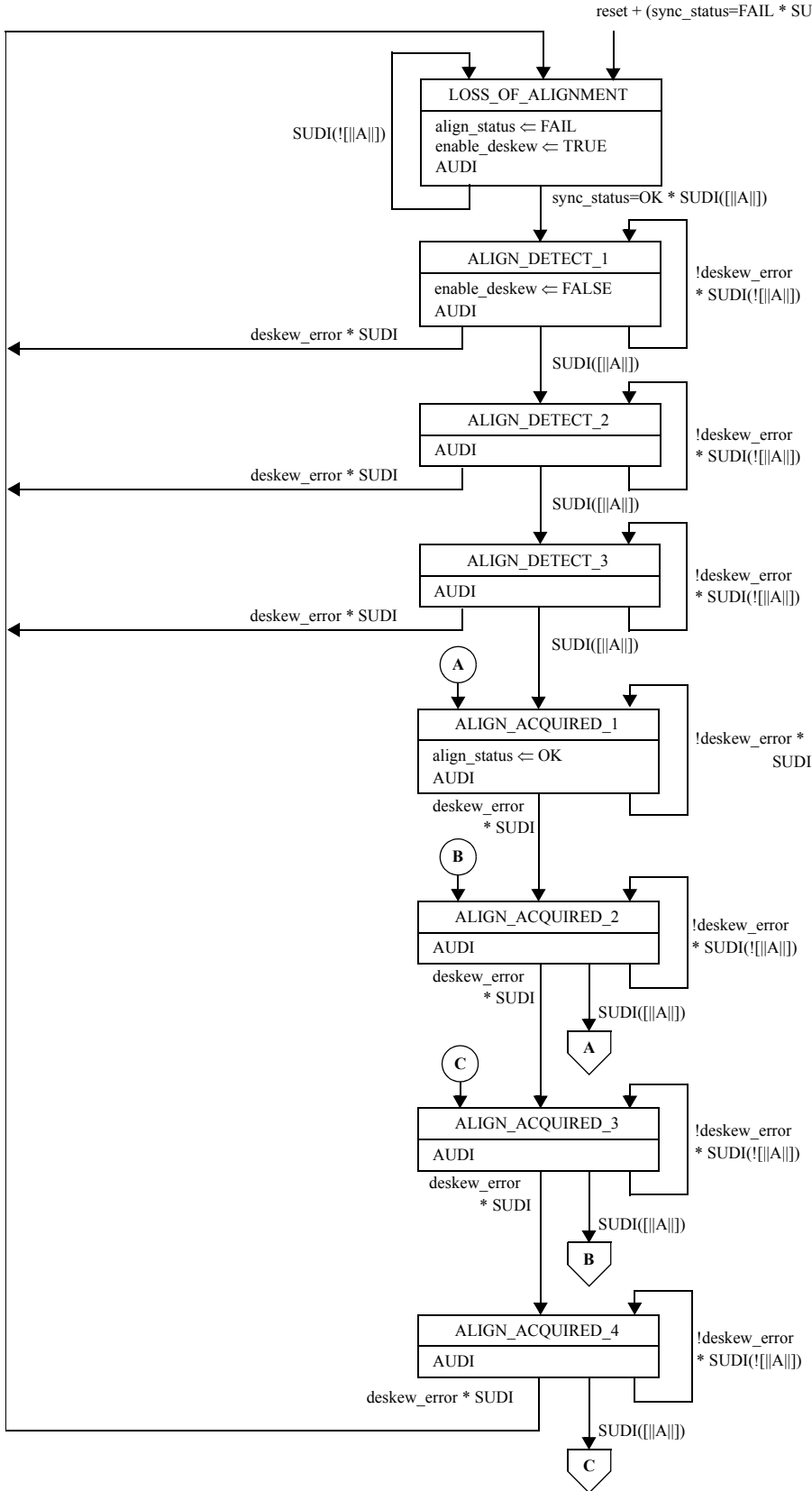


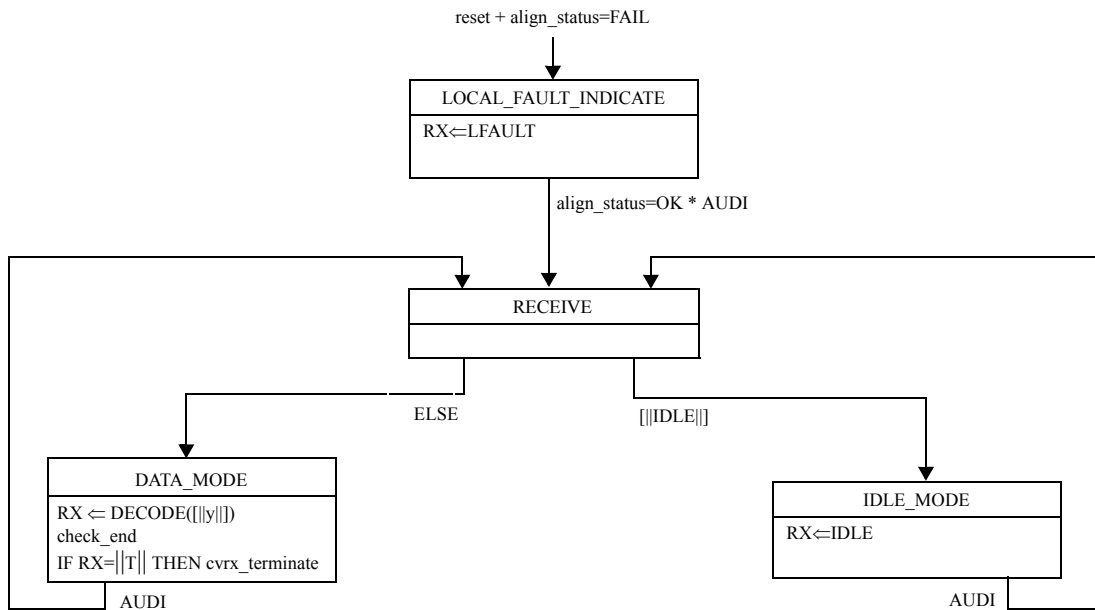
Figure 48–8—PCS deskew state diagram

**48.2.6.2.4 Receive**

The PCS shall implement its Receive process as depicted in Figure 48–9, including compliance with the associated state variables as specified in 48.2.6.1.

The PCS Receive process continuously performs the DECODE function on the received code-groups from the PCS Deskew Process via the ALIGNED\_UNITDATA.indicate message. The PCS Receive process generates the receive clock signal of the XGMII (RX\_CLK) as specified in Clause 46. State transitions in the PCS Receive state diagram that generate the data and control characters (RXD<31:0> and RXC<3:0>) on the XGMII occur synchronous to RX\_CLK. The Receive process operates in the following two modes:

- a) Data mode during packet reception including Start and Terminate. Additionally, Data mode is active whenever !||I|| columns are received during the Idle sequence or !||I|| or !||Q|| columns are received during the Fault sequence signifying either an error or unusual or unsupported indication. Valid code-groups received while in Data mode are mapped to corresponding XGMII data or control characters regardless of whether or not the control characters are valid XGMII control characters. Invalid or Error code-groups are mapped directly to XGMII Error control characters. All code-groups are mapped on a lane by lane basis.
- b) Idle mode during idle reception excluding Start and Terminate. Idle mode is active whenever ||I|| is received during idle reception. ||I|| is translated to XGMII Idle control characters.



**Figure 48–9—PCS receive state diagram**

**48.2.6.3 Initialization process**

Link initialization involves the completion of the PCS Synchronization and Deskew processes and the ability to transmit and receive code-groups via the PCS Transmit and Receive processes, respectively. The status register link\_status flag is set to OK whenever the align\_status flag is set to OK and no errors preventing link operation are present in the PCS or PMA.

#### **48.2.6.4 Link status reporting**

Link status reporting involves detection of link status conditions and the signaling of link fault status. The purpose of link status reporting is to quickly identify and convey link status conditions to the RS which can take the necessary action to activate (deactivate) the link via the setting of the RS link\_fault 2-bit variable. Link status reporting and MAC packet transmission is mutually exclusive.

##### **48.2.6.4.1 Link status detection**

10GBASE-X link status conditions include signal and deskew status conditions. Link status conditions include Local Fault and Remote Fault signals. A receive fault is recognized by the PCS Receive process whenever align\_status=FAIL. Other fault conditions are not detected by the PCS or PMA and are detected only by the RS. A fault condition may also be recognized by any 10GBASE-X process upon detection of an error condition, which prevents continued reliable operation, but this is beyond the scope of this standard.

##### **48.2.6.4.2 Link status signaling**

Link status signaling follows the detection or recognition of a link status condition and involves the generation of Sequence ordered-sets (||Q||) by the PCS Transmit process. Link status signaling involves the transmission of ||Q|| following ||A|| transmission in the Idle sequence as specified in 48.2.4.2.

##### **48.2.6.4.3 Link status messages**

A 10GBASE-X link status message is a Sequence ordered-set. Ordered-sets associated with link status messages are specified in Table 48–4. Link status messages detected by the PCS Receive process are forwarded to the XGMII.

### **48.3 Physical Medium Attachment (PMA) sublayer**

The PMA is specified in the form of a service interface to the PCS. These services are described in an abstract manner and do not imply any particular implementation. The PMA service interface supports the exchange of code-group information between PCS entities. The PMA converts code-groups into bits and passes these to the PMD, and vice versa.

#### **48.3.1 Functions within the PMA**

The PMA comprises the PMA Transmit process and PMA Receive process. Figure 48–4 depicts the mapping of the 36-bit-wide data and control path of the XGMII to the forty-bit-wide code-groups of the PMA service interface, and on to the four lane serial PMD service interface.

NOTE—Strict adherence to manufacturer-supplied guidelines for the operation and use of PMA serializer components is required to meet the jitter specifications of Clause 47 and Clause 53. The supplied guidelines should address the quality of power supply filtering associated with the transmit clock generator, and also the purity of the reference clock fed to the transmit clock generator.

##### **48.3.1.1 PMA transmit process**

The PMA Transmit process passes data unaltered (except for serializing) from the PCS directly to the PMD. Upon receipt of the PMA\_UNITDATA.request primitive, the PMA shall individually serialize the four aligned 10-bit code-groups, one from each of four lanes, and transmit them to the PMD in the form of forty PMD\_UNITDATA.request primitives, 10 each on four lanes.

Within each lane for each 10-bit code-group, the lowest numbered bit of the PMA\_UNITDATA.indicate parameter corresponds to the first bit transmitted to the PMD and the highest numbered bit of the



PMA\_UNITDATA.indicate parameter corresponds to the last bit transmitted to the PMD. There is no numerical significance ascribed to the bits within a PMA code-group; that is, the code-group is simply a bit pattern that has some predefined interpretation. PMA to PMD bit and lane association is illustrated in Table 48–1. PMA to PMD bit ordering is illustrated in Figure 48–4.

PMA\_UNITDATA.request primitives shall be generated with a frequency of  $312.5 \text{ MHz} \pm 100 \text{ ppm}$ . An internal clock multiplier unit multiplies the frequency of the 10-bit code-group based PMA\_UNITDATA.request primitives by a factor of 10 to serialize the latched data out of the PMA and into the PMD.

### 48.3.1.2 PMA receive process

The PMA Receive process passes data unaltered (except for deserializing) from the PMD directly to the PCS. Upon receipt of forty PMD\_UNITDATA.indicate primitives, 10 in succession from each of four lanes, the PMA shall assemble the bits received into a 40-bit vector representing four 10-bit unaligned code-groups and pass that vector to the PCS as the parameter of four PMA\_UNITDATA.indicate primitives.

Within each lane for each 10-bit code-group, the lowest numbered bit of the PMA\_UNITDATA.indicate parameter corresponds to the first bit received from the PMD and the highest numbered bit of the PMA\_UNITDATA.indicate parameter corresponds to the last bit received from the PMD. There is no numerical significance ascribed to the bits within a PMA code-group; that is, the code-group is simply a bit pattern that has some predefined interpretation. Receive code-group alignment is performed by the PCS and is not applicable to PMA. PMA to PMD bit and lane association is illustrated in Table 48–1. PMA to PMD bit ordering is illustrated in Figure 48–4.

PMA\_UNITDATA.indicate primitives shall be generated with a frequency of  $312.5 \text{ MHz} \pm 100 \text{ ppm}$ . The line rate of each of four PMD lanes is  $3.125 \text{ GBaud} \pm 100 \text{ ppm}$ . The serial data stream of the PMD includes an embedded clock that nominally operates at a frequency 10 times higher than that of a single lane code-group stream. The PMA Receive process shall recover a clock from a valid 8B/10B received data stream if the stream is within tolerance.

### 48.3.2 Service interface

The following primitives are defined:

```
PMA_UNITDATA.request(tx_code-group <39:0>)
PMA_UNITDATA.indicate(rx_unaligned <39:0>)
```

#### 48.3.2.1 PMA\_UNITDATA.request

This primitive defines the transfer of data in the form of aligned code-groups from the PCS to the PMA. PMA\_UNITDATA.request is generated by the PCS Transmit process.

##### 48.3.2.1.1 Semantics of the service primitive

```
PMA_UNITDATA.request(tx_code-group <39:0>)
```

The data conveyed by PMA\_UNITDATA.request is the tx\_code-group <39:0> parameter defined in 48.2.6.1.3.

#### **48.3.2.1.2 When generated**

The PCS continuously sends tx\_code-group <39:0> to the PMA at a nominal rate of 312.5 MHz  $\pm$  100 ppm, as governed by frequency and tolerance of XGMII TX\_CLK.

#### **48.3.2.1.3 Effect of receipt**

Upon receipt of this primitive, the PMA generates a series of forty PMD\_UNITDATA.request primitives, 10 for each of the four PMD lanes, tx\_lane <3:0>, requesting the four lane serial transmission of tx\_code-group <39:0> to the PMD.

#### **48.3.2.2 PMA\_UNITDATA.indicate**

This primitive defines the transfer of data in the form of code-groups from the PMA to the PCS. PMA\_UNITDATA.indicate is used by the PCS Synchronization process.

##### **48.3.2.2.1 Semantics of the service primitive**

PMA\_UNITDATA.indicate(rx\_unaligned <39:0>)

The data conveyed by PMA\_UNITDATA.indicate is the rx\_unaligned <39:0> parameter defined in 48.2.6.1.3.

##### **48.3.2.2.2 When generated**

The PMA continuously sends rx\_unaligned <39:0> to the PCS at a nominal rate of 312.5 MHz  $\pm$  100 ppm, as governed by frequency and tolerance of PMD\_UNITDATA.indicate.

##### **48.3.2.2.3 Effect of receipt**

Upon receipt of this primitive, the PCS Synchronization process attempts to achieve code-group synchronization on each lane (see 48.2.6.2.2).

#### **48.3.3 Loopback mode**

Loopback mode shall be provided for the 10GBASE-X PMA and DTE XGXS, and optionally for the PHY XGXS, as specified in this subclause, by the transmitter and receiver of a device as a test function to the device. When Loopback mode is selected, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. A device is explicitly placed in Loopback mode (i.e., Loopback mode is not the normal mode of operation of a device). Loopback applies to all lanes as a group (i.e., the lane 0 transmitter is directly connected to the lane 0 receiver, the lane 1 transmitter is directly connected to the lane 1 receiver, etc.). The method of implementing Loopback mode is not defined by this standard.

Control of the Loopback function may be supported through the MDIO management interface of Clause 45 or equivalent.

NOTE—The signal path that is exercised in the Loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this Loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

#### **48.3.3.1 Receiver considerations**

Entry into or exit from Loopback mode may result in a temporary loss of synchronization.

#### **48.3.3.2 Transmitter considerations**

While in Loopback mode, the transmitter output is not defined.

#### **48.3.4 Test functions**

A limited set of test functions may be provided as an implementation option for testing of the transmitter function or for testing of an attached receiver.

Some test functions that are not defined by this standard may be provided by certain implementations. Compliance with the standard is not affected by the provision or exclusion of such functions by an implementation. Random jitter test patterns for 10GBASE-X are specified in Annex 48A. Test-pattern capability and selection is optional and supported via MDIO register bits defined in Clause 45. Jitter Test methodology for 10GBASE-X is specified in Annex 48B.

A typical test function is the ability to transmit invalid code-groups within an otherwise valid PHY bit stream. Certain invalid PHY bit streams may cause a receiver to lose word and/or bit synchronization. See ANSI X3.230-1994, FC-PH subclause 5.4 for a more detailed discussion of receiver and transmitter behavior under various test conditions.

### **48.4 Compatibility considerations**

There is no requirement for a compliant device to implement or expose any of the interfaces specified for the PCS or PMA. Implementations of an XGMII shall comply with the requirements as specified in Clause 46.

### **48.5 Delay constraints**

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sub-layer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of transmit and receive delay contributed by the 10GBASE-X PCS shall be no more than 2048 BT.

The reference point for all MDI measurements is the 50% point of the mid-cell transition corresponding to the reference bit, as measured at the MDI.

### **48.6 Environmental specifications**

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801: 1995.

## 48.7 Protocol Implementation Conformance Statement (PICS) proforma for Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X<sup>8</sup>

### 48.7.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ae-2002, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

### 48.7.2 Identification

#### 48.7.2.1 Implementation identification

Supplier <sup>1</sup>	
Contact point for enquiries about the PICS <sup>1</sup>	
Implementation Name(s) and Version(s) <sup>1,3</sup>	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Names(s) <sup>2</sup>	
<p>NOTES</p> <p>1—Required for all implementations.</p> <p>2—May be completed as appropriate in meeting the requirements for the identification.</p> <p>3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).</p>	

#### 48.7.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ae-2002, Clause 48, Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
<p>Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to the standard.)</p>	
Date of Statement	

<sup>8</sup>Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

**48.7.3 Major capabilities/options**

Item	Feature	Subclause	Value/Comment	Status	Support
MD	MDIO	45, 48.1.3.1	Registers and interface supported	O	Yes [ ] No [ ]
XGXS	Support of XAUI/XGXS	47, 48.1.5		O	Yes [ ] No [ ]
XGE	XGMII compatibility interface	46, 48.1.3.1	Compatibility interface is supported	O	Yes [ ] No [ ]
LX4	Support of 10GBASE-LX4 PMD	53, 48.1.3.3		O	Yes [ ] No [ ]
CX4	Support of 10GBASE-CX4 PMD	54, 48.1.3.3		O	Yes [ ] No [ ]

**48.7.4 PICS proforma tables for the PCS and PMA sublayer, type 10GBASE-X****48.7.4.1 Compatibility considerations**

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Jitter test patterns	48.3.4	As per Annex 48A	M	Yes [ ]
CC2	Environmental specifications	48.6		M	Yes [ ]

**48.7.4.2 PCS functions**

Item	Feature	Subclause	Value/Comment	Status	Support
CG	Code-group usage	48.2.3	PCS support of 8B/10B code-groups	M	Yes [ ]
IOS	I   sequencing rules	48.2.4.2	All rules apply	M	Yes [ ]
PRBS	Random integer generator	48.2.4.2	$X^7 + X^3 + 1$ or $X^7 + X^6 + 1$ . Used for   A   spacing. Optional and ancillary use for testing	M	Yes [ ]
CMA	Comma detection	48.2.4.2.1	comma+ and comma- for /K/	M	Yes [ ]
CKCU	Clock rate compensation in unencoded idle stream	48.2.4.2.3	Meets the requirements of 48.2.4.2.3	O	Yes [ ] No [ ]
ERR	Error indication	48.2.4.4	Replacement of invalid code-groups with /E/	M	Yes [ ]
TSD	Transmit state diagrams	48.2.6.2.1	Meets the requirements of Figures 48–6	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
SSD	Synchronization state diagram	48.2.6.2.2	Meets the requirements of Figure 48–7	M	Yes [ ]
DSD	Deskew state diagrams	48.2.6.2.3	Meets the requirements of Figure 48–8	M	Yes [ ]
RSD	Receive state diagrams	48.2.6.2.4	Meets the requirements of Figure 48–9	M	Yes [ ]

#### 48.7.4.3 PMA Functions

Item	Feature	Subclause	Value/Comment	Status	Support
PMAT	Transmit function	48.3.1.1	PMA_UNITDATA.request	M	Yes [ ]
TXRT	Transmit rate	48.3.1.1	3.125 GBaud $\pm$ 100 ppm	M	Yes [ ]
PMAR	Receive function	48.3.1.2	PMA_UNITDATA.indicate	M	Yes [ ]
RXRT	Receive rate	48.3.1.2	3.125 GBaud $\pm$ 100 ppm	M	Yes [ ]
CDR	Clock and data recovery	48.3.1.2	Required if line rate is within 3.125 GBaud $\pm$ 100 ppm	M	Yes [ ]

#### 48.7.4.4 Interface functions

Item	Feature	Subclause	Value/Comment	Status	Support
SKEW	Allowable lane skew	48.2.4.2.2	Table 48–5	M	Yes [ ]
LBXPMA	10GBASE-X PMA Loopback mode	48.3.3		M	Yes [ ]
LBDTE	DTE XGXS Loopback mode	48.3.3		M	Yes [ ]
LBPHY	PHY XGXS Loopback mode	48.3.3		O	Yes [ ]
DLY	Delay constraints	48.5	2048 BT	M	Yes [ ]

**54. Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4**

**54.1 Overview**

This clause specifies the 10GBASE-CX4 PMD (including MDI) and the baseband medium. In order to form a complete Physical Layer, the PMD shall be integrated with the appropriate physical sublayers (see Table 54-1) and with the management functions which are accessible through the Management Interface defined in Clause 45, all of which are hereby incorporated by reference.

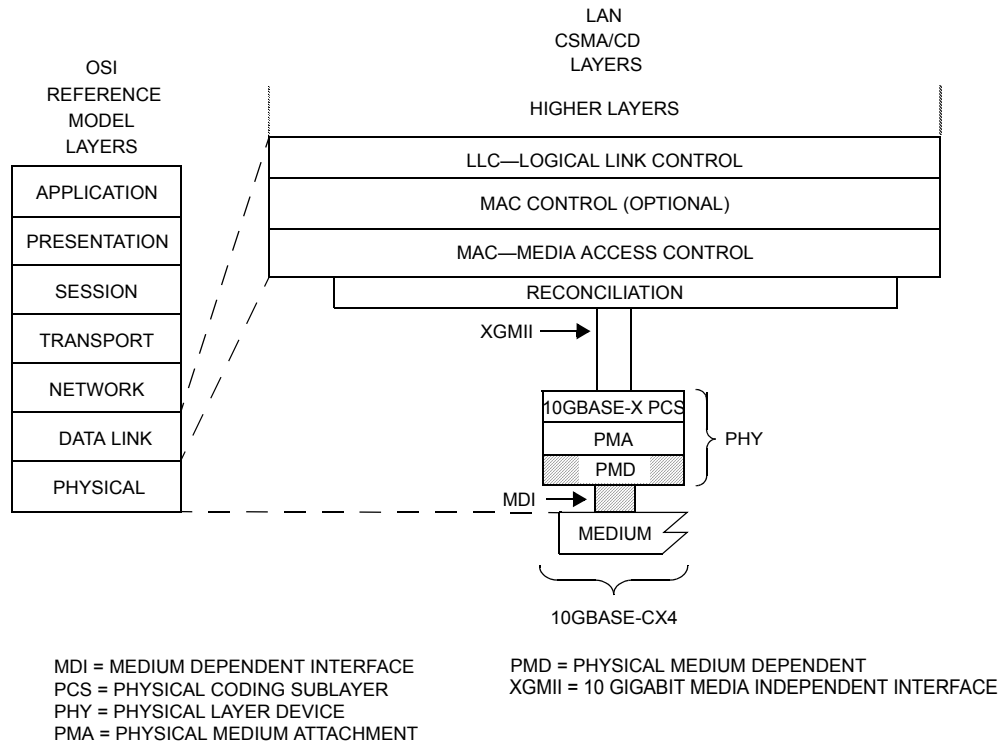
**Table 54-1—10GBASE-CX4 PMD type and associated physical layer clauses**

Associated Clause	10GBASE-CX4
46— XGMII <sup>a</sup>	Optional
47—XGXS and XAUI	Optional
48—10GBASE-X PCS/PMA	Required
49—10GBASE-R PCS	n/a
50—10GBASE-W WIS	n/a

<sup>a</sup>The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation must behave functionally as though the RS and XGMII were present.

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Figure 54–1 shows the relationship of the PMD and MDI sublayers to the ISO/IEC (IEEE) OSI reference model.



**Figure 54–1—10GBASE-CX4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model**

**54.1.1 Physical Medium Dependent (PMD) service interface**

This subclause specifies the services provided by the 10GBASE-CX4 PMD. The service interface for this PMD is described in an abstract manner and do not imply any particular implementation. The PMD Service Interface supports the exchange of encoded data between peer PMA entities. The PMD translates the encoded data to and from signals suitable for the specified medium.

The following PMD service primitives are defined:

- PMD\_UNITDATA.request
- PMD\_UNITDATA.indicate
- PMD\_SIGNAL.indicate

**54.1.2 PMD\_UNITDATA.request**

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMA to the PMD.

**54.1.2.1 Semantics of the service primitive**

- PMD\_UNITDATA.request (tx\_bit <0:3>)



1 The data conveyed by PMD\_UNITDATA.request is a continuous sequence of four parallel code-group  
2 streams, one stream for each lane. The tx\_bit <0:3> correspond to the bits in the tx\_lane<0:3> bit streams.  
3 Each bit in the tx\_bit parameter can take one of two values: ONE or ZERO.  
4

#### 5 **54.1.2.2 When generated**

6  
7 The PMA continuously sends four parallel code-group streams to the PMD at a nominal signaling speed of  
8 3.125 GBaud.  
9

#### 10 **54.1.2.3 Effect of Receipt**

11  
12 Upon receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals on  
13 the MDI.  
14

#### 15 **54.1.3 PMD\_UNITDATA.indicate**

16  
17 This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMD to the  
18 PMA.  
19

#### 20 **54.1.3.1 Semantics of the service primitive**

21  
22 PMD\_UNITDATA.indicate (rx\_bit <0:3>)

23  
24 The data conveyed by PMD\_UNITDATA.indicate is a continuous sequence of four parallel encoded bit  
25 streams. The rx\_bit<0:3> correspond to the bits in the rx\_lane<0:3> bit streams. Each bit in the rx\_bit  
26 parameter can take one of two values: ONE or ZERO.  
27

#### 28 **54.1.3.2 When generated**

29  
30 The PMD continuously sends stream of bits to the PMA corresponding to the signals received from the  
31 MDI.  
32

#### 33 **54.1.3.3 Effect of receipt**

34  
35 The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.  
36

#### 37 **54.1.4 PMD\_SIGNAL.indicate**

38  
39 This primitive is generated by the PMD to indicate the status of the signals being received from the MDI.  
40

#### 41 **54.1.4.1 Semantics of the service primitive**

42  
43 PMD\_SIGNAL.indicate (SIGNAL\_DETECT)

44  
45 The SIGNAL\_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL\_DETECT =  
46 FAIL, rx\_bit is undefined, but consequent actions based on PMD\_UNITDATA.indicate, where necessary,  
47 interpret rx\_bit as a logic ZERO.  
48

49 NOTE—SIGNAL\_DETECT = OK does not guarantee that rx\_bit is known to be good. It is possible for a poor quality  
50 link to provide sufficient power for a SIGNAL\_DETECT = OK indication and still not meet the  $10^{-12}$  BER objective.  
51

#### 52 **54.1.4.2 When generated**

53  
54 The PMD generates this primitive to indicate a change in the value of SIGNAL\_DETECT.

1 **54.1.4.3 Effect of receipt**

2  
3 The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

4  
5 **54.2 PCS and PMA functionality**

6  
7 The 10GBASE-CX4 PCS and PMA shall conform to the PCS and PMA defined in clause 48 unless other-  
8 wise noted herein.

9  
10 **54.3 Input / Output mapping**

11  
12 The 10GBASE-CX4 shall have the XAUI lane, as shown in Figure 47-2, to MDI connector pin mapping  
13 depicted in Table 54–2.

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17 **Table 54–2—XAUI lane to MDI connector pin mapping**

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XAUI Rx lane	MDI Connector pin	XAUI Tx lane	MDI Connector pin
DL0<p>	S1	SL0<p>	S16
DL0<n>	S2	SL0<n>	S15
DL1<p>	S3	SL1<p>	S14
DL1<n>	S4	SL1<n>	S13
DL2<p>	S5	SL2<p>	S12
DL2<n>	S6	SL2<n>	S11
DL3<p>	S7	SL3<p>	S10
DL3<n>	S8	SL3<n>	S9

35  
36 **54.4 Delay constraints**

37  
38 Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be  
39 an upper bound on the propagation delays through the network. This implies that MAC, MAC Control  
40 sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and  
41 administrators conform to constraints regarding the cable topology and concatenation of devices.

42  
43 The sum of transmit and receive delay contributed by the 10GBASE-CX4 PMD shall be no more than 512  
44 BT (including 1 meter of cable).

**54.5 PMD MDIO function mapping**

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. Mapping of MDIO control variables to PMD control variables is shown in Table 54–3. Mapping of MDIO status variables to PMD status variables is shown in Table 54–4.

**Table 54–3—MDIO/PMD control variable mapping**

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
Global transmit disable	Control register 1	1.9.0	Global_PMD_transmit_disable
Transmit disable 3	Transmit disable register	1.9.4	PMD_transmit_disable_3
Transmit disable 2	Transmit disable register	1.9.3	PMD_transmit_disable_2
Transmit disable 1	Transmit disable register	1.9.2	PMD_transmit_disable_1
Transmit disable 0	Transmit disable register	1.9.1	PMD_transmit_disable_0

**Table 54–4—MDIO/PMD status variable mapping**

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Local fault	Status register 1	1.1.7	PMD_fault
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD signal detect	Receive signal detect register	1.10.0	Global_PMD_signal_detect
PMD signal detect 3	Receive signal detect register	1.10.4	PMD_signal_detect_3
PMD signal detect 2	Receive signal detect register	1.10.3	PMD_signal_detect_2
PMD signal detect 1	Receive signal detect register	1.10.2	PMD_signal_detect_1
PMD signal detect 0	Receive signal detect register	1.10.1	PMD_signal_detect_0

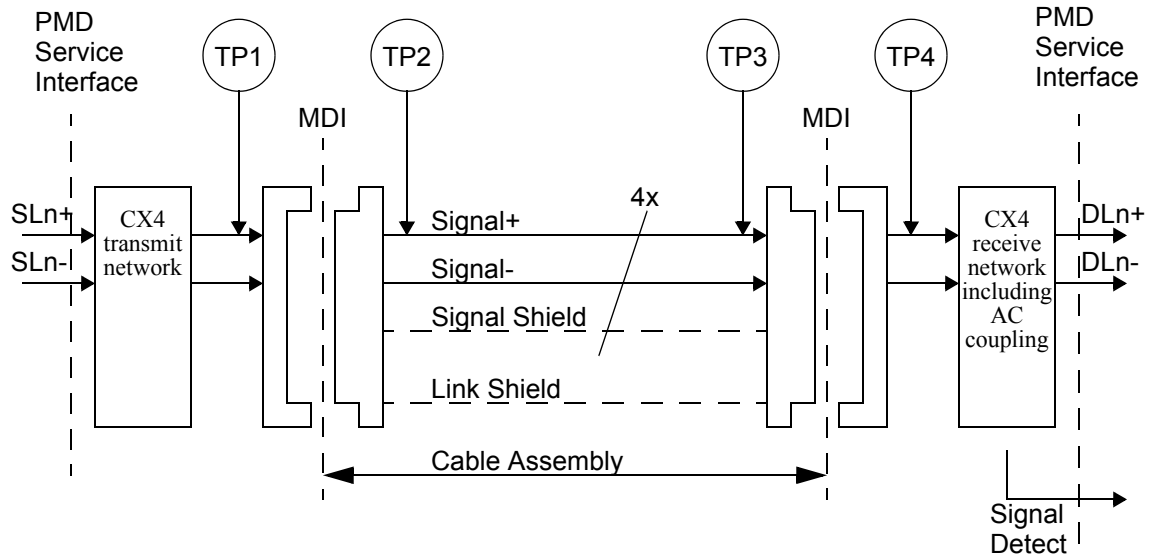
**54.6 PMD functional specifications**

The 10GBASE-CX4 PMD performs the Transmit and Receive functions which convey data between the PMD service interface and the MDI plus various management functions if the optional MDIO is implemented.

**54.6.1 PMD block diagram**

The PMD block diagram is shown in Figure 54–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The electrical transmit signal is defined at the output end of the connector (TP2). Unless specified otherwise, all transmitter measurements and tests defined in 54.7.3 are made at TP2. The electrical receive signal is defined at the output of the cabling connector (TP3). Unless specified otherwise, all receiver measurements and tests defined in 54.7.4 are made at TP3.

**Figure 54–2—10GBASE-CX4 link (half link is shown)**



Note: SLn+ and SLn- are the positive and negative sides of the transmit differential signal pair and DLn+ and DLn- are the positive and negative sides of the receive differential signal pair for Lane n (n = 0, 1, 2, 3)

**54.6.2 PMD transmit function**

The PMD Transmit function shall convert the four electronic bit streams requested by the PMD service interface message PMD\_UNITDATA.request (tx\_bit<0:3>) into four separate electrical signal streams. The four electrical signal streams shall then be delivered to the MDI, all according to the transmit electrical specifications in this clause. The higher output voltage of SLn+ minus SLn- (differential voltage) shall correspond to tx\_bit = ONE.

**54.6.3 PMD receive function**

The PMD Receive function shall convert the four electrical signal streams from the MDI into four electronic bit streams for delivery to the PMD service interface using the message PMD\_UNITDATA.indicate (rx\_bit<0:3>), all according to the receive electrical specifications in this clause. The higher electrical voltage level in each signal stream of DLn+ minus DLn- (differential voltage) shall correspond to a rx\_bit = ONE.

The PMD shall convey the bits received from the PMD\_UNITDATA.request(tx\_bit<0:3>) service primitive to the PMD service interface using the message PMD\_UNITDATA.indicate(rx\_bit<0:3>), where rx\_bit<0:3> = tx\_bit<0:3>.

**54.6.4 Global PMD signal detect function**

The Global\_PMD\_signal\_detect function shall report the state of SIGNAL\_DETECT via the PMD service interface. The SIGNAL\_DETECT parameter is signaled continuously, while the PMD\_SIGNAL.indicate message is generated when a change in the value of SIGNAL\_DETECT occurs.

SIGNAL\_DETECT shall be a global indicator of the presence of electrical signals on all four lanes. The PMD receiver is not required to verify whether a compliant 10GBASE-CX4 signal is being received, however, it shall be required to assert SIGNAL\_DETECT = OK when the differential peak-to-peak voltage on all four lanes at the MDI has exceeded 175mVppd. The transition from SIGNAL\_DETECT = FAIL to SIGNAL\_DETECT = OK shall occur within 100µs after the condition for SIGNAL\_DETECT = OK has been received.

The PMD receiver may assert SIGNAL\_DETECT = FAIL when the differential peak-to-peak voltage on all four lanes at the MDII has dropped below 50mVppd and has remained below 50mVppd for longer than 250µs. The PMD shall assert SIGNAL\_DETECT = FAIL when the differential peak-to-peak voltage on all four lanes at the MDI has dropped below 50mVppd and has remained below 50mVppd for longer than 500µs.

**Table 54–5—SIGNAL\_DETECT summary**

Parameter	Value	Units
SIGNAL_DETECT = OK level (maximum)	175	mVppd
SIGNAL_DETECT = OK assertion time (maximum)	100	µs
SIGNAL_DETECT = FAIL level (mimumum)	50	mVppd
SIGNAL_DETECT = FAIL de-assertion time		
maximum	500	µs
mimumum	250	µs

Note: The SIGNAL\_DETECT assertion time is recommended to be much faster than 100µs, however, this specification assumes measurement through the MII management interface and is thus limited by the sampling time required through that interface.

**54.6.5 PMD lane by lane signal detect function**

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD\_signal\_detect\_n, where n represents the lane number in the range 0:3, value shall be continuously set in response to the amplitude of the receive signal on its associated lane, according to the requirements of section 54.6.4.

**54.6.6 PMD reset function**

If the MDIO interface is implemented, and if PMD\_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

### 54.6.7 Global PMD transmit disable function

The Global\_PMD\_transmit\_disable function is optional and allows all of the transmitters to be disabled.

- a) When a Global\_PMD\_transmit\_disable variable is set to ONE, this function shall turn off all of the transmitters such that the each transmitter drives a constant logic level (i.e. no transitions) and meets the requirements of the absolute output voltage limits in Table 54–6.
- b) If a PMD\_fault is detected, then the PMD may set the Global\_PMD\_transmit\_disable to ONE, turning off the electrical transmitter in each lane.

### 54.6.8 PMD lane by lane transmit disable function

The PMD\_transmit\_disable\_n function allows the electrical transmitters in each lane to be selectively disabled.

- a) When a PMD\_transmit\_disable\_n variable is set to ONE, this function shall turn off the transmitter associated with that variable such that the each transmitter drives a constant logic level (i.e. no transitions) and meets the requirements of the absolute output voltage limits in Table 54–6.
- b) If a PMD\_fault is detected, then the PMD may set each PMD\_transmit\_disable\_n to ONE, turning off the electrical transmitter in each lane.

If the PMD\_transmit\_disable\_n function is not implemented in MDIO, an alternative method shall be provided to independently disable each transmit lane.

### 54.6.9 Loopback mode

Loopback mode shall be provided for the 10GBASE-CX4 as specified in this subclause, by the transmitter and receiver of a device as a test function to the device. When Loopback mode is selected by setting either the loopback control bit of 1.0.0 or 3.0.14, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link and the transmitters shall be turned off such that the each transmitter drives a constant logic level (i.e. no transitions) and meets the requirements of the absolute output voltage limits in Table 54–6. A device is explicitly placed in Loopback mode (i.e., Loopback mode is not the normal mode of operation of a device). Loopback applies to all lanes as a group (i.e., the lane 0 transmitter is directly connected to the lane 0 receiver, the lane 1 transmitter is directly connected to the lane 1 receiver, etc.). The method of implementing Loopback mode is not defined by this standard.

Control of the Loopback function may be supported through the MDIO management interface of Clause 45 or equivalent.

NOTE—The signal path that is exercised in the Loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this Loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

### 54.6.10 PMD fault function

If the MDIO is implemented, and the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD\_fault to ONE.

### 54.6.11 PMD transmit fault function

If the MDIO is implemented, and the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD\_transmit\_fault variable to ONE.

**54.6.12 PMD receive fault function**

If the MDIO is implemented, and the PMD has detected a local fault on any receive lane, the PMD shall set the PMD\_receive\_fault variable to ONE.

**54.7 PMD to MDI Electrical specifications for 10GBASE-CX4**

**54.7.1 Signal levels**

The 10GBASE-CX4 MDI is a low swing AC coupled differential interface. AC coupling allows for interoperability between components operating from different supply voltages. Low swing differential signaling provides noise immunity and improved electromagnetic interference (EMI).

**54.7.2 Signal paths**

The 10GBASE-CX4 MDI signal paths are point-to-point connections. Each path corresponds to a 10GBASE-CX4 MDI lane and is comprised of two complementary signals making a balanced differential pair. There are four differential paths in each direction for a total of eight pairs, or sixteen connections. The signal paths are intended to operate up to approximately 15m over standard twinaxial cables as described in 54.8.

**54.7.3 Driver characteristics**

Transmitter characteristics shall be measured at TP2, unless otherwise noted, and are summarized in Table 54–6 and detailed in the following subclauses.

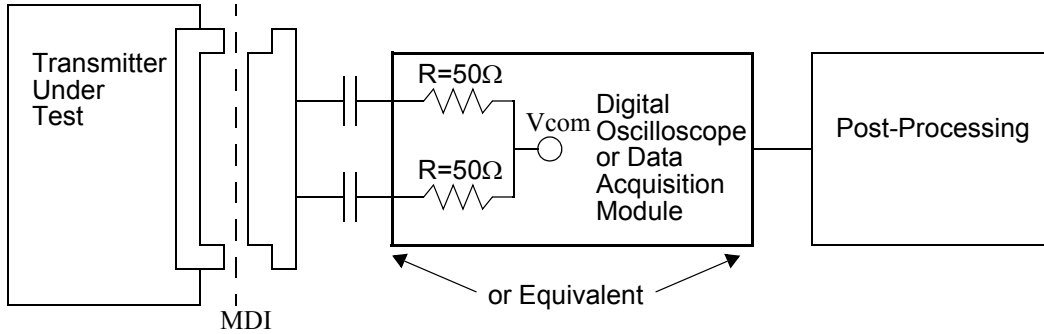
**Table 54–6—Driver characteristics’ summary**

Parameter	Subclause reference	Value	Units
Baud rate tolerance	54.7.3.3	3.125 GBd ± 100 ppm	GBd ppm
Unit interval nominal	54.7.3.3	320	ps
Differential peak amplitude maximum minimum	54.7.3.4	1600 TBD (750?)	mV <sub>pp</sub> mV <sub>pp</sub>
Absolute output voltage limits maximum minimum	54.7.3.4	2.3 –0.4	V V
Differential output return loss minimum	54.7.3.5	[See Equation (54.1a) and (54.1b)]	dB
Differential output template	54.7.3.6	[See figure (54–5) and table (54–7)]	V
Transition time maximum minimum	54.7.3.7	130 60	ps ps
Output jitter Random jitter Deterministic jitter Total jitter	54.7.3.8	± 0.090 peak from the mean ± 0.085 peak from the mean ± 0.175 peak from the mean	UI UI UI

1 **54.7.3.1 Test Fixtures**

2  
3 The following fixture (illustrated by Figure 54–3), or its functional equivalent, shall be used for measuring  
4 the transmitter specifications described in 54.7.3. The transmitter under test includes the driver, pcb traces,  
5 any AC coupling components and the MDI connector described in 54.9.1  
6

7 **Figure 54–3—Transmit Test Fixture**



21 **54.7.3.2 Load**

22  
23 The load shall be  $100 \Omega \pm 1\%$  from 100MHz to 2.0 GHz for these measurements, unless otherwise noted.  
24

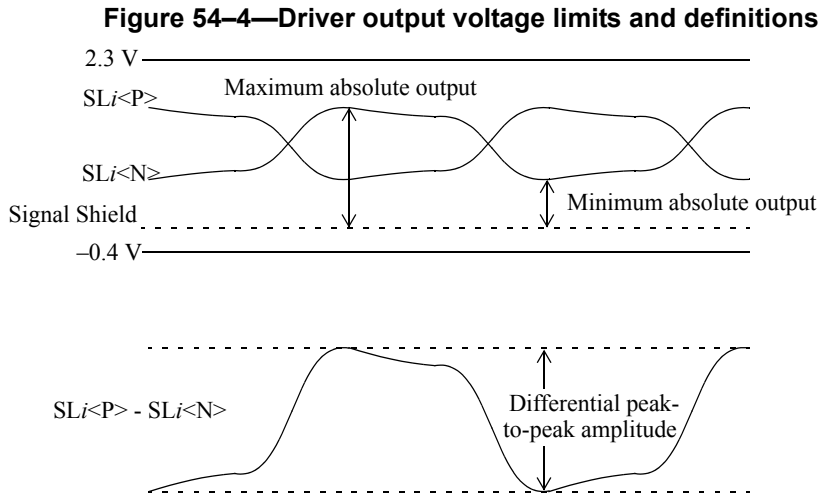
25 **54.7.3.3 Baud rate tolerance**

26  
27 The 10GBASE-CX4 MDI Baud shall be 3.125 GBaud  $\pm 100$  ppm. The corresponding Baud period is nomi-  
28 nally 320 ps.  
29

30 **54.7.3.4 Amplitude and swing**

31  
32 Driver differential output amplitude shall be less than  $1600 \text{ mV}_{p-p}$ . The minimum differential peak to peak  
33 output voltage shall be greater than TBD  $800 \text{ mV}_{p-p}$ . DC-referenced logic levels are not defined since the  
34 receiver is AC coupled. Absolute driver output voltage shall be between  $-0.4 \text{ V}$  and  $2.3 \text{ V}$  with respect to  
35 ground. See Figure 54–4 for an illustration of absolute driver output voltage limits and definition of differ-  
36 ential peak-to-peak amplitude.  
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Note: [SLi<P> and SLi<N> are the positive and negative sides of the differential signal pair for Lane *i* (*i*=0,1,2,3)]

**54.7.3.5 Output impedance**

For frequencies from 100MHz to 2.0 GHz, the differential return loss of the driver shall exceed Equation 54.1a and 54.1b. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100 Ω.

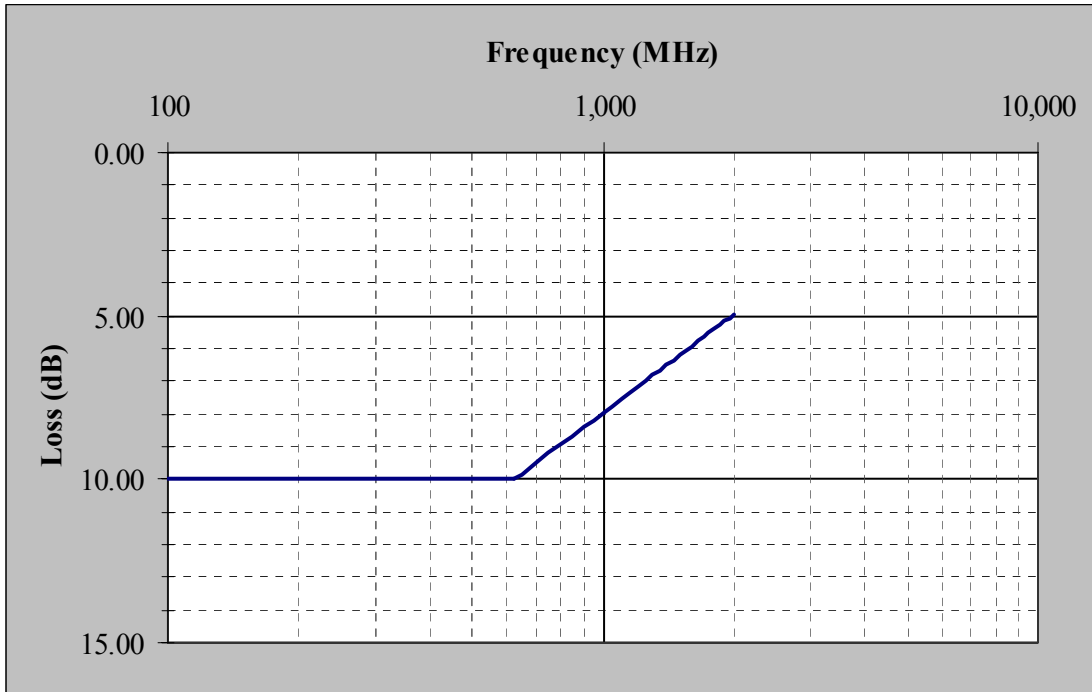
$$ReturnLoss(f) \leq 10 \tag{Eq. (54.1a)}$$

for 100 MHz ≤ f < 625MHz and

$$ReturnLoss(f) \leq 10 - 10 \times \log\left(\frac{f}{625}\right) \tag{Eq. (54.1b)}$$

for 625 MHz ≤ f < 200MHz.

**Figure 54–5—Transmit differential output return loss**



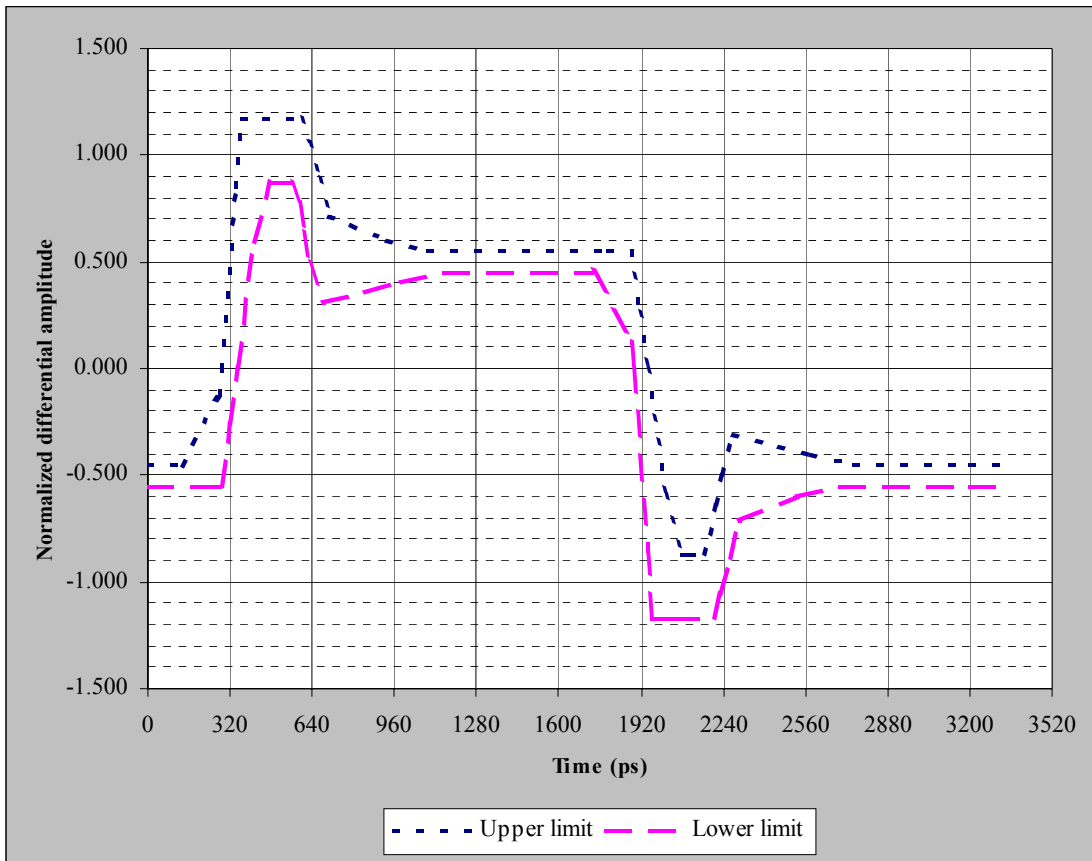
**54.7.3.6 Differential output template**

The differential output template shall be tested using the low frequency test pattern specified in Annex 48A.2. The waveform under test is normalized by using the following procedure:

- 1) Adjust the output waveform under test to fit as best as possible along the horizontal time axis.
- 2) Calculate the +1 low frequency level as  $V_{lowp}$  = average of any 2 continuous baud (640ps) between 800ps and 1760ps.
- 3) Calculate the -1 low frequency level as  $V_{lowm}$  = average of any 2 continuous baud (640ps) between 2400ps and 3360ps.
- 4) Calculate the verticle offset to be subtracted from the waveform as  $V_{off} = (V_{lowp} + V_{lowm}) / 2$ .
- 5) Calculate the verticle normilization factor from the waveform as  $V_{norm} = (V_{lowp} - V_{lowm}) / 2$ .
- 6) Calculate the normalized waveform as  $NormalizedWaveform = (OriginalWaveform - V_{off}) * (0.5 / V_{norm})$ .
- 7) Adjust the normalized output waveform under test to fit as best as possible along the horizontal time axis.

The differential voltage waveform shall lie within the time domain template defined in Figure 54–6 and the piece wise linear interpolation between the points in Table 54–7. These measurements are to be made for each pair while observing the differential signal output at the MDI using the transmitter test fixture.

Figure 54-6—Normalized transmit template as measured at MDI using Figure 54-3



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**Table 54–7—Normalized transmit time domain template**

Time (ps)	Upper limit	Time (ps)	Lower limit
0	-0.450	0	-0.550
131	-0.450	189	-0.550
283	-0.125	287	-0.550
283	-0.125	319	-0.266
291	0.000	349	0.000
343	0.850	414	0.586
363	1.175	477	0.870
451	1.175	509	0.870
602	1.175	565	0.870
629	1.060	591	0.776
669	0.888	611	0.635
709	0.715	631	0.494
709	0.715	685	0.306
931	0.600	989	0.400
1091	0.550	1149	0.450
1789	0.550	1731	0.450
1887	0.550	1883	0.125
1919	0.266	1883	0.125
1949	0.000	1891	0.000
2014	-0.586	1943	-0.850
2077	-0.870	1963	-1.175
2109	-0.870	2051	-1.175
2165	-0.870	2202	-1.175
2191	-0.776	2229	-1.060
2211	-0.635	2269	-0.888
2231	-0.494	2309	-0.715
2285	-0.306	2309	-0.715
2589	-0.400	2531	-0.600
2749	-0.450	2691	-0.550
3200	-0.450	3200	-0.550
3360	-0.450	3360	-0.550

NOTE—The ASCII for Table 54–7 is available from <http://www.ieee802.org/3/publication/index.html>. (Editor’s note: NEED correct url)

#### 54.7.3.7 Transition time

Differential transition times between 60 and 130 ps are recommended, as measured between the 20% and 80% levels. Shorter transitions may result in excessive high-frequency components and increase EMI and crosstalk. The upper recommended limit of 130 ps corresponds to a sine wave at half the Baud rate

#### 54.7.3.8 Transmit jitter

The driver shall satisfy the jitter requirements with a maximum total jitter of  $\pm 0.175$  UI peak from the mean, a maximum deterministic component of  $\pm 0.085$  UI peak from the mean and a random component of  $\pm 0.09$  UI peak from the mean. Note that these values assume symmetrical jitter distributions about the mean. If a distribution is not symmetrical, its peak-to-peak total jitter value must be less than these total jitter values to claim compliance. Jitter specifications include all but  $10^{-12}$  of the jitter population.

**54.7.4 Receiver characteristics**

Receiver characteristics are summarized in Table 54–8 and detailed in the following subclauses.

**Table 54–8—Receiver characteristics’ summary**

Parameter	Subclause reference	Value	Units
Bit error ratio	54.7.4.1	$10^{-12}$	bps
Baud rate tolerance	54.7.4.2	3.125 $\pm 100$	GBd ppm
Unit interval (UI) nominal	54.7.4.2	320	ps
Receiver coupling	54.7.4.3	AC	
Differential input amplitude maximum	54.7.4.4	1600	mV <sub>pp</sub>
Return loss <sup>a</sup> differential common mode	54.7.4.5	10 6	dB dB
Jitter tolerance	54.7.4.6	[See figure (54–7)]	UI

<sup>a</sup>Relative to 100 Ω differential and 25 Ω common mode. See 54.7.4.5 for input impedance details.

**54.7.4.1 Bit error ratio**

The receiver shall operate with a BER of better than  $10^{-12}$  in the presence of a compliant transmit signal, as defined in 54.7.3, and a compliant channel as defined in 54.8.

**54.7.4.2 Baud rate tolerance**

A 10GBASE-CX4 receiver shall tolerate a baud rate of 3.125GBd  $\pm 100$  ppm.

**54.7.4.3 AC coupling**

The 10GBASE-CX4 receiver shall be AC coupled to the cable assembly to allow for maximum interoperability between various 10 Gbps components. AC coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC coupling in actual implementations.

Note: It is recommended that the maximum value of the coupling capacitors be limited to 470pF. This will limit the inrush currents to the receiver, that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

**54.7.4.4 Input signal amplitude**

10GBASE-CX4 receivers shall accept differential input signal amplitudes produced by compliant transmitters connected without attenuation to the receiver. Note that this may be larger than the 1600 mV<sub>pp</sub> differential maximum of 54.7.3.3 due to actual driver and receiver input impedances. The minimum input amplitude is defined by the transmit driver, the channel and the actual receiver input impedance. Note that the transmit

1 driver is defined using a well controlled load impedance. The minimum signal amplitude into an actual  
 2 receiver may vary from the minimum height due to the actual receiver input impedance. Since the  
 3 10GBASE-CX4 receiver is AC coupled, the absolute voltage levels with respect to the receiver ground are  
 4 dependent on the receiver implementation.

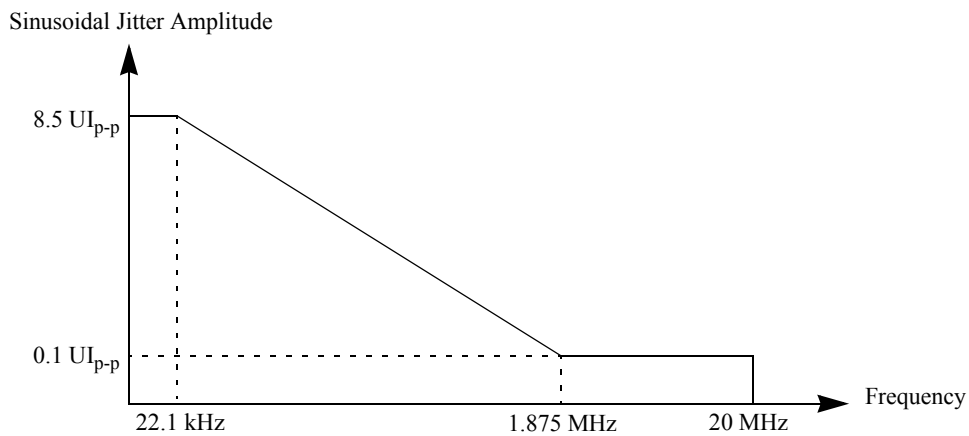
5  
 6 **54.7.4.5 Input impedance**

7  
 8 Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode  
 9 return loss better than 6 dB from 100 MHz to 2.0 GHz. This includes contributions from on-chip circuitry, the  
 10 chip package and any off-chip components related to the receiver. AC coupling components are included in  
 11 this requirement. The reference impedance for return loss measurements is 100 Ω for differential return loss  
 12 and 25 Ω for common mode return loss.

13  
 14 **54.7.4.6 Jitter tolerance**

15  
 16 The total jitter is composed of three components: deterministic jitter, random jitter, and an additional sinuso-  
 17 idal jitter. Deterministic jitter tolerance shall be at least 0.17 UI<sub>p-p</sub> not including any jitter due to ISI. Ran-  
 18 dom jitter tolerance shall be at least 0.18 UI<sub>p-p</sub>. Tolerance to the sum of deterministic and random jitter shall  
 19 be at least 0.35 UI<sub>p-p</sub>. The 10GBASE-CX4 receivers shall tolerate an additional sinusoidal jitter with any  
 20 frequency and amplitude defined by the mask of Figure 54-7. This additional component is intended to  
 21 ensure margin for low-frequency jitter, wander, noise, crosstalk and other variable system effects. Jitter  
 22 specifications include all but 10<sup>-12</sup> of the jitter population. Jitter tolerance test requirements are specified in  
 23 54.10.1.

24  
 25 **Figure 54-7—Single-tone sinusoidal jitter mask**



**54.8 Cable assembly characteristics**

The 10GBASE-CX4 is primarily intended as a point-to-point interface of up to approximately 15 m between integrated circuits using controlled impedance cables. Loss and jitter budgets are presented in Table 54–9.

**Table 54–9—Informative 10GBASE-CX4 loss and jitter budget**

	Loss (dB)	Total jitter (UI <sub>p-p</sub> ) <sup>a</sup>	Random jitter (UI <sub>p-p</sub> ) <sup>a</sup>	Deterministic jitter (UI <sub>p-p</sub> ) <sup>ab</sup>
Driver & package	0	0.35	0.18	0.17
PCB & connector	TBD	TBD		TBD
Cable Assembly	TBD (19.4?)	TBD		TBD
Other <sup>c</sup>	TBD	TBD		TBD
Total	TBD	TBD	0.18	TBD

<sup>a</sup>Jitter specifications include all but 10<sup>-12</sup> of the jitter population.

<sup>b</sup>All bounded jitter not including jitter from ISI.

<sup>c</sup>Includes such effects as crosstalk, noise, and interaction between jitter and eye height.

**Table 54–10—Cable assembly differential characteristics' summary**

Description	Reference	Value	Unit
Characteristic Impedance @ TP2/TP3 <sup>a</sup>	54.8.1	100 ± 10	Ω
Insertion loss at 1.5625 GHz (max.)	54.8.2 & 54.8.3	TBD (16.4?)	dB
Return loss at 1.5625 GHz (max.)	54.8.4	TBD	dB
Minimum NEXT loss	54.8.5.2	TBD (28?)	dB
Minimum MDNEXT loss	54.8.5.2	TBD	dB
Minimum FEXT loss	54.8.6	TBD (26?)	dB
Minimum MDFEXT loss	54.8.6	TBD	dB

<sup>a</sup>The link impedance measurement identifies the impedance mismatches present in the cable assembly when terminated in its characteristic impedance. This measurement includes mated connectors at both ends of the Jumper cable assembly (points TP2 and TP3). The impedance for the jumper cable assembly, shall be recorded 4.0 ns following the reference location determined by an open connector at TP2 and TP3.

**54.8.1 Characteristic impedance**

The recommended differential characteristic impedance of circuit board trace pairs and the cable assembly is 100 Ω ± 10% from 100 MHz to 2.0 GHz.

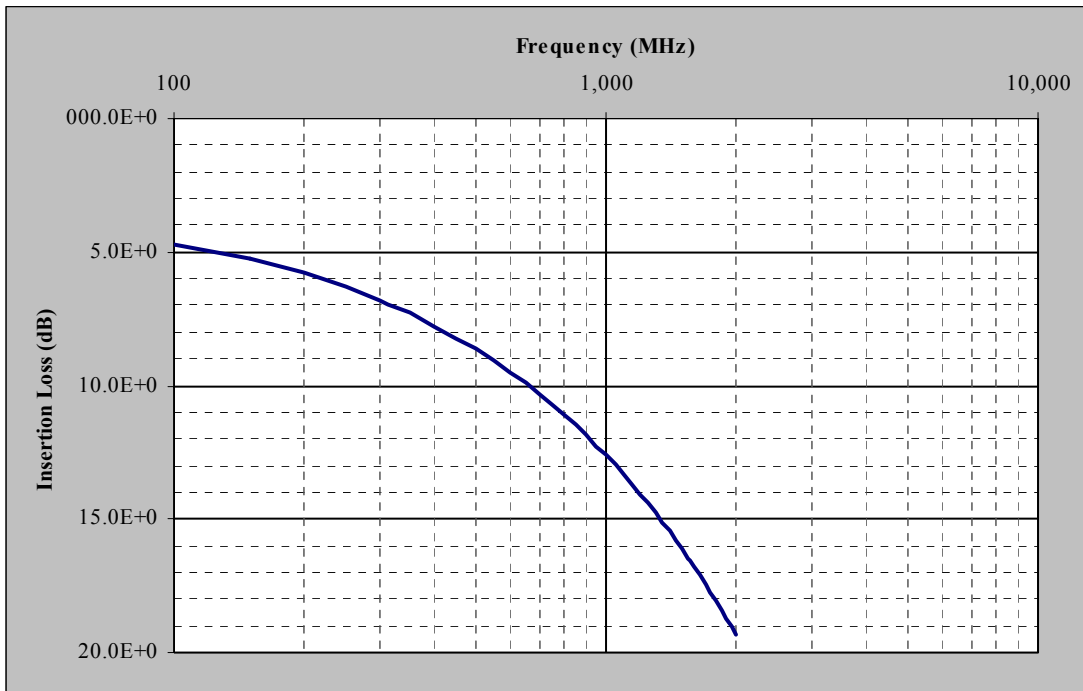
**54.8.2 Cable assembly insertion loss**

The insertion loss, in dB with f in MHz, of each pair of the 10GBASE-CX4 cable assembly shall be:

$$InsertionLoss(f) \leq (0.2629 \cdot \sqrt{f}) + (3.408 \times 10^{-3} \cdot f) + \left(\frac{12.76}{\sqrt{f}}\right) + 0.5 \quad \text{Eq. (54.2)}$$

for all frequencies from 100 MHz to 2.0 GHz. This includes the attenuation of the differential cabling pairs, and the assembly connector.

**Figure 54–8—Cable assembly insertion loss**



**54.8.3 Cable assembly insertion loss deviation**

The insertion loss, in dB, of each pair of the 10GBASE-CX4 cable assembly shall not deviate more than TBD from a best fit to an equation of the form:

$$InsertionLoss(f) = (a \cdot \sqrt{f}) + (b \cdot f) + \left(\frac{c}{\sqrt{f}}\right) + d \quad \text{Eq. (54.3)}$$

for all frequencies from 100 MHz to 2.0 GHz. This includes the attenuation of the differential cabling pairs, and the assembly connector.

**54.8.4 Cable assembly return loss**

The return loss, in dB with f in MHz, of each pair of the 10GBASE-CX4 cable assembly shall be:



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$$ReturnLoss(f) \leq 20 - 17.7 \times \log\left(\frac{f}{100}\right) \tag{Eq. (54.4a)}$$

for 100 MHz ≤ f < 500MHz.

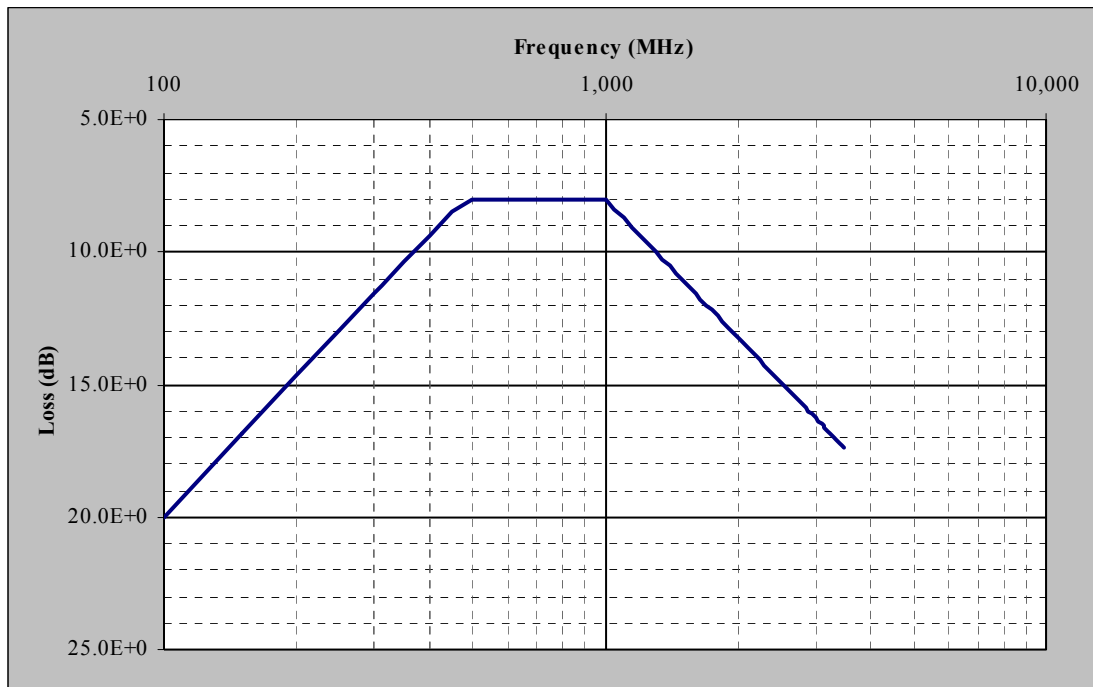
$$ReturnLoss(f) \leq 8 \tag{Eq. (54.4b)}$$

for 500 MHz ≤ f < 1000MHz.

$$ReturnLoss(f) \leq 8 + 17.3 \times \log\left(\frac{f}{1000}\right) \tag{Eq. (54.4c)}$$

for 1000 MHz ≤ f < 2000MHz. This includes the attenuation of the differential cabling pairs, and the assembly connector.

**Figure 54–9—Cable assembly return loss**



**54.8.5 Near-End Crosstalk (NEXT)**

**54.8.5.1 Differential Near-End Crosstalk**

In order to limit the crosstalk at the near end of a link segment, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between the any of the four transmit channels and any of the four receive channels is

1 specified to meet the bit error rate objective specified in 54.7.4.1. The NEXT loss between any transmit and  
 2 receive channel of a link segment, in dB with  $f$  in MHz, shall be at least

$$3 \quad 4 \quad 5 \quad 6 \quad 7 \quad 8 \quad 9 \quad 10 \quad 11 \quad 12 \quad 13 \quad 14 \quad 15 \quad 16 \quad 17 \quad 18 \quad 19 \quad 20 \quad 21 \quad 22 \quad 23 \quad 24 \quad 25 \quad 26 \quad 27 \quad 28 \quad 29 \quad 30 \quad 31 \quad 32 \quad 33 \quad 34 \quad 35 \quad 36 \quad 37 \quad 38 \quad 39 \quad 40 \quad 41 \quad 42 \quad 43 \quad 44 \quad 45 \quad 46 \quad 47 \quad 48 \quad 49 \quad 50 \quad 51 \quad 52 \quad 53 \quad 54$$

$$NEXT(f) \leq 30 - 17 \times \log\left(\frac{f}{2000}\right) \quad \text{Eq. (54.5)}$$

for all frequencies from 100 MHz to 2.0 GHz. This includes the attenuation of the differential cabling pairs, and the assembly connector.

**54.8.5.2 Multiple Disturber Near-End Crosstalk (MDNEXT)**

Since four transmit and four receive channels are used to transfer data between PMDs, the NEXT that is coupled into a receive channel will be from the four transmit channels. To ensure the total NEXT coupled into a receive channel is limited, multiple disturber NEXT loss is specified as the power sum of the individual NEXT losses.

The Power Sum loss between a receive channel and the four transmit channels, in dB with  $f$  in MHz, shall be at least

$$MDNEXT(f) \leq 25 - 17 \times \log\left(\frac{f}{2000}\right) \quad \text{Eq. (54.6)}$$

for all frequencies from 100 MHz to 2.0 GHz. This includes the attenuation of the differential cabling pairs, and the assembly connector.

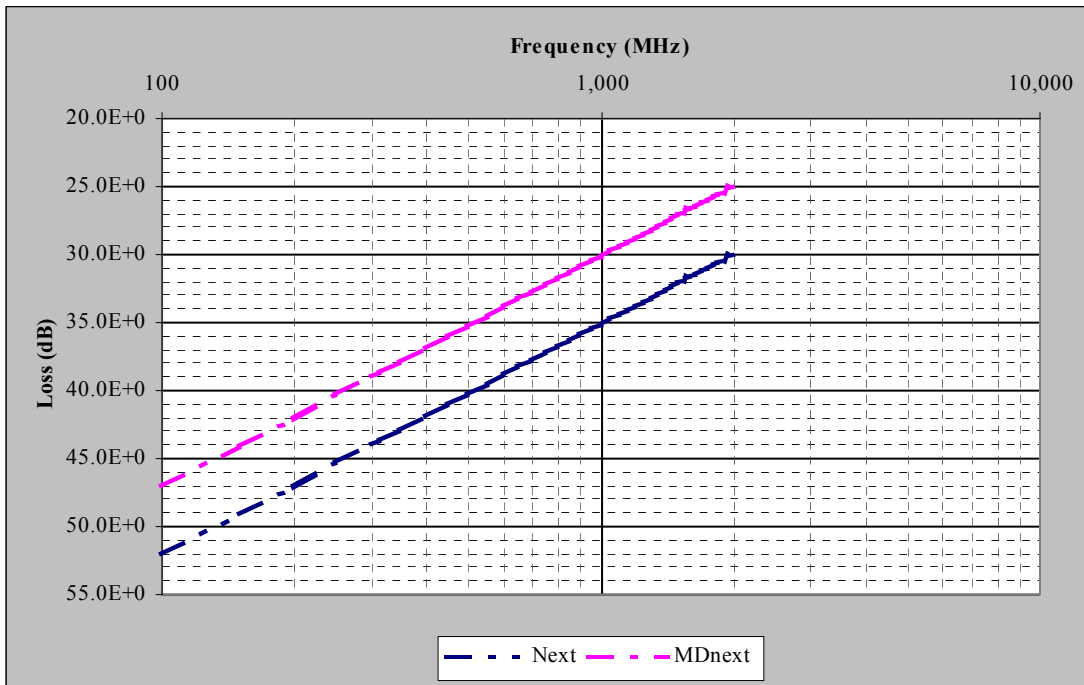
MDNEXT loss is determined by summing the magnitude of the four individual pair-to-pair differential NEXT loss values over the frequency range 100MHz to 2GHz as follows:

$$MDNEXT\_Loss(f) = -10 \log_{10} \sum_{i=1}^{i=3} 10^{-(NL(f)i)/10} \quad \text{Eq. (54.7)}$$

where

- NL( $f$ ) <sub>$i$</sub>  is the magnitude of NEXT loss at frequency  $f$  of pair combination  $i$
- $i$  is the 1, 2, or 3 (pair-to-pair combination)

Figure 54–10—Cable assembly NEXT / MDNEXT loss



54.8.5.3 Far-End Crosstalk (FEXT)

54.8.5.3.1 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk at the far end of each link segment duplex channel and meet the BER objective specified in 54.7.4.1. Far-End Crosstalk (FEXT) is crosstalk that appears at the far end of a duplex channel (disturbed channel), which is coupled from another duplex channel (disturbing channel) with the noise source (transmitters) at the near end. FEXT loss is defined as

$$FEXT\_Loss(f) = 20\log_{10}[V_{pds}(f)/V_{pcn}(f)]$$

and ELFEXT\_Loss is defined as

$$ELFEXT\_Loss(f) = 20\log_{10}[V_{pds}(f)/V_{pcn}(f)] - SLS\_Loss(f)$$

where

- $V_{pds}$  is the peak voltage of disturbing signal (near-end transmitter)
- $V_{pcn}$  is the peak crosstalk noise at far end of disturbed channel
- $SLS\_Loss$  is the insertion loss of disturbed channel in dB

The worst pair ELFEXT loss between any two duplex channels shall be at least:

$$ELFEXT(f) \leq 20 - 20 \times \log\left(\frac{f}{2000}\right) \tag{Eq. (54.8)}$$

1 for all frequencies from 100 MHz to 2.0 GHz. This includes the attenuation of the differential cabling pairs,  
 2 and the assembly connector.

3  
 4 **54.8.5.3.2 Multiple Disturber Equal Level Far-End Crosstalk (MDEL FEXT) loss**

5  
 6 Since four duplex channels are used to transfer data between PMDs, the FEXT that is coupled into a data  
 7 carrying channel will be from the three adjacent disturbing duplex channels. This specification is consistent  
 8 with three channel-to-channel. To ensure the total FEXT coupled into a duplex channel is limited, multiple  
 9 disturber ELFEXT loss is specified as the power sum of the individual ELFEXT losses.

10  
 11 The Power Sum loss between a duplex channel and the three adjacent disturbers shall be at least:

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 14 
$$MDEL FEXT(f) \leq 18 - 20 \times \log\left(\frac{f}{2000}\right)$$
 Eq. (54.9)  
 15  
 16  
 17

18 for all frequencies from 100 MHz to 2.0 GHz. This includes the attenuation of the differential cabling pairs,  
 19 and the assembly connector.

20  
 21 **54.8.5.3.3 Multiple-Disturber Power Sum Equal Level Far-End Crosstalk (PSELFEXT) loss**

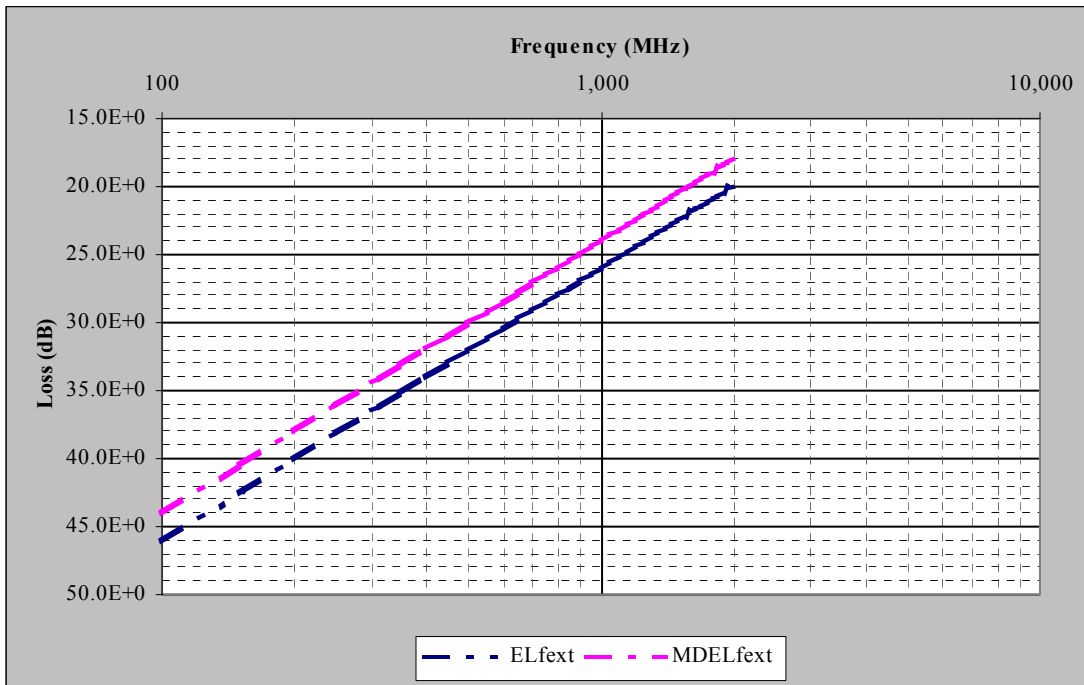
22  
 23 PSELFEXT loss is determined by summing the magnitude of the three individual pair-to-pair differential  
 24 ELFEXT loss values over the frequency range 100MHz to 2000 MHz as follows:

25  
 26  
 27 
$$PSELFEXT(f) = -10 \log_{10} \sum_{i=1}^{i=3} 10^{-(NL(f)i)/10}$$
 Eq. (54.10)  
 28  
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 30

31 where

- 32  
 33  $NL(f)_i$  is the magnitude of FEXT loss at frequency  $f$  of pair combination  $i$   
 34  $i$  is the 1, 2, or 3 (pair-to-pair combination)  
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**Figure 54–11—Cable assembly ELFEXT / MDELTEXT loss**



**54.8.6 Shielding**

The cable assembly shall provide class 2 or better shielding in accordance with IEC 61196-1.

**54.9 MDI specification**

This sub-clause defines the Media Dependent Interface (MDI). The 10GBASE-CX4 PMD of 54.7 is coupled to the cable assembly of 54.8 by the media dependent interface (MDI).

**54.9.1 MDI connectors**

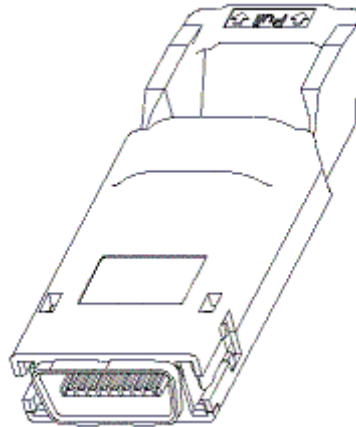
Connectors meeting the requirements of 54.9.1 shall be used as the mechanical interface between the PMD of 54.7 and the jumper cable assembly of 54.8. The plug connector shall be used on the jumper cable assembly and the receptacle on the PHY.

**54.9.1.1 Connector specification**

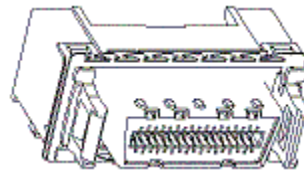
The connector for the cable assemblies shall be the <Editor’s note: short description here> with the mechanical mating interface defined by IEC <Editor’s note: IEC reference number here?>, having pinouts matching those in Table 54–2, and the signal quality and electrical requirements of 54.7 and 54.8.

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**Figure 54–12—Connector Plug**



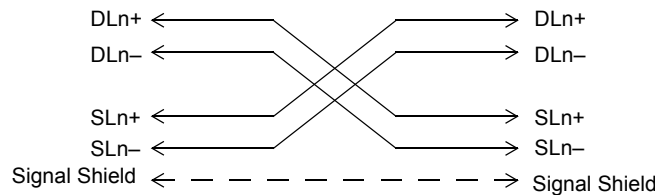
**Figure 54–13—Connector Jack**



**54.9.2 Crossover function**

The default cable assembly shall be wired in a crossover fashion as shown in Figure 54–14, with each of the four pairs being attached to the transmitter contacts at one end and the receiver contacts at the other end.

**Figure 54–14—Cable wiring**



Note: [SL<sub>i</sub><P> and SL<sub>i</sub><N> are the positive and negative sides of the differential signal pair for Lane *i* (*i*=0,1,2,3)]

**54.10 Electrical measurement requirements**

**54.10.1 Jitter test requirements**

For the purpose of jitter measurement, the effect of a single-pole high pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements is the CJPAT pattern defined in Annex 48A. All four lanes of the 10GBASE-CX4 transceiver are active in both directions, and opposite ends of the link use asynchronous clocks. Jitter is measured with AC coupling and at 0 volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER bathtub curve such as that described in Annex 48B.

**54.10.1.1 Transmit jitter**

Transmit jitter is measured at the MDI output when terminated into the load specified in 54.7.3.2.

**54.10.1.2 Jitter tolerance**

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the required sum of deterministic and random jitter defined in 54.7.4.6 and then passing the signal through a cable assemble with an insertion loss that is worst than that as defined in 54.8.3. Random jitter is calibrated using a high pass filter with a low-frequency corner of 20 MHz and 20 dB/decade rolloff. The required sinusoidal jitter specified in 54.7.4.6 is then added to the signal and the far-end load is replaced by the receiver being tested.

**54.11 Environmental specifications**

All equipment subject to this clause shall conform to the requirements of 14.7 and applicable sections of ISO/IEC 11801: 1995.

**54.12 Protocol Implementation Conformance Statement (PICS) proforma for Clause 54., Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4<sup>1</sup>**

**54.12.1 Introduction**

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ak-2003, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

**54.12.2 Identification**

**54.12.2.1 Implementation identification**

Supplier <sup>1</sup>	
Contact point for enquiries about the PICS <sup>1</sup>	
Implementation Name(s) and Version(s) <sup>1,3</sup>	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) <sup>2</sup>	
NOTES	
1—Required for all implementations.	
2—May be completed as appropriate in meeting the requirements for the identification.	
3—The terms Name and Version should be interpreted appropriately to correspond with a supplier’s terminology (e.g., Type, Series, Model).	

<sup>1</sup>Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

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**54.12.2.2 Protocol summary**

Identification of protocol standard	IEEE Std 802.3ak-2003, Clause 54., Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ak-2003.)	

Date of Statement	
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**54.12.3 PICS proforma tables for 10GBASE-CX4 and baseband medium**

**54.12.3.1 Compatibility considerations**

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Jitter test patterns	54.10.1	As per Annex 48A	M	Yes [ ]
CC2	Environmental specifications	54.11		M	Yes [ ]



1 | **54.12.4 Major capabilities / options**

Item	Feature	Subclause	Value/Comment	Status	Support
CX4	10GBASE-CX4 PMD	54.1		O	Yes [ ] No [ ]
MC1	XGMII interface	54.1	Device integrates Clause 46 XGMII interface?	O	Yes [ ] No [ ]
MC2	XGXS & XAUI	54.1	Device integrates Clause 47 XGXS and XAUI interface?	O	Yes [ ] No [ ]
MC3	10GBASE-X PCS/PMA	54.1, 54.2	Device integrates Clause 48 10GBASE-X PCS/PMA?	M	Yes [ ]
MC4	XAUI lane to MDI lane assignment	54.3	Device supports connector pin assignments in Table 54-2	M	Yes [ ]
DC	Delay constraints	54.4	Device conforms to delay constraints	M	Yes [ ]
*MD	MDIO capability	54.5	Registers and interface supported	O	Yes [ ] No [ ]
TP1	Standardized reference point TP1 exposed and available for testing	54.6.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Standardized reference point TP4 exposed and available for testing	54.6.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]

**54.12.4.1 PMD Functional specifications**

Item	Feature	Sub clause	Value/Comment	Status	Support
PF1	Transmit function	54.6.2	Convey bits requested by PMD_UNITDATA.request() to the MDI	M	Yes [ ]
PF2	delivery to the MDI	54.6.2	Supplies electrical signal streams for delivery to the MDI	M	Yes [ ]
PF3	Mapping between electrical signal and logical signal for transmitter	54.6.2	Higher differential voltage is a one	M	Yes [ ]
PF4	Receive function	54.6.3	Convey bits received from the MDI to PMD_UNITDATA.indicate(rx_bit<0:3>)	M	Yes [ ]
PF5	Conversion of four electrical signals to four electrical signals	54.6.3	Converts the four electrical signal streams into four electrical bit streams for delivery to the PMD service	M	Yes [ ]
PF6	Mapping between electrical signal and logical signal for receiver	54.6.3	Higher differential voltage is a one	M	Yes [ ]
PF7	Receive function behavior	54.6.3	Conveys bits from PMD service primitive to the PMD service interface	M	Yes [ ]

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Item	Feature	Sub clause	Value/Comment	Status	Support
PF8	Global Signal Detect function	54.6.4	Report to the PMD service interface the message PMD_SIGNAL.indicate(SIGNAL_DETECT)	M	Yes [ ]
PF11	Global Signal Detect behavior	54.6.4	SIGNAL_DETECT is a global indicator of the presence of electrical signals on all four lanes	M	Yes [ ]
PF12	Global Signal Detect OK threshold	54.6.4	SIGNAL_DETECT = OK for signal value $\geq 175\text{mVppd}$	M	Yes [ ]
PF12	Global Signal Detect OK response	54.6.4	SIGNAL_DETECT = OK indicated within 100 $\mu\text{s}$	M	Yes [ ]
PF13	Global Signal Detect FAIL threshold	54.6.4	SIGNAL_DETECT = FAIL for signal level $< 50\text{mVppd}$ for 250 $\mu\text{s}$ or more	O	Yes [ ] No [ ]
PF14	Global Signal Detect FAIL response	54.6.4	SIGNAL_DETECT = FAIL for signal level $< 50\text{mVppd}$ for 500 $\mu\text{s}$ or more	M	Yes [ ]
PF15	Lane-by-Lane Signal Detect function	54.6.5	Sets PMD_signal_detect_n values on a lane-by-lane basis per requirements of section 54.6.4	MD:O	Yes [ ] No [ ] NA [ ]
PF16	PMD_reset function	54.6.6	Resets the PMD sublayer	MD:O	Yes [ ] No [ ] NA [ ]
PF17	Loop Back	54.6.9	Loopback function provided	M	Yes [ ]
PF18	Loop Back transmit disable	54.6.9	Loopback function disables all transmitters by forcing a constant output state	M	Yes [ ]

54.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Management register set	54.5		MD:M	Yes [ ] N/A [ ]
MF2	Global_PMD_transmit_disable	54.6.7	Disables all transmitters by forcing a constant output state	MD:O	Yes [ ] No [ ] NA [ ]
MF3	PMD_fault disables transmitter	54.6.7	Disables all transmitters by forcing a constant output state when a fault is detected	MD:O	Yes [ ] No [ ] NA [ ]
MF4	PMD_transmit_disable_n	54.6.8	Disables transmitter n (n=0:3) by forcing a constant output state	MD:M	Yes [ ] No [ ]
MF5	PMD_fault disables transmitter n	54.6.8	Disables transmitter n (n=0:3) by forcing a constant output state when a fault is detected	MD:O	Yes [ ] No [ ] NA [ ]
MF6	PMD_fault function	54.6.10	Sets PMD_fault to a logical 1 if any local fault is detected	MD:M	Yes [ ] No [ ]
MF7	PMD_transmit_fault function	54.6.11	Sets PMD_transmit_fault_n to a logical 1 if a local fault is detected on the transmit path x	MD:M	Yes [ ] No [ ]
MF8	PMD_receive_fault function	54.6.12	Sets PMD_receive_fault_x to a logical 1 if a local fault is detected on the receive path x	MD:M	Yes [ ] No [ ]

### 54.12.4.3 Driver specifications

Item	Feature	Subclause	Value/Comment	Status	Support
DS1	Test performed at TP2	54.7.3		M	Yes [ ]
DS2	Test fixture	54.7.3.1	Test fixture of Figure 54-3 or equivalent used	M	Yes [ ]
DS3	Test load	54.7.3.2	100 ohm load used	M	Yes [ ]
DS4	Baud Rate	54.7.3.3	3.125GBd $\pm$ 100ppm	M	Yes [ ]
DS5	Maximum driver output amplitude	54.7.3.4	Less than 1600 mVppd	M	Yes [ ]
DS6	Minimum peak driver output amplitude	54.7.3.4	Greater than TBD 800mVppd	M	Yes [ ]
DS7	Absolute driver output swing	54.7.3.4	Between -0.4 and +2.3 V	M	Yes [ ]
DS8	Driver output impedance	54.7.3.5	$s_{11} = -10$ dB for 312.5 MHz < Freq ( $f$ ) < 625 MHz, and $-10 + 10\log(f/625)$ dB for 625 MHz <= Freq ( $f$ ) < 3.125 GHz	M	Yes [ ]
DS9	Driver output template	54.7.3.6	Measured at TP2	M	Yes [ ]
DS10	Transition time	54.7.3.7	Between 60-130ps	O	Yes [ ]
DS11	Jitter test requirements	54.10.1	Meet BER bathtub curve, See Annex 48B	M	Yes [ ]
DS12	Total jitter	54.7.3.8	less than $\pm 0.175$ UIp	M	Yes [ ]
DS13	Deterministic jitter	54.7.3.8	less than $\pm 0.085$ UIb	M	Yes [ ]
DS14	Random jitter	54.7.3.8	less than $\pm 0.09$ UIp	M	Yes [ ]

**54.12.4.4 Receiver specifications**

Item	Feature	Subclause	Value/Comment	Status	Support
RS1	Bit Error Ratio	54.7.4.1	BER of better than $10^{-12}$	M	Yes [ ]
RS2	Baud rate tolerance	54.7.4.2	3.125GBd $\pm$ 100ppm	M	Yes [ ]
RS3	A.C. Coupling	54.7.4.3		M	Yes [ ]
RS4	Input amplitude tolerance	54.7.4.4	Accepts signals compliant with 54.7.3, may be larger than 1600 mV <sub>ppd</sub>	M	Yes [ ]
RS5	Return Loss	54.7.4.5	At least 10 dB differential and 6 dB common mode return loss	M	Yes [ ]
RS6	Deterministic jitter tolerance	54.7.4.6	At least 0.17 UIpp	M	Yes [ ]
RS7	Random jitter tolerance	54.7.4.6	At least 0.18 UIpp	M	Yes [ ]
RS8	Tolerance to sum of deterministic and random jitter	54.7.4.6	At least 0.35 UIpp	M	Yes [ ]
RS9	Additional sinusoidal jitter tolerance	54.7.4.6	Per Figure 54-7	M	Yes [ ]
RS10	Jitter test requirements	54.10.1	Meet BER bathtub curve, See Annex 48B	M	Yes [ ]

**54.12.4.5 Cable assembly specifications**

Item	Feature	Subclause	Value/Comment	Status	Support
CA1			100 $\Omega$ $\pm$ 10%	M	Yes [ ]
CA2				M	Yes [ ]
CA3				M	Yes [ ]
CA4				M	Yes [ ]
CA5				M	Yes [ ]
CA6				M	Yes [ ]
CA7				M	Yes [ ]
CA8				M	Yes [ ]
CA9				M	Yes [ ]
CA10				M	Yes [ ]
CA11				M	Yes [ ]
CA12				M	Yes [ ]
CA13				M	Yes [ ]
CA				M	Yes [ ]



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