Proposal
for
an initial draft
of a
10GBASE-CX4 PMD
Version 3.2

by: Howard Baumer, Broadcom
David Law, 3Com
Naresh Raman, LSI Logic
Peter Bradshaw, BitBlitz
Schelto VanDoorn, Intel
Jeff Cain, Cisco

30.5.1.1.2 aMAUType

Change this subclause as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A GET-SET ENUMERATION that meets the requirements of the description below:

global	undefined
other	See
unknown	Initializing, true state or type not yet known
AUI	no internal MAU, view from AUI
10BASE5	Thick coax MAU as specified in Clause 8
FOIRL	FOIRL MAU as specified in 9.9
10BASE2	Thin coax MAU as specified in Clause 10
10BROAD36	Broadband DTE MAU as specified in Clause 11
10BASE-T	UTP MAU as specified in Clause 14, duplex mode unknown
10BASE-THD	UTP MAU as specified in Clause 14, half duplex mode
10BASE-TFD	UTP MAU as specified in Clause 14, full duplex mode
10BASE-FP	Passive fiber MAU as specified in Clause 16
10BASE-FB	Synchronous fiber MAU as specified in Clause 17
10BASE-FL	Asynchronous fiber MAU as specified in Clause 18, duplex mode unknown
10BASE-FLHD	Asynchronous fiber MAU as specified in Clause 18, half duplex mode
10BASE-FLFD	Asynchronous fiber MAU as specified in Clause 18, full duplex mode
100BASE-T4	Four-pair Category 3 UTP as specified in Clause 23
100BASE-TX	Two-pair Category 5 UTP as specified in Clause 25, duplex mode unknown
100BASE-TXHD	Two-pair Category 5 UTP as specified in Clause 25, half duplex mode
100BASE-TXFD	Two-pair Category 5 UTP as specified in Clause 25, full duplex mode
100BASE-FX	X fiber over PMD as specified in Clause 26, duplex mode unknown
100BASE-FXHD	X fiber over PMD as specified in Clause 26, half duplex mode
100BASE-FXFD	X fiber over PMD as specified in Clause 26, full duplex mode
100BASE-T2	Two-pair Category 3 UTP as specified in Clause 32, duplex mode unknown
100BASE-T2HD	Two-pair Category 3 UTP as specified in Clause 32, half duplex mode
100BASE-T2FD	Two-pair Category 3 UTP as specified in Clause 32, full duplex mode
1000BASE-X	X PCS/PMA as specified in Clause 36 over undefined PMD, duplex mode unknown
1000BASE-XHD	X PCS/PMA as specified in Clause 36 over undefined PMD, half duplex mode
1000BASE-XFD	X PCS/PMA as specified in Clause 36 over undefined PMD, full duplex mode
1000BASE-LX	X fiber over long-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-LXHD	X fiber over long-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-LXFD	X fiber over long-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-SX	X fiber over short-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-SXHD	X fiber over short-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-SXFD	X fiber over short-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-CX	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, duplex mode unknown
1000BASE-CXHD	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, half duplex mode

1000BASE-CXFD	X copper over 150-Ohm balanced cable PMD as specified in Clause 39, full duplex mode
1000BASE-T	Four-pair Category 5 UTP PHY to be specified in Clause 40, duplex mode unknown
1000BASE-THD	Four-pair Category 5 UTP PHY to be specified in Clause 40, half duplex mode
1000BASE-TFD	Four-pair Category 5 UTP PHY to be specified in Clause 40, full duplex mode
10GBASE-X	X PCS/PMA as specified in Clause 48 over undefined PMD
10GBASE-LX4	X fibre over 4 lane 1310nm optics as specified in Clause 53
10GBASE-CX4	X copper over 8 pair 100-Ohm balanced cable as specified in Clause 54
10GBASE-R	R PCS/PMA as specified in Clause 49 over undefined PMD
10GBASE-ER	R fibre over 1550nm optics as specified in Clause 52
10GBASE-LR	R fibre over 1310nm optics as specified in Clause 52
10GBASE-SR	R fibre over 850nm optics as specified in Clause 52
10GBASE-W	W PCS/PMA as specified in Clauses 49 and 50 over undefined PMD
10GBASE-EW	W fibre over 1550nm optics as specified in Clause 52
10GBASE-LW	W fibre over 1310nm optics as specified in Clause 52
10GBASE-SW	W fibre over 850nm optics as specified in Clause 52
802.9a	Integrated services MAU as specified in IEEE Std 802.9 ISLAN-16T

30B.2 ASN.1 module for CSMA/CD managed objects

Change this subclause as follows:

```
TypeValue::= ENUMERATED {
    global              (0),    --undefined
    other               (1),    --undefined
    unknown             (2),    --initializing, true state not yet known
    AUI                 (7),    --no internal MAU, view from AUI
    10BASE5             (8),    --Thick coax MAU as specified in Clause 8
    FOIRL               (9),    --FOIRL MAU as specified in 9.9
    10BASE2             (10),   --Thin coax MAU as specified in Clause 10
    10BROAD36           (11),   --Broadband DTE MAU as specified in Clause 11
    10BASE-T            (14),   --UTP MAU as specified in Clause 14, duplex mode
                                  unknown
    10BASE-THD          (141),  --UTP MAU as specified in Clause 14, half duplex mode
    10BASE-TFD          (142),  --UTP MAU as specified in Clause 14, full duplex mode
    10BASE-FP           (16),   --Passive fiber MAU as specified in Clause 16
    10BASE-FB           (17),   --Synchronous fiber MAU as specified in Clause 17
    10BASE-FL           (18),   --Asynchronous fiber MAU as specified in Clause 18, duplex
                                  mode unknown
    10BASE-FLHD         (181),  --Asynchronous fiber MAU as specified in Clause 18, half
                                  duplex mode
    10BASE-FLFD         (182),  --Asynchronous fiber MAU as specified in Clause 18, full
                                  duplex mode
    100BASE-T4          (23),   --Four-pair Category 3 UTP as specified in Clause 23
    100BASE-TX          (25),   --Two-pair Category 5 UTP as specified in Clause 25, duplex
                                  mode unknown
    100BASE-TXHD        (251),  --Two-pair Category 5 UTP as specified in Clause 25, half
                                  duplex mode
    100BASE-TXFD        (252),  --Two-pair Category 5 UTP as specified in Clause 25, full
                                  duplex mode
    100BASE-FX          (26),   --X fiber over PMD as specified in Clause 26, duplex mode
                                  unknown
```

100BASE-FXHD	(261),	--X fiber over PMD as specified in Clause 26, half duplex mode
100BASE-FXFD	(262),	--X fiber over PMD as specified in Clause 26, full duplex mode
100BASE-T2	(32),	--Two-pair Category 3 UTP as specified in Clause 32, duplex mode unknown
100BASE-T2HD	(321),	--Two-pair Category 3 UTP as specified in Clause 32, half duplex mode
100BASE-T2FD	(322),	--Two-pair Category 3 UTP as specified in Clause 32, full duplex mode
1000BASE-X	(36),	--X PCS/PMA as specified in Clause 36 over unknown PMD, duplex mode unknown
1000BASE-XHD	(361),	--X PCS/PMA as specified in Clause 36 over unknown PMD, half duplex mode
1000BASE-XFD	(362),	--X PCS/PMA as specified in Clause 36 over unknown PMD, full duplex mode
1000BASE-LX	(381),	--X fiber over long-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-LXHD	(382),	--X fiber over long-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-LXFD	(383),	--X fiber over long-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-SX	(384),	--X fiber over short-wavelength laser PMD as specified in Clause 38, duplex mode unknown
1000BASE-SXHD	(385),	--X fiber over short-wavelength laser PMD as specified in Clause 38, half duplex mode
1000BASE-SXFD	(386),	--X fiber over short-wavelength laser PMD as specified in Clause 38, full duplex mode
1000BASE-CX	(39),	--X copper over 150-Ohm balanced cable PMD as specified in Clause 39, duplex mode unknown
1000BASE-CXHD	(391),	--X copper over 150-Ohm balanced cable PMD as specified in Clause 39, half duplex mode
1000BASE-CXFD	(392),	--X copper over 150-Ohm balanced cable PMD as specified in Clause 39, full duplex mode
1000BASE-T	(40),	--Four-pair Category 5 UTP PHY as specified in Clause 40, duplex mode unknown
1000BASE-THD	(401),	--Four-pair Category 5 UTP PHY as specified in Clause 40, half duplex mode
1000BASE-TFD	(402),	--Four-pair Category 5 UTP PHY as specified in Clause 40, full duplex mode
10GBASE-X	(48)	--X PCS/PMA as specified in Clause 48 over undefined PMD
10GBASE-LX4	(481)	--X fibre over WWDM optics as specified in Clause 53
10GBASE-CX4	(482)	--X copper over 8 pair 100-Ohm balanced cable as specified in Clause 54
10GBASE-R	(49)	--R PCS/PMA as specified in Clause 49 over undefined PMD
10GBASE-ER	(491)	--R fibre over 1550nm optics as specified in Clause 52
10GBASE-LR	(492)	--R fibre over 1310nm optics as specified in Clause 52
10GBASE-SR	(493)	--R fibre over 850nm optics as specified in Clause 52
10GBASE-W	(50)	--W PCS/PMA as specified in Clauses 49 and 50 over undefined PMD
10GBASE-EW	(501)	--W fibre over 1550nm optics as specified in Clause 52
10GBASE-LW	(502)	--W fibre over 1310nm optics as specified in Clause 52
10GBASE-SW	(503)	--W fibre over 850nm optics as specified in Clause 52
802.9a	(99)	--Integrated services MAU as specified in IEEE Std 802.9 ISLAN-16T

}

44. Introduction to 10 Gb/s baseband network

44.1.1 Scope

Change pharagraph 1 & 2 in 44.1.1 to read as follows:

10 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer, connected through a 10 Gigabit Media Independent Interface (XGMII) to Physical Layer entities such as 10GBASE-SR, 10GBASE-LX4, 10GBASE-CX4, 10GBASE-LR, 10GBASE-ER, 10GBASE-SW, 10GBASE-LW, and 10GBASE-EW.

10 Gigabit Ethernet extends the IEEE 802.3 MAC beyond 1000 Mb/s to 10 Gb/s. The bit rate is faster and the bit times are shorter—both in proportion to the change in bandwidth. The minimum packet transmission time has been reduced by a factor of ten. A rate control mode (see ~~4.2.3.2.2~~4.2.3.2.2) is added to the MAC to adapt the average MAC data rate to the SONET/SDH data rate for WAN-compatible applications of this standard. Achievable topologies for 10 Gb/s operation are comparable to those found in 1000BASE-X full duplex mode and equivalent to those found in WAN applications.

44.1.2Objectives

Change 44.1.2 to read as follows:

The following are the objectives of 10 Gigabit Ethernet:

a) Support the full duplex Ethernet MAC.
b) Provide 10 Gb/s data rate at the XGMII.
c) Support LAN PMDs operating at 10 Gb/s, and WAN PMDs operating at SONET STS-192c/SDH VC-4-64c rate.
d) Support cable plants using optical fiber compliant with ISO/IEC 11801: 1995.
e) Allow for a nominal network extent of up to 40 km.
f) Support operation over 15m of copper cable as specified in section 54.8.
g) Meet or exceed FCC/CISPR Class A operation.
h) Support a BER objective of 10^{-12}.

44.1.3 Relationship of 10 Gigabit Ethernet to the ISO OSI reference model

Change item d in 44.1.3 to read as follows:

d) The MDI as specified in Clause 53 for 10GBASE-~~LX4~~ LX4, Clause 54 for 10GBASE-CX4 and in Clause 52 for other PMD types.

44.1.4.4 Physical Layer signaling systems

Change 2nd paragraph in 44.1.4.4 to read as follows:

The term 10GBASE-X, specified in ~~Clause 48~~ Clauses 48, 53 and ~~Clause 53~~54, refers to a specific family of physical layer implementations based upon 8B/10B data coding method. The 10GBASE-X family of physical layer implementations is composed of 10GBASE-~~LX4~~LX4 and 10GBASE-CX4.

Change Table 44-1 to read as follows:

Table 44–1—Nomenclature and clause correlation

Nomenclature	Clause								
	48	49	50	51	52			53	54
	8B/10B PCS & PMA	64B/66B PCS	WIS	Serial PMA	850 nm Serial PMD	1310 nm Serial PMD	1550 nm Serial PMD	1310 nm WDM PMD	4-Lane Cu PMD
10GBASE-SR		M[a]		M	M				
10GBASE-SW		M	M	M	M				
10GBASE-LX4	M							M	
10GBASE-CX4	M								M
10GBASE-LR		M		M		M			
10GBASE-LW		M	M	M		M			
10GBASE-ER		M		M			M		
10GBASE-EW		M	M	M			M		

[a]M = Mandatory

Change 4th paragraph in 44.1.4.4 to read as follows:

Specifications of each physical layer device are contained in Clause 52 and Clause ~~53~~53 and Clause 54.

44.3 Delay constraints

Change Table 44-2 to read as follows:

Table 44–2—Round-trip delay constraints (informative)

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Notes
MAC, RS and MAC Control	8192	16	See 46.1.4.
XGXS and XAUI	4096	8	Round-trip of 2 XGXS and trace for both directions. See 47.2.2.
10GBASE-X PCS and PMA	2048	4	See 48.5.
10GBASE-R PCS	3584	7	See 49.2.15.
WIS	14336	28	See 50.3.7.
CX4 PMD	512	1	Includes **1 meter** of 24AWG cable.
LX4 PMD	512	1	Includes 2 meters of fiber. See 53.2.
Serial PMA and PMD	512	1	Includes 2 meters of fiber. See 52.2.

44.4 Protocol Implementation Conformance Statement (PICS) proforma

Change 1st paragraph in 44.4 to read as follows:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE 802.3, Clause 45 through Clause ~~53~~54, demonstrates compliance by completing a Protocol Implementation Conformance Statement (PICS) proforma.

45. Management Data Input/Output (MDIO) Interface

Change 45.2.1.6.1 to read as follows:

45.2.1.6.1 PMA/PMD type selection (1.7.~~2~~3:0)

Change 1st paragraph in 45.2.1.6.1 to read as follows:

The PMA/PMD type of the 10G PMA/PMD shall be selected using bits ~~2~~ 3 through 0. The PMA/PMD type abilities of the 10G PMA/PMD are advertised in bits 7 through 0 of the 10G PMA/PMD status 2 register. A 10G PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised in the status register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

Change table 45-7 to read as follows:

Table 45–7—10G PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.15:~~4~~3	Reserved	Value always 0, writes ignored	R/W
1.7.3:0	PMA/PMD type selection	3 2 1 0 1 1 1 x = Reserved 1 1 0 1 = Reserved 1 1 0 0 = 10GBASE-CX4 PMA/PMD type 1 0 x x = Reserved 0 1 1 1 = 10GBASE-SR PMA/PMD type 0 1 1 0 = 10GBASE-LR PMA/PMD type 0 1 0 1 = 10GBASE-ER PMA/PMD type 0 1 0 0 = 10GBASE-LX4 PMA/PMD type 0 0 1 1 = 10GBASE-SW PMA/PMD type 0 0 1 0 = 10GBASE-LW PMA/PMD type 0 0 0 1 = 10GBASE-EW PMA/PMD type 0 0 0 0 = Reserved	R/W

[a]R/W = Read/Write

45.2.1.7 10G PMA/PMD status 2 register (Register 1.8)

Change Table 45-8 to read as follows:

Table 45–8—10G PMA/PMD status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.8.15:14	Device present	15 14 1 0 = Device responding at this address 1 1 = No device responding at this address 0 1 = No device responding at this address 0 0 = No device responding at this address	RO
1.8.13	Transmit fault ability	1 = PMA/PMD has the ability to detect a fault condition on the transmit path 0 = PMA/PMD does not have the ability to detect a fault condition on the transmit path	RO
1.8.12	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.8.11	Transmit fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	RO/LH
1.8.10	Receive fault	1 = Fault condition on receive path 0 = No fault condition on receive path	RO/LH
1.8.9	~~Reserved~~ 10GBASE-CX4 ability	~~Ignore on read~~ 1 = PMA/PMD is able to perform 10GBASE-CX4 0 = PMA/PMD is not able to perform 10GBASE-CX4	RO
1.8.8	PMD transmit disable ability	1 = PMD has the ability to disable the transmit path 0 = PMD does not have the ability to disable the transmit path	RO
1.8.7	10GBASE-SR ability	1 = PMA/PMD is able to perform 10GBASE-SR 0 = PMA/PMD is not able to perform 10GBASE-SR	RO
1.8.6	10GBASE-LR ability	1 = PMA/PMD is able to perform 10GBASE-LR 0 = PMA/PMD is not able to perform 10GBASE-LR	RO
1.8.5	10GBASE-ER ability	1 = PMA/PMD is able to perform 10GBASE-ER 0 = PMA/PMD is not able to perform 10GBASE-ER	RO
1.8.4	10GBASE-LX4 ability	1 = PMA/PMD is able to perform 10GBASE-LX4 0 = PMA/PMD is not able to perform 10GBASE-LX4	RO
1.8.3	10GBASE-SW ability	1 = PMA/PMD is able to perform 10GBASE-SW 0 = PMA/PMD is not able to perform 10GBASE-SW	RO
1.8.2	10GBASE-LW ability	1 = PMA/PMD is able to perform 10GBASE-LW 0 = PMA/PMD is not able to perform 10GBASE-LW	RO

Table 45–8—10G PMA/PMD status 2 register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.8.1	10GBASE-EW ability	1 = PMA/PMD is able to perform 10GBASE-EW 0 = PMA/PMD is not able to perform 10GBASE-EW	RO
1.8.0	PMA loopback ability	1 = PMA has the ability to perform a loopback function 0 = PMA does not have the ability to perform a loopback function	RO

[a]RO = Read Only, LH = Latching High

Renumber original sections 45.2.1.7.6 thru 45.2.1.7.15 as 45.2.1.7.7 thru 45.2.1.7.16 and add the following as section 45.2.1.7.6:

45.2.1.7.6 10GBASE-CX4 ability (1.8.9)

When read as a one, bit 1.8.4 indicates that the PMA/PMD is able to support a 10GBASE-CX4 PMA/PMD type. When read as a zero, bit 1.8.4 indicates that the PMA/PMD is not able to support a 10GBASE-CX4 PMA/PMD type.

45.2.1.9.5 Global PMD receive signal detect (1.10.0)

Change 3rd paragraph in 45.2.1.9.5 to read as follows:

Multiple wavelength or multiple lane PMD types indicate the global status of the lane-by-lane signal detect indications using this bit. This bit is read as a one when all the lane signal detect indications are one; otherwise, this bit is read as a zero.

45.5.5.3 PMA/PMD management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MM1	Device responds to all register addresses for that device	45.2		PMA:M	Yes [ ] N/A [ ]
MM2	Writes to undefined and read-only registers have no effect	45.2		PMA:M	Yes [ ] N/A [ ]
MM3	Operation is not affected by writes to reserved and unsupported bits.	45.2		PMA:M	Yes [ ] N/A [ ]
MM4	Reserved and unsupported bits return a value of zero	45.2		PMA:M	Yes [ ] N/A [ ]
MM5	Latching low bits remain low until after they have been read via the management interface	45.2		PMA:M	Yes [ ] N/A [ ]
MM6	Latching low bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PMA:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM7	Latching high bits remain high until after they have been read via the management interface	45.2		PMA:M	Yes [ ] N/A [ ]
MM8	Latching high bits assume correct value once read via the management interface	45.2	Correct value is based upon current state	PMA:M	Yes [ ] N/A [ ]
MM9	Action on reset	45.2.1.1.1	Reset the registers of the entire device to default values and set bit 15 of the Control register to one	PMA:M	Yes [ ] N/A [ ]
MM10	Return 1 until reset completed	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM11	Control and management interfaces are restored to operation within 0.5 s of reset	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM12	Responds to reads of bit 15 during reset	45.2.1.1.1		PMA:M	Yes [ ] N/A [ ]
MM13	Device responds to transactions necessary to exit low-power mode while in low-power state	45.2.1.1.2		PMA:M	Yes [ ] N/A [ ]
MM14	Speed selection bits 13 and 6 are written as one	45.2.1.1.3		PMA:M	Yes [ ] N/A [ ]
MM15	Invalid writes to speed selection bits are ignored	45.2.1.1.3		PMA:M	Yes [ ] N/A [ ]
MM16	PMA is set into Loopback mode when bit 0 is set to a one	45.2.1.1.4		PMA*ALB:M	Yes [ ] N/A [ ]
MM17	PMA transmit data is returned on receive path when in loopback	45.2.1.1.4		PMA*ALB:M	Yes [ ] N/A [ ]
MM18	PMA ignores writes to this bit if it does not support loopback.	45.2.1.1.4		PMA*!ALB:M	Yes [ ] N/A [ ]
MM19	PMA returns a value of zero when read if it does not support loopback.	45.2.1.1.4		PMA*!ALB:M	Yes [ ] N/A [ ]
MM20	Writes to status 1 register have no effect	45.2.1.2		PMA:M	Yes [ ] N/A [ ]
MM21	Receive link status implemented with latching low behavior	45.2.1.2.2		PMA:M	Yes [ ] N/A [ ]
MM22	Unique identifier is composed of OUI, model number and revision	45.2.1.3		PMA:M	Yes [ ] N/A [ ]
MM23	10G PMA/PMD type is selected using bits ~~2~~3:0	45.2.1.6.1		PMA:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM24	10G PMA/PMD ignores writes to type selection bits that select types that it has not advertised	45.2.1.6.1		PMA:M	Yes [ ] N/A [ ]
MM25	Writes to the status 2 register have no effect	45.2.1.7		PMA:M	Yes [ ] N/A [ ]
MM26	PMA/PMD returns a value of zero for transmit fault if it is unable to detect a transmit fault	45.2.1.7.4		PMA:M	Yes [ ] N/A [ ]
MM27	Transmit fault is implemented using latching high behavior	45.2.1.7.4		PMA*PLF:M	Yes [ ] N/A [ ]
MM28	PMA/PMD returns a value of zero for receive fault if it is unable to detect a receive fault	45.2.1.7.5		PMA*!PLF:M	Yes [ ] N/A [ ]
MM29	Receive fault is implemented using latching high behavior	45.2.1.7.5		PMA*PLF:M	Yes [ ] N/A [ ]
MM30	Writes to register 9 are ignored by device that does not implement transmit disable	45.2.1.8		PMA*!PTD:M	Yes [ ] N/A [ ]
MM31	Single wavelength device uses lane zero for transmit disable	45.2.1.8		PMA*PTD:M	Yes [ ] N/A [ ]
MM32	Single wavelength device ignores writes to bits 1 – 4 and returns a value of zero for them	45.2.1.8		PMA*PTD:M	Yes [ ] N/A [ ]
MM33	Setting bit 4 to a one disables transmission on lane 3	45.2.1.8.1		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM34	Setting bit 4 to a zero enables transmission on lane 3	45.2.1.8.1		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM35	Setting bit 3 to a one disables transmission on lane 2	45.2.1.8.2		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM36	Setting bit 3 to a zero enables transmission on lane 2	45.2.1.8.2		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM37	Setting bit 2 to a one disables transmission on lane 1	45.2.1.8.3		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM38	Setting bit 2 to a zero enables transmission on lane 1	45.2.1.8.3		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM39	Setting bit 1 to a one disables transmission on lane 0	45.2.1.8.4		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM40	Setting bit 1 to a zero enables transmission on lane 0	45.2.1.8.4		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MM41	Setting bit 0 to a one disables transmission	45.2.1.8.5		PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM42	Setting bit 0 to a zero enables transmission	45.2.1.8.5	Only is all lane transmit disables are zero	PMA*PTD:M	Yes [ ] No [ ] N/A [ ]
MM43	Unique identifier is composed of OUI, model number and revision	45.2.1.10		PMA:M	Yes [ ] N/A [ ]

48. Physical Coding Sublayer (PCS) and Physical Medium Attachment (PMA) sublayer, type 10GBASE-X

48.1 Overview

Change 1st paragraph in 48.1 to read as follows:

This clause specifies the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) sublayer that are common to a family of 10 Gb/s Physical Layer implementations, collectively known as 10GBASE-X. The 10GBASE-LX4 PMD described in Clause 53 ~~is a member~~ and 10GBASE-CX4 described in Clause 54 are members of the 10GBASE-X PHY family. The term 10GBASE-X is used when referring to issues common to any of the variants within this family.

48.1.2 Relationship of 10GBASE-X to other standards

Change Figure 48-1 as follows:

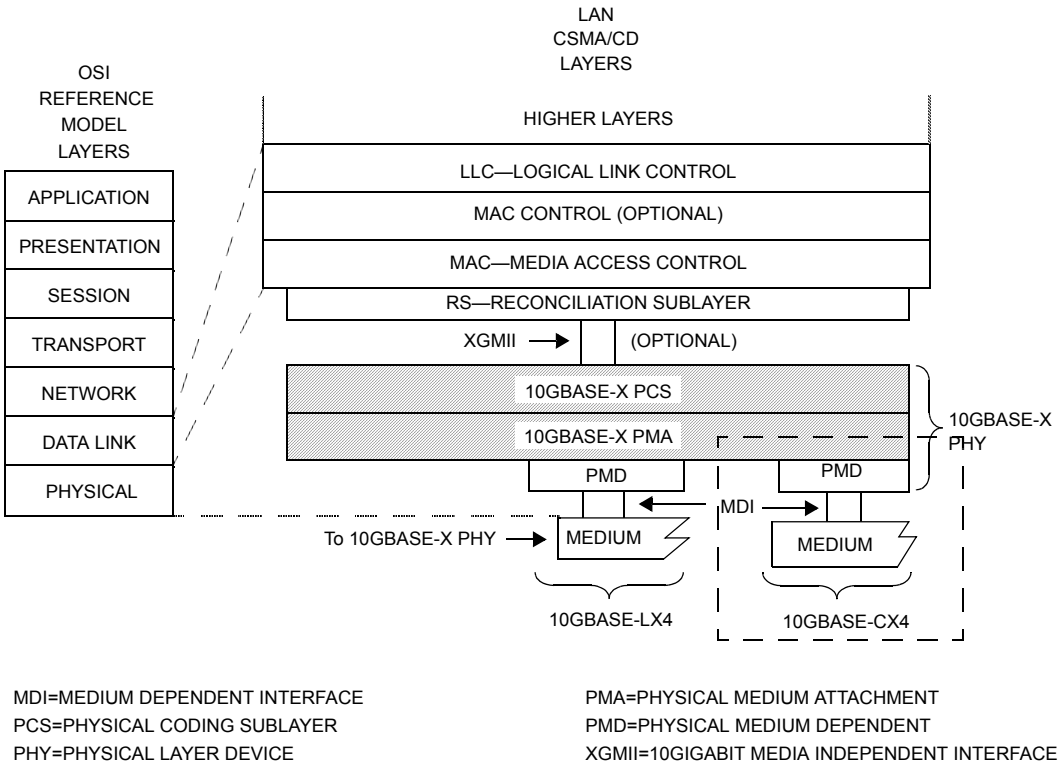


Figure 48–1—10GBASE-X PCS and PMA relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE CSMA/CD LAN Model

48.1.3.3 Physical Medium Dependent (PMD) sublayer

Change 1st paragraph in 48.1.3.3 to read as follows:

10GBASE-X supports the PMD sublayer and MDI specified in Clause 53. The 10GBASE-LX4 ~~PMD performs~~ and 10GBASE-CX4 PMDs perform the following functions:

48.7.3 Major capabilities/options

Change the Table in 48.7.3 to read as follows:

Item	Feature	Subclause	Value/Comment	Status	Support
MD	MDIO	45, 48.1.3.1	Registers and interface supported	O	Yes [ ] No [ ]
XGXS	Support of XAUI/XGXS	47, 48.1.5		O	Yes [ ] No [ ]
XGE	XGMII compatibility interface	46, 48.1.3.1	Compatibility interface is supported	O	Yes [ ] No [ ]
LX4	Support of 10GBASE-LX4 PMD	53, 48.1.3.3		O	Yes [ ] No [ ]
CX4	Support of 10GBASE-CX4 PMD	54, 48.1.3.3		O	Yes [ ] No [ ]

54. Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4

54.1 Overview

This clause specifies the 10GBASE-CX4 PMD (including MDI) and the baseband medium. In order to form a complete Physical Layer, the PMD shall be integrated with the appropriate physical sublayers (see Table 54–1) and with the management functions which are accessible through the Management Interface defined in Clause 45, all of which are hereby incorporated by reference.

Table 54–1—10GBASE-CX4 PMD type and associated physical layer clauses

Associated Clause	10GBASE-CX4
46— XGMII[a]	Optional
47—XGXS and XAUI	Optional
48—10GBASE-X PCS/PMA	Required

[a]The XGMII is an optional interface. However, if the XGMII is not implemented, a conforming implementation must behave functionally as though the RS and XGMII were present.

Figure 54–1 shows the relationship of the PMD and MDI sublayers to the ISO/IEC (IEEE) OSI reference model.

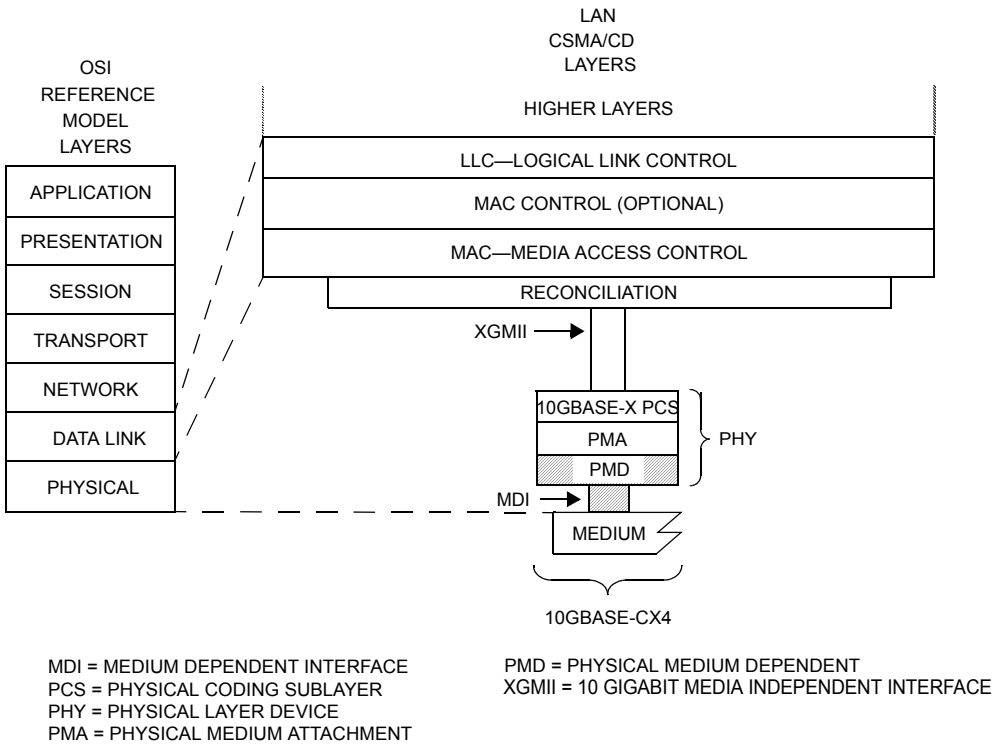


Figure 54–1—10GBASE-CX4 PMD relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model

54.1.1 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the 10GBASE-CX4 PMD. The service interface for this PMD is described in an abstract manner and do not imply any particular implementation. The PMD Service Interface supports the exchange of encoded data between peer PMA entities. The PMD translates the encoded data to and from signals suitable for the specified medium.

The following PMD service primitives are defined:

PMD_UNITDATA.request

PMD_UNITDATA.indicate

PMD_SIGNAL.indicate

54.1.2 PMD_UNITDATA.request

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMA to the PMD.

54.1.2.1 Semantics of the service primitive

PMD_UNITDATA.request (tx_bit <0:3>)

The data conveyed by PMD_UNITDATA.request is a continuous sequence of four parallel code-group streams, one stream for each lane. The tx_bit <0:3> correspond to the bits in the tx_lane<0:3> bit streams. Each bit in the tx_bit parameter can take one of two values: ONE or ZERO.

54.1.2.2 When generated

The PMA continuously sends four parallel code-group streams to the PMD at a nominal signaling speed of 3.125 GBaud.

54.1.2.3 Effect of Receipt

Upon receipt of this primitive, the PMD converts the specified stream of bits into the appropriate signals on the MDI.

54.1.3 PMD_UNITDATA.indicate

This primitive defines the transfer of data (in the form of encoded 8B/10B characters) from the PMD to the PMA.

54.1.3.1 Semantics of the service primitive

PMD_UNITDATA.indicate (rx_bit <0:3>)

The data conveyed by PMD_UNITDATA.indicate is a continuous sequence of four parallel encoded bit streams. The rx_bit<0:3> correspond to the bits in the rx_lane<0:3> bit streams. Each bit in the rx_bit parameter can take one of two values: ONE or ZERO.

54.1.3.2 When generated

The PMD continuously sends stream of bits to the PMA corresponding to the signals received from the MDI.

54.1.3.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

54.1.4 PMD_SIGNAL.indicate

This primitive is generated by the PMD to indicate the status of the signals being received from the MDI.

54.1.4.1 Semantics of the service primitive

PMD_SIGNAL.indicate (SIGNAL_DETECT)

The SIGNAL_DETECT parameter can take on one of two values: OK or FAIL. When SIGNAL_DETECT = FAIL, rx_bit is undefined, but consequent actions based on PMD_UNITDATA.indicate, where necessary, interpret rx_bit as a logic ZERO.

NOTE—SIGNAL_DETECT = OK does not guarantee that rx_bit is known to be good. It is possible for a poor quality link to provide sufficient power for a SIGNAL_DETECT = OK indication and still not meet the 10^{-12} BER objective.

54.1.4.2 When generated

The PMD generates this primitive to indicate a change in the value of SIGNAL_DETECT.

54.1.4.3 Effect of receipt

The effect of receipt of this primitive by the client is unspecified by the PMD sublayer.

54.2 PCS and PMA functionality

The 10GBASE-CX4 PCS and PMA shall conform to the PCS and PMA defined in clause 48 unless otherwise noted herein.

54.3 Input / Output mapping

The 10GBASE-CX4 shall have the XAUI lane, as shown in Figure 47-2, to MDI connector pin mapping depicted in Table 54–2.

Table 54–2—XAUI lane to MDI connector pin mapping

XAUI Rx lane	MDI Connector pin	XAUI Tx lane	MDI Connector pin
DL0<p>	S1	SL0<p>	S16
DL0<n>	S2	SL0<n>	S15
DL1<p>	S3	SL1<p>	S14
DL1<n>	S4	SL1<n>	S13
DL2<p>	S5	SL2<p>	S12
DL2<n>	S6	SL2<n>	S11
DL3<p>	S7	SL3<p>	S10
DL3<n>	S8	SL3<n>	S9

54.4 Delay constraints

Predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers must conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of transmit and receive delay contributed by the 10GBASE-CX4 PMD shall be no more than 512 BT (including 1 meter of cable).

54.5 PMD MDIO function mapping

The optional MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMD. Mapping of MDIO control variables to PMD control variables is shown in Table 54–3. Mapping of MDIO status variables to PMD status variables is shown in Table 54–4.

Table 54–3—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
Global transmit disable	Control register 1	1.9.0	Global_PMD_transmit_disable
Transmit disable 3	Transmit disable register	1.9.4	PMD_transmit_disable_3
Transmit disable 2	Transmit disable register	1.9.3	PMD_transmit_disable_2
Transmit disable 1	Transmit disable register	1.9.2	PMD_transmit_disable_1
Transmit disable 0	Transmit disable register	1.9.1	PMD_transmit_disable_0

Table 54–4—MDIO/PMD status variable mapping

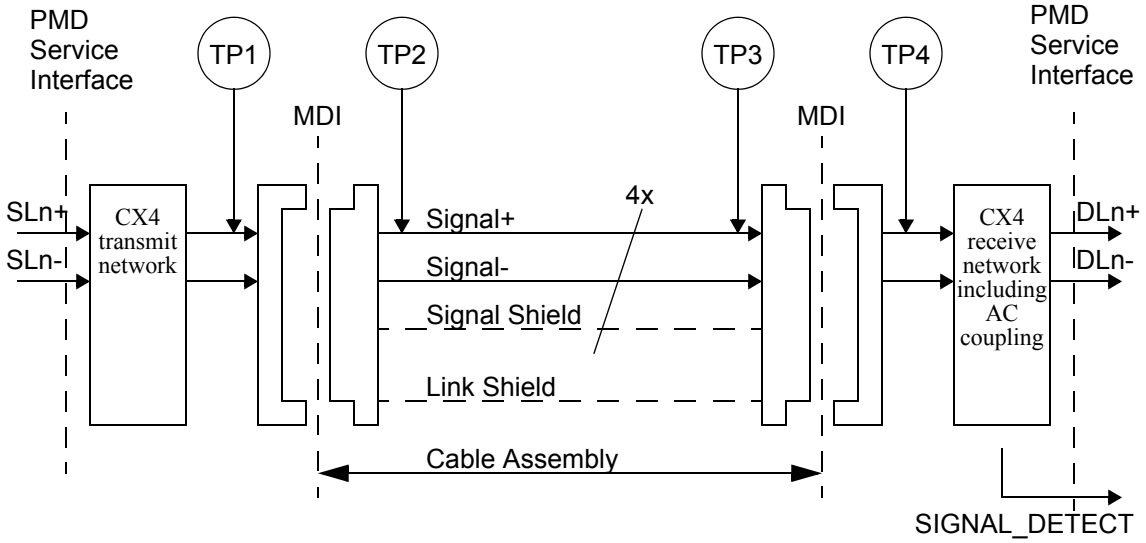
MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Local fault	Status register 1	1.1.7	PMD_fault
Transmit fault	Status register 2	1.8.11	PMD_transmit_fault
Receive fault	Status register 2	1.8.10	PMD_receive_fault
Global PMD signal detect	Receive signal detect register	1.10.0	Global_PMD_signal_detect
PMD signal detect 3	Receive signal detect register	1.10.4	PMD_signal_detect_3
PMD signal detect 2	Receive signal detect register	1.10.3	PMD_signal_detect_2
PMD signal detect 1	Receive signal detect register	1.10.2	PMD_signal_detect_1
PMD signal detect 0	Receive signal detect register	1.10.1	PMD_signal_detect_0

54.6 PMD functional specifications

The 10GBASE-CX4 PMD performs the Transmit and Receive functions which convey data between the PMD service interface and the MDI plus various management functions if the optional MDIO is implemented.

54.6.1 PMD block diagram

The PMD block diagram is shown in Figure 54–2. For purposes of system conformance, the PMD sublayer is standardized at the points described in this subclause. The electrical transmit signal is defined at the output end of the mated connector (TP2). Unless specified otherwise, all transmitter measurements and tests defined in 54.7.3 are made at TP2. The electrical receive signal is defined at the output of the cabling mated connector (TP4). Unless specified otherwise, all receiver measurements and tests defined in 54.7.4 are made at TP3.



Note: SLn+ and SLn- are the positive and negative sides of the transmit differential signal pair and DLn+ and DLn- are the positive and negative sides of the receive differential signal pair for Lane n (n = 0, 1, 2, 3)

Figure 54–2—10GBASE-CX4 link (half link is shown)

54.6.2 PMD transmit function

The PMD Transmit function shall convert the four electronic bit streams requested by the PMD service interface message PMD_UNITDATA.request (tx_bit<0:3>) into four separate electrical signal streams. The four electrical signal streams shall then be delivered to the MDI, all according to the transmit electrical specifications in this clause. A positive output voltage of SLn+ minus SLn– (differential voltage) shall correspond to tx_bit = ONE.

54.6.3 PMD receive function

The PMD Receive function shall convert the four electrical signal streams from the MDI into four electronic bit streams for delivery to the PMD service interface using the message PMD_UNITDATA.indicate

(rx_bit<0:3>), all according to the receive electrical specifications in this clause. A positive input voltage level in each signal stream of DLn+ minus DLn– (differential voltage) shall correspond to a rx_bit = ONE.

The PMD shall convey the bits received from the PMD_UNITDATA.request(tx_bit<0:3>) service primitive to the PMD service interface using the message PMD_UNITDATA.indicate(rx_bit<0:3>), where rx_bit<0:3> = tx_bit<0:3>.

54.6.4 Global PMD signal detect function

The Global_PMD_signal_detect function shall report the state of SIGNAL_DETECT via the PMD service interface. The SIGNAL_DETECT parameter is signaled continuously, while the PMD_SIGNAL.indicate message is generated when a change in the value of SIGNAL_DETECT occurs.

SIGNAL_DETECT shall be a global indicator of the presence of electrical signals on all four lanes. The PMD receiver is not required to verify whether a compliant 10GBASE-CX4 signal is being received, however, it shall be required to assert SIGNAL_DETECT = OK when the differential peak-to-peak voltage on each of the four lanes at the MDI has exceeded 175mVppd for at least 1 UI. The transition from SIGNAL_DETECT = FAIL to SIGNAL_DETECT = OK shall occur within 100µs after the condition for SIGNAL_DETECT = OK has been received.

The PMD receiver shall not assert SIGNAL_DETECT = FAIL until the differential peak-to-peak voltage on any of the four lanes at the MDI has dropped below 50mVppd and has remained below 50mVppd for at least 250µs. The PMD shall assert SIGNAL_DETECT = FAIL when the differential peak-to-peak voltage on any of the four lanes at the MDI has dropped below 50mVppd and has remained below 50mVppd for longer than 500µs.

Table 54–5—SIGNAL_DETECT summary

Parameter	Value	Units
SIGNAL_DETECT = OK level (maximum)	175	mVppd
SIGNAL_DETECT = OK width (minimum)	1	UI
SIGNAL_DETECT = OK assertion time (maximum)	100	µs
SIGNAL_DETECT = FAIL level (mimimum)	50	mVppd
SIGNAL_DETECT = FAIL de-assertion time maximum mimimum	 500 250	 µs µs

Note: The SIGNAL_DETECT=OK assertion time is recommended to be much faster than 100µs, however, this specification assumes measurement through the MII management interface and is thus limited by the sampling time required through that interface.

54.6.5 PMD lane by lane signal detect function

Various implementations of the Signal Detect function are permitted by this standard. When the MDIO is implemented, each PMD_signal_detect_n, where n represents the lane number in the range 0:3, value shall be continuously set in response to the amplitude of the receive signal on its associated lane, according to the requirements of section 54.6.4.

54.6.6 PMD reset function

If the MDIO interface is implemented, and if PMD_reset is asserted, the PMD shall be reset as defined in 45.2.1.1.1.

54.6.7 Global PMD transmit disable function

The Global_PMD_transmit_disable function is optional and allows all of the transmitters to be disabled.

a) When a Global_PMD_transmit_disable variable is set to ONE, this function shall turn off all of the transmitters such that each transmitter drives a constant logic level (i.e. no transitions) and meets the requirements of the absolute output voltage limits in Table 54–6.
b) If a PMD_fault is detected, then the PMD may set the Global_PMD_transmit_disable to ONE, turning off the electrical transmitter in each lane.
c) Loopback as defined in 54.6.9 shall not be affected by Global_PMD_transmit_disable.

54.6.8 PMD lane by lane transmit disable function

The PMD_transmit_disable_n function allows the electrical transmitters in each lane to be selectively disabled.

a) When a PMD_transmit_disable_n variable is set to ONE, this function shall turn off the transmitter associated with that variable such that each transmitter drives a constant logic level (i.e. no transitions) and meets the requirements of the absolute output voltage limits in Table 54–6.
b) If a PMD_fault is detected, then the PMD may set each PMD_transmit_disable_n to ONE, turning off the electrical transmitter in each lane.
c) Loopback as defined in 54.6.9 shall not be affected by PMD_transmit_disable_n.

If the PMD_transmit_disable_n function is not implemented in MDIO, an alternative method shall be provided to independently disable each transmit lane.

54.6.9 Loopback mode

Loopback mode shall be provided for the 10GBASE-CX4 as specified in this subclause, by the transmitter and receiver of a device as a test function to the device. When Loopback mode is selected by setting ~~either~~ the loopback control bit of 1.0.0 ~~or 3.0.14~~, transmission requests passed to the transmitter are shunted directly to the receiver, overriding any signal detected by the receiver on its attached link. A device is explicitly placed in Loopback mode (i.e., Loopback mode is not the normal mode of operation of a device). Loopback applies to all lanes as a group (i.e., the lane 0 transmitter is directly connected to the lane 0 receiver, the lane 1 transmitter is directly connected to the lane 1 receiver, etc.). The method of implementing Loopback mode is not defined by this standard.

Control of the Loopback function may be supported through the MDIO management interface of Clause 45 or equivalent.

NOTE—The signal path that is exercised in the Loopback mode is implementation specific, but it is recommended that this signal path encompass as much of the circuitry as is practical. The intention of providing this Loopback mode of operation is to permit diagnostic or self-test functions to test the transmit and receive data paths using actual data. Other loopback signal paths may also be enabled independently using loopback controls within other devices or sublayers.

54.6.10 PMD fault function

If the MDIO is implemented, and the PMD has detected a local fault on any of the transmit or receive paths, the PMD shall set PMD_fault to ONE.

54.6.11 PMD transmit fault function

If the MDIO is implemented, and the PMD has detected a local fault on any transmit lane, the PMD shall set the PMD_transmit_fault variable to ONE.

54.6.12 PMD receive fault function

If the MDIO is implemented, and the PMD has detected a local fault on any receive lane, the PMD shall set the PMD_receive_fault variable to ONE.

54.7 PMD to MDI Electrical specifications for 10GBASE-CX4

54.7.1 Signal levels

The 10GBASE-CX4 MDI is a low swing AC coupled differential interface. AC coupling allows for interoperability between components operating from different supply voltages. Low swing differential signaling provides noise immunity and improved electromagnetic interference (EMI).

54.7.2 Signal paths

The 10GBASE-CX4 MDI signal paths are point-to-point connections. Each path corresponds to a 10GBASE-CX4 MDI lane and is comprised of two complementary signals making a balanced differential pair. There are four differential paths in each direction for a total of eight pairs, or sixteen connections. The signal paths are intended to operate up to approximately 15m over standard twinaxial cables as described in 54.8.

54.7.3 Transmitter characteristics

Transmitter characteristics shall be measured at TP2, unless otherwise noted, and are summarized in Table 54–6 and detailed in the following subclauses.

Table 54–6—Driver characteristics' summary

Parameter	Subclause reference	Value	Units
Baud rate tolerance	54.7.3.3	3.125 GBd ± 100 ppm	GBd ppm
Unit interval nominal	54.7.3.3	320	ps
Differential peak amplitude maximum minimum	54.7.3.4	 1600 800	 mV_{pp} mV_{pp}
Common mode Signal+/- voltage limits maximum minimum	54.7.3.4	 1.9 –0.4	 V V
Differential output return loss minimum	54.7.3.5	[See Equation (54.1a) and (54.1b)]	dB
Differential output template	54.7.3.6	[See figure (54–6) and table (54–7)]	V
Transition time maximum minimum	54.7.3.7	 130 60	 ps ps
Output jitter Random jitter Deterministic jitter[a] Total jitter	54.7.3.8	 ± 0.090 peak from the mean ± 0.085 peak from the mean ± 0.175 peak from the mean	 UI UI UI

[a]Deterministic jitter is already incorporated into the differential output template.

54.7.3.1 Test Fixtures

The following fixture (illustrated by Figure 54–3), or its functional equivalent, shall be used for measuring the transmitter specifications described in 54.7.3. The transmitter under test includes the driver, pcb traces, any AC coupling components and the MDI connector described in 54.9.1

~~Vabcd~~

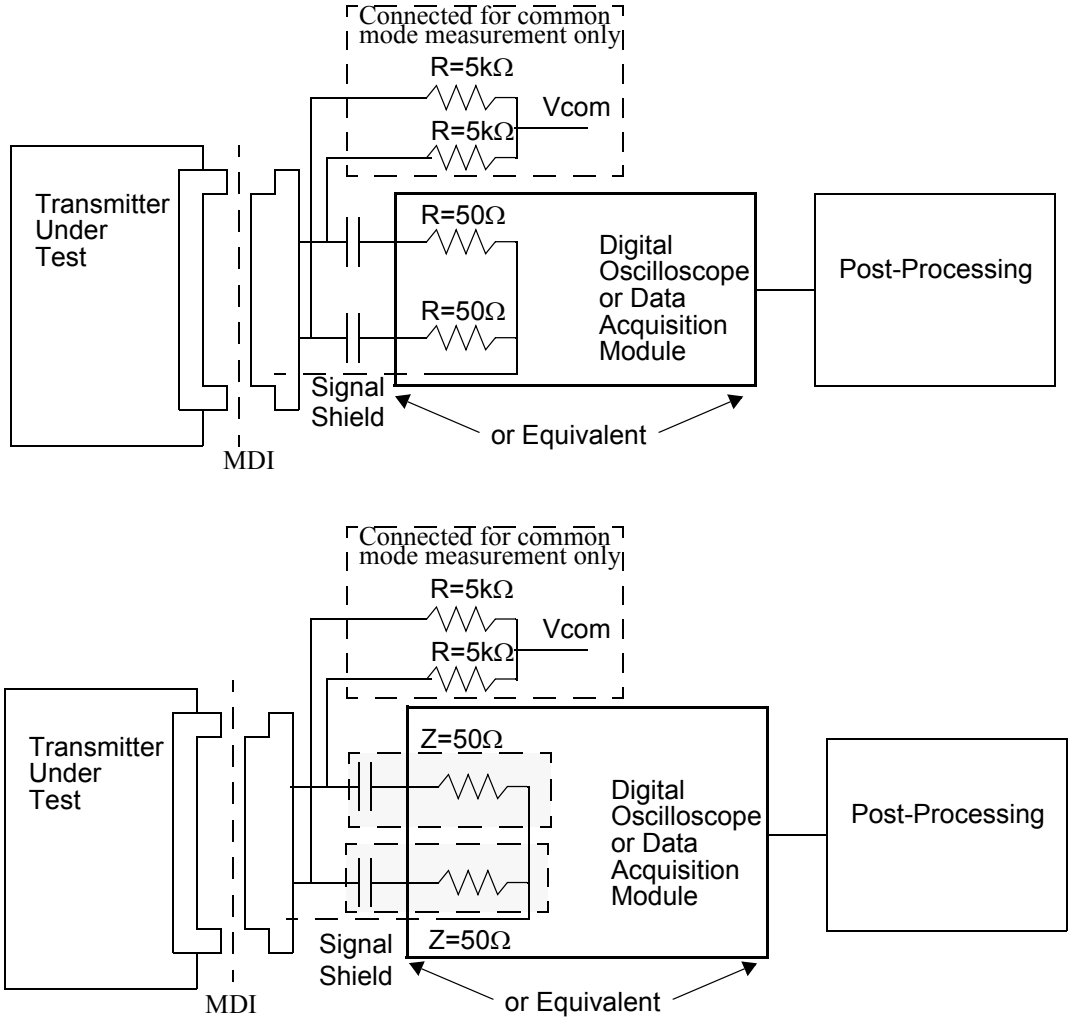


Figure 54–3—Transmit Test Fixture

54.7.3.2 Test Fixture Impedance

The test fixture impedance shall be 2 x 50Ω ± 1% to signal shield from 100 MHz to 2.0 GHz for these measurements, unless otherwise noted.

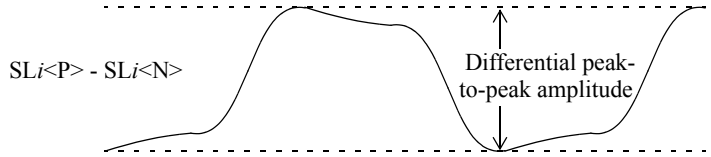
54.7.3.3 Baud rate tolerance

The 10GBASE-CX4 MDI Baud shall be 3.125 GBaud ±100 ppm. The corresponding Baud period is nominally 320 ps.

54.7.3.4 Amplitude and swing

Driver differential output amplitude shall be less than 1600 mV_{p-p}. The minimum differential peak to peak output voltage shall be greater than 800 mV_{p-p}. See Figure 54–4 for an illustration of definition of differential peak-to-peak amplitude.

DC-referenced logic levels are not defined since the receiver is AC coupled. The Signal+ / Signal- D.C. common mode voltage shall be between –0.4 V and 1.9 V with respect to Signal Shield as measured at Vcom in Figure 54–3.



Note: [SL*i*<P> and SL*i*<N> are the positive and negative sides of the differential signal pair for Lane *i* (*i*=0,1,2,3)]

Figure 54–4—Driver output voltage limits and definitions

54.7.3.5 Output impedance

For frequencies from 100 MHz to 2.0 GHz, the differential return loss, in dB with f in MHz, of the driver shall exceed Equation 54.1a and 54.1b. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100Ω.

$$ReturnLoss(f) \geq 10 \qquad \text{Eq. (54.1a)}$$

for 100 MHz <= f < 625 MHz and

$$ReturnLoss(f) \geq 10 - 10 \times \log\left(\frac{f}{625}\right) \qquad \text{Eq. (54.1b)}$$

for 625 MHz <= f < 2.0 GHz.

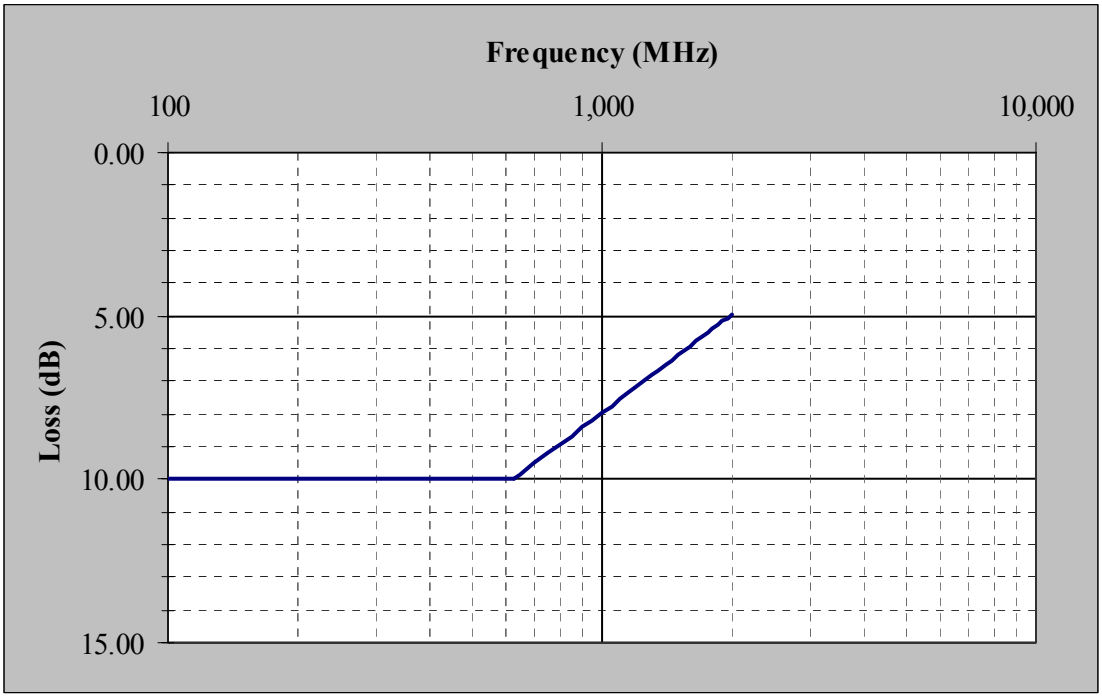


Figure 54–5—Transmit differential output return loss

54.7.3.6 Differential output template

The differential output template shall be tested using the low frequency test pattern specified in Annex 48A.2. The waveform under test shall be normalized by using the following procedure:

1) Align the output waveform under test, to achieve the best fit along the horizontal time axis.

2) Calculate the +1 low frequency level as Vlowp = average of any 2 continuous baud (640ps) between 800ps and 1760ps.

3) Calculate the -1 low frequency level as Vlowm = average of any 2 continuous baud (640ps) between 2400ps and 3360ps.

4) Calculate the vertical offset to be subtracted from the waveform as Voff = (Vlowp + Vlowm) / 2.

5) Calculate the vertical normalization factor for the waveform as Vnorm = (Vlowp - Vlowm) / 2.

6) Calculate the normalized waveform as: NormalizedWaveform = (OriginalWaveform - Voff) * (0.5 / Vnorm).

7) Align the normalized output waveform under test, to achieve the best fit along the horizontal time axis.

The normalized differential voltage waveform shall lie within the time domain template defined in Figure 54–6 and the piece-wise linear interpolation between the points in Table 54–7. These measurements are to be made for each pair while observing the differential signal output at the MDI using the transmitter test fixture.

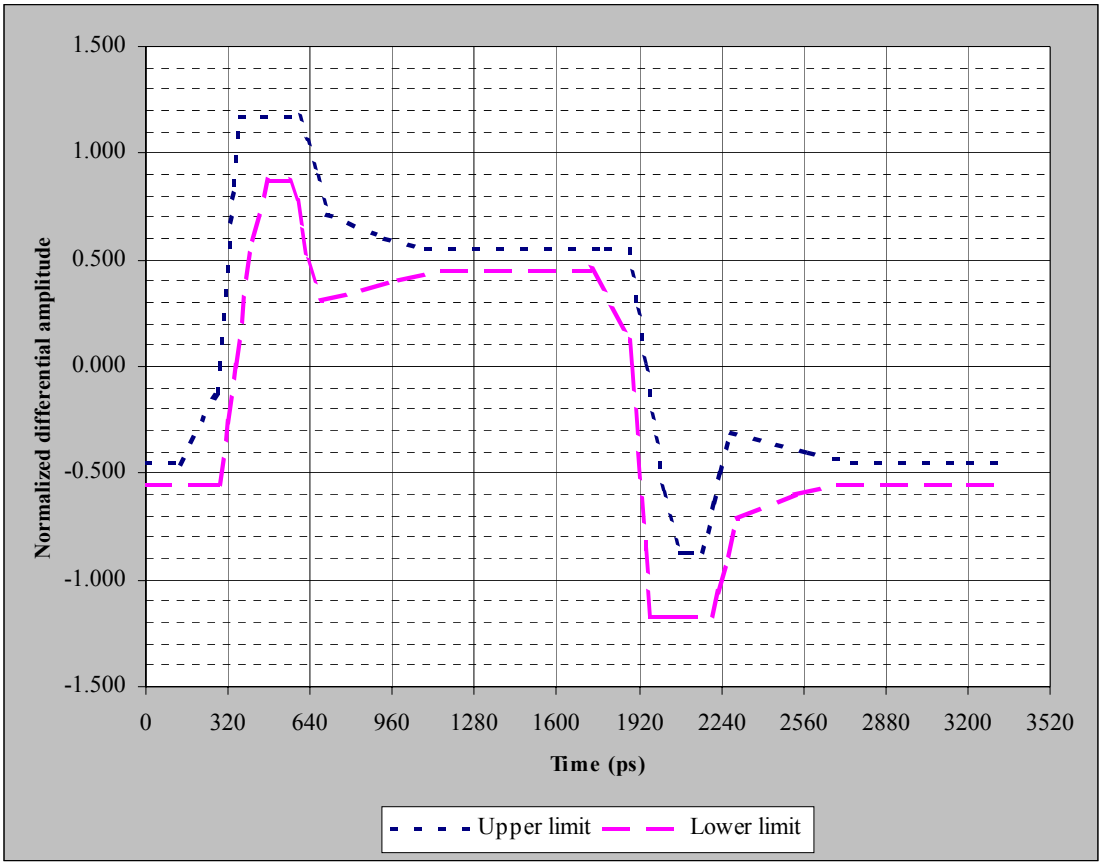


Figure 54–6—Normalized transmit template as measured at MDI using Figure 54–3

Table 54–7—Normalized transmit time domain template

Time (ps)	Upper limit	Time (ps)	Lower limit
0	-0.450	0	-0.550
131	-0.450	189	-0.550
283	-0.125	287	-0.550
283	-0.125	319	-0.266
291	0.000	349	0.000
343	0.850	414	0.586
363	1.175	477	0.870
451	1.175	509	0.870
602	1.175	565	0.870
629	1.060	591	0.776
669	0.888	611	0.635
709	0.715	631	0.494
709	0.715	685	0.306
931	0.600	989	0.400
1091	0.550	1149	0.450
1789	0.550	1731	0.450
1887	0.550	1883	0.125
1919	0.266	1883	0.125
1949	0.000	1891	0.000
2014	-0.586	1943	-0.850
2077	-0.870	1963	-1.175
2109	-0.870	2051	-1.175
2165	-0.870	2202	-1.175
2191	-0.776	2229	-1.060
2211	-0.635	2269	-0.888
2231	-0.494	2309	-0.715
2285	-0.306	2309	-0.715
2589	-0.400	2531	-0.600
2749	-0.450	2691	-0.550
3200	-0.450	3200	-0.550
3360	-0.450	3360	-0.550

NOTE—The ASCII for Table 54–7 is available from http://www.ieee802.org/3/publication/index.html.
Editor's note: NEED correct url

54.7.3.7 Transition time

Differential transition times shall be between 60 and 130 ps as measured between the 20% and 80% levels while transmitting the pattern defined by 48A.1. Faster transitions may result in excessive high-frequency components and increase EMI and crosstalk.

54.7.3.8 Transmit jitter

The transmitter shall satisfy the jitter requirements with a maximum total jitter of ± 0.175 UI peak from the mean, a maximum deterministic component of ± 0.085 UI peak from the mean and a random component of ± 0.09 UI peak from the mean. Note that these values assume symmetrical jitter distributions about the mean. If a distribution is not symmetrical, its peak-to-peak total jitter value must be less than these total jitter values to claim compliance. Jitter specifications include all but 10^{-12} of the jitter population.

Editor's Note: The transmitter jitter allocation is a subject for analysis and will be reconsidered at the March 2003 Plenary.

54.7.4 Receiver characteristics

Receiver characteristics are summarized in Table 54–8 and detailed in the following subclauses.

Table 54–8—Receiver characteristics' summary

Parameter	Subclause reference	Value	Units
Bit error ratio	54.7.4.1	10^{-12}	
Baud rate tolerance	54.7.4.2	3.125 ±100	GBd ppm
Unit interval (UI) nominal	54.7.4.2	320	ps
Receiver coupling	54.7.4.3	AC	
Differential input amplitude (maximum)	54.7.4.4	1600	mVpp
Return loss[a] differential (minimum)	54.7.4.5	10	dB
Jitter tolerance	54.7.4.6	[See figure (54–8)]	UI

[a]Relative to 100 Ω differential.

54.7.4.1 Bit error ratio

The receiver shall operate with a BER of better than 10^{-12} in the presence of a compliant transmit signal, as defined in 54.7.3, and a compliant channel as defined in 54.8.

54.7.4.2 Baud rate tolerance

A 10GBASE-CX4 receiver shall tolerate a baud rate of 3.125GBd ±100 ppm.

54.7.4.3 AC coupling

The 10GBASE-CX4 receiver shall be AC coupled to the cable assembly to allow for maximum interoperability between various 10 Gbps components. AC coupling is considered to be part of the receiver for the purposes of this specification unless explicitly stated otherwise. It should be noted that there may be various methods for AC coupling in actual implementations.

Note: It is recommended that the maximum value of the coupling capacitors be limited to 470pF. This will limit the inrush currents to the receiver, that could damage the receiver circuits when repeatedly connected to transmit modules with a higher voltage level.

54.7.4.4 Input signal amplitude

10GBASE-CX4 receivers shall accept differential input signal amplitudes produced by compliant transmitters connected without attenuation to the receiver. Note that this may be larger than the 1600 mV_{pp} differential maximum of 54.7.3.3 due to actual driver and receiver input impedances. The minimum input amplitude is defined by the transmit driver, the channel and the actual receiver input impedance. Note that the transmit

driver is defined using a well controlled load impedance. The minimum signal amplitude into an actual receiver may vary from the minimum height due to the actual receiver input impedance. Since the 10GBASE-CX4 receiver is AC coupled, the absolute voltage levels with respect to the receiver ground are dependent on the receiver implementation.

54.7.4.5 Input impedance

For frequencies from 100 MHz to 2.0 GHz, the differential return loss, in dB with f in MHz, of the receiver shall exceed Equation 54.2a and 54.2b. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100Ω

$$ReturnLoss(f) \geq 10 \qquad \text{Eq. (54.2a)}$$

for 100 MHz <= f < 625 MHz and

$$ReturnLoss(f) \geq 10 - 10 \times \log\left(\frac{f}{625}\right) \qquad \text{Eq. (54.2b)}$$

for 625 MHz <= f < 2.0 GHz.

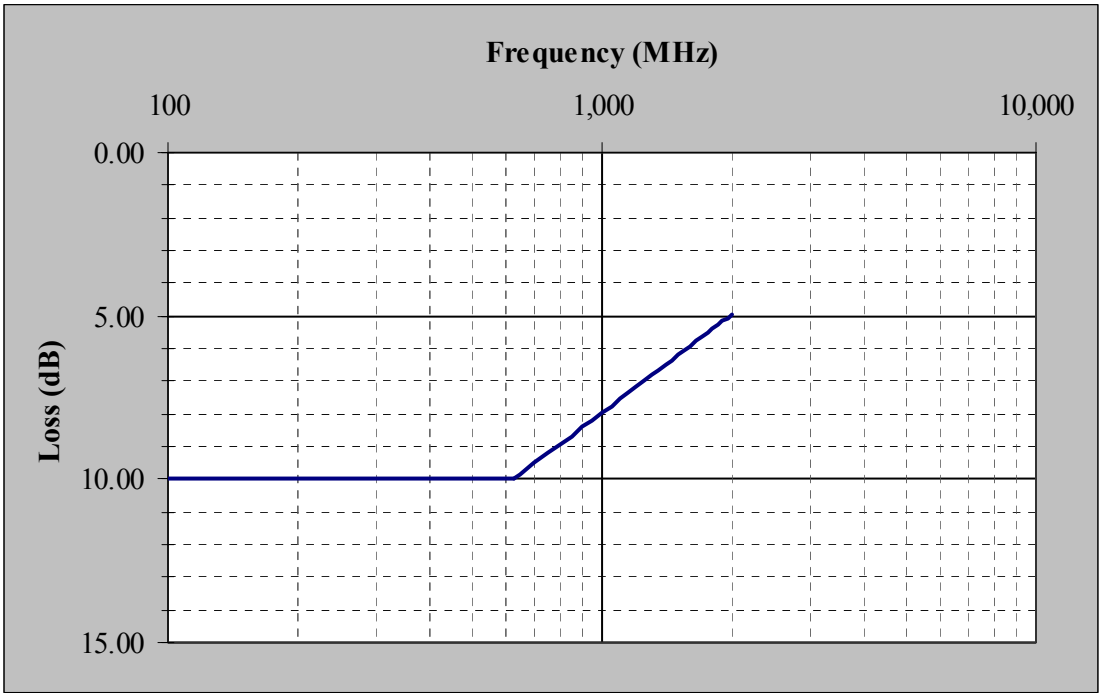


Figure 54–7—Receiver differential input return loss

54.7.4.6 Jitter tolerance

The total jitter is composed of three components: deterministic jitter, random jitter, and an additional sinusoidal jitter. The receiver shall tolerate the maximum deteministic, random and total jitter as defined in 54.7.3.8 with any compliant transmit signal, as defined in 54.7.3 through any compliant channel as defined in 54.8. The receiver shall tolerate an additional sinusoidal jitter with any frequency and amplitude defined by the mask of Figure 54–8. This additional component is intended to ensure margin for low-frequency jitter, wander, noise, crosstalk and other variable system effects. Jitter specifications include all but 10^{-12} of the jitter population. Jitter tolerance test requirements are specified in 54.10.1.

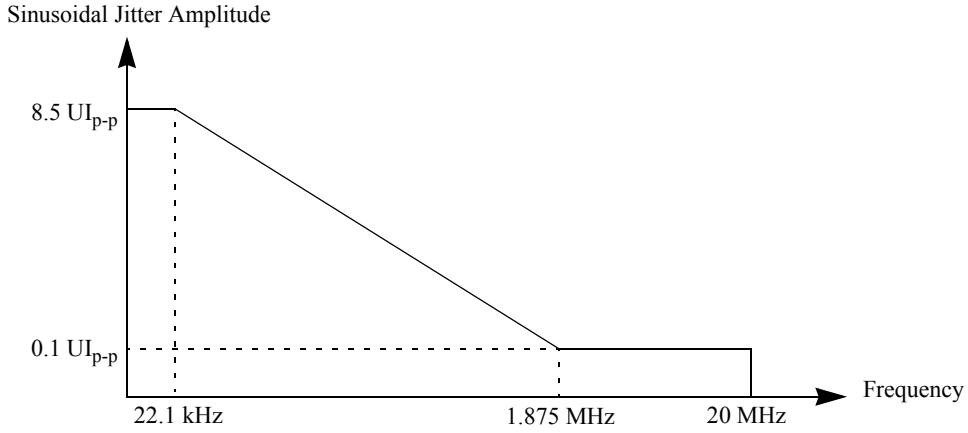


Figure 54–8—Single-tone sinusoidal jitter mask

54.8 Cable assembly characteristics

The 10GBASE-CX4 is primarily intended as a point-to-point interface of up to approximately 15 m between integrated circuits using controlled impedance cables. Loss and jitter budgets are presented in Table 54–9.

Table 54–9—Informative 10GBASE-CX4 loss and jitter budget

	Loss (dB) @ 1.5625 GHz	Total jitter (UI_{p-p})[a]	Random jitter (UI_{p-p})[a]	Deterministic jitter (UI_{p-p})[a]
Driver & package	0	0.35	0.18	0.17
PCBs[b]	1.0	0.02		0.02
Cable Assembly	16.5	0.18[c]		0.18
Other[d]	1.0	0.10		0.10
Total	18.5	0.65	0.18	0.47

[a]Jitter specifications include all but 10^{-12} of the jitter population.
[b]Loss is for 5.08cm of FR4 on each end of the link.
[c]The cable assembly jitter due to ISI may be larger than indicated and equalization is expected to limit to the indicated amount.
[d]Includes such effects as crosstalk, noise, and interaction between jitter and eye height.

Table 54–10—Cable assembly differential characteristics' summary

Description	Reference	Value	Unit
Characteristic Impedance @ TP2/TP3[a]	54.8.1	100 ± 10	Ω
Insertion loss at 1.5625 GHz (max.)	54.8.2 & 54.8.3	16.5	dB
Return loss at 1.5625 GHz (max.)	54.8.3	11.4	dB
Minimum NEXT loss at 1.5625 GHz (max.)	54.8.4.1	31.8	dB
Minimum MDNEXT loss at 1.5625 GHz (max.)	54.8.4.2	26.8	dB
Minimum ELFEXT loss at 1.5625 GHz (max.)	54.8.5.1	22.1	dB
Minimum MDELFEXT loss at 1.5625 GHz (max.)	54.8.5.2	20.1	dB

[a]The link impedance measurement identifies the impedance mismatches present in the cable assembly when terminated in its characteristic impedance. This measurement includes mated connectors at both ends of the Jumper cable assembly (points TP2 and TP3). The impedance for the jumper cable assembly, shall be recorded 4.0 ns following the reference location determined by an open connector at TP2 and TP3.

54.8.1 Characteristic impedance

The recommended differential characteristic impedance of circuit board trace pairs and the cable assembly is 100 Ω ± 10% from 100 MHz to 2.0 GHz.

54.8.2 Cable assembly insertion loss

The insertion loss, in dB with f in MHz, of each pair of the 10GBASE-CX4 cable assembly shall be:

$$InsertionLoss(f) \leq (0.2629 \cdot \sqrt{f}) + (0.0034 \cdot f) + \left(\frac{12.76}{\sqrt{f}}\right) + 0.5 \qquad \text{Eq. (54.3)}$$

for all frequencies from 100 MHz to 2.0 GHz. This includes the attenuation of the differential cabling pairs, and the assembly connector.

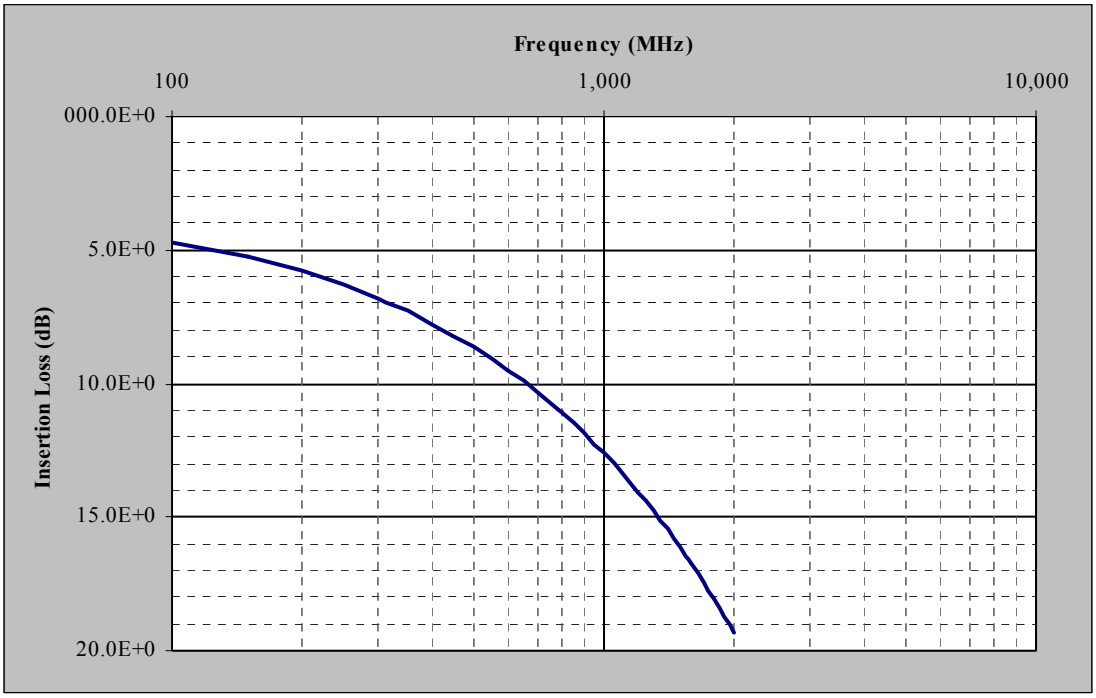


Figure 54–9—Cable assembly insertion loss

54.8.3 Cable assembly return loss

The return loss, in dB with f in MHz, of each pair of the 10GBASE-CX4 cable assembly shall be:

$$ReturnLoss(f) \geq 20 - 17.7 \times \log\left(\frac{f}{100}\right) \quad \text{Eq. (54.4a)}$$

for 100 MHz <= f < 500 MHz.

$$ReturnLoss(f) \geq 8 \quad \text{Eq. (54.4b)}$$

for 500 MHz <= f < 1000 MHz.

$$ReturnLoss(f) \geq 8 + 17.3 \times \log\left(\frac{f}{1000}\right) \quad \text{Eq. (54.4c)}$$

for 1000 MHz <= f < 2.0 GHz. This includes the attenuation of the differential cabling pairs, and the assembly connector.

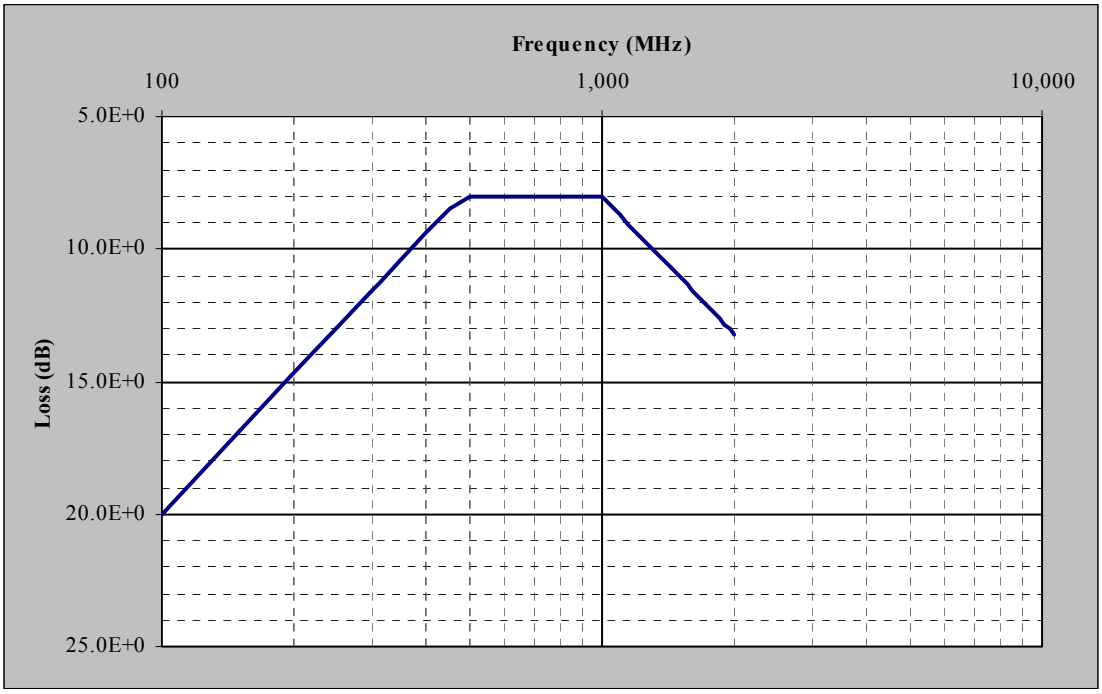


Figure 54–10—Cable assembly return loss

54.8.4 Near-End Crosstalk (NEXT)

54.8.4.1 Differential Near-End Crosstalk

In order to limit the crosstalk at the near end of a link segment, the differential pair-to-pair Near-End Crosstalk (NEXT) loss between the any of the four transmit channels and any of the four recieve channels is specified to meet the bit error rate objective specified in 54.7.4.1. The NEXT loss between any transmit and receive channel of a link segment, in dB with f in MHz, shall be at least

$$NEXT(f) \geq 30 - 17 \times \log\left(\frac{f}{2000}\right) \qquad \text{Eq. (54.5)}$$

for all frequencies from 100 MHz to 2.0 GHz. This includes the attenuation of the differential cabling pairs, and the assembly connector.

54.8.4.2 Multiple Disturber Near-End Crosstalk (MDNEXT)

Since four transmit and four recieve channels are used to transfer data between PMDs, the NEXT that is coupled into a receive channel will be from the four transmit channels. To ensure the total NEXT coupled into a receive channel is limited, multiple disturber NEXT loss is specified as the power sum of the individual NEXT losses.

The Power Sum loss between a receive channel and the four transmit channels, in dB with f in MHz, shall be at least

$$MDNEXT(f) \geq 25 - 17 \times \log\left(\frac{f}{2000}\right) \quad \text{Eq. (54.6)}$$

for all frequencies from 100 MHz to 2.0 GHz. This includes the attenuation of the differential cabling pairs, and the assembly connector.

MDNEXT loss is determined by summing the magnitude of the four individual pair-to-pair differential NEXT loss values over the frequency range 100 MHz to 2.0 GHz as follows:

$$\text{MDNEXT\_Loss(f)} = -10\log_{10}\sum_{i=0}^{i=3} 10^{-(NL(f)i)/10} \quad \text{Eq. (54.7)}$$

where

NL(*f*)i is the magnitude of NEXT loss at frequency *f* of pair combination i

i is the 0, 1, 2, or 3 (pair-to-pair combination)

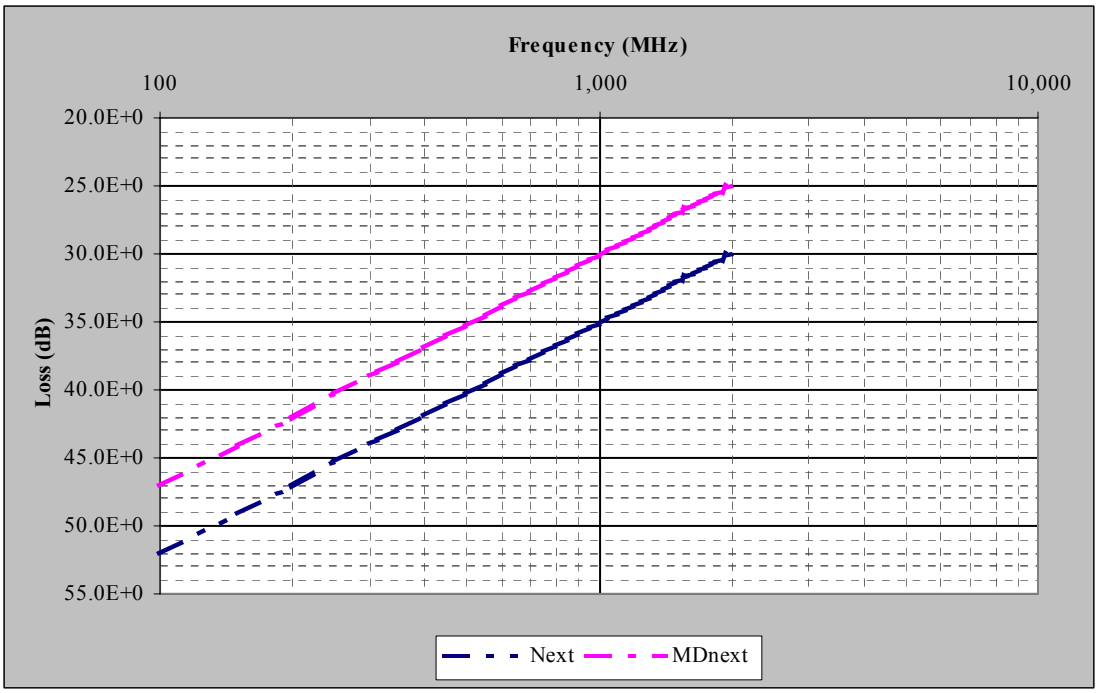


Figure 54–11—Cable assembly NEXT / MDNEXT loss

54.8.5 Far-End Crosstalk (FEXT)

54.8.5.1 Equal Level Far-End Crosstalk (ELFEXT) loss

Equal Level Far-End Crosstalk (ELFEXT) loss is specified in order to limit the crosstalk at the far end of each link segment duplex channel and meet the BER objective specified in 54.7.4.1. Far-End Crosstalk

(FEXT) is crosstalk that appears at the far end of a duplex channel (disturbed channel), which is coupled from another duplex channel (disturbing channel) with the noise source (transmitters) at the near end. FEXT loss is defined as

$$FEXT\_Loss(f) = 20\log_{10}[V\text{pds}(f)/V\text{pcn}(f)]$$

and ELFEXT_Loss is defined as

$$ELFEXT\_Loss(f) = 20\log_{10}[V\text{pds}(f)/V\text{pcn}(f)] - SLS\_Loss(f)$$

where

*V*pds is the peak voltage of disturbing signal (near-end transmitter)
*V*pcn is the peak crosstalk noise at far end of disturbed channel
SLS_Loss is the insertion loss of disturbed channel in dB

The worst pair ELFEXT loss between any two duplex channels shall be at least:

$$ELFEXT(f) \geq 20 - 20 \times \log\left(\frac{f}{2000}\right) \quad \text{Eq. (54.8)}$$

for all frequencies from 100 MHz to 2.0 GHz. This includes the attenuation of the differential cabling pairs, and the assembly connector.

54.8.5.2 Multiple Disturber Equal Level Far-End Crosstalk (MDELFEXT) loss

Since four duplex channels are used to transfer data between PMDs, the FEXT that is coupled into a data carrying channel will be from the three adjacent disturbing duplex channels. This specification is consistent with three channel-to-channe. To ensure the total FEXT coupled into a duplex channel is limited, multiple disturber ELFEXT loss is specified as the power sum of the individual ELFEXT losses.

The Power Sum loss between a duplex channel and the three adjacent disturbers shall be at least:

$$MDELFEXT(f) \geq 18 - 20 \times \log\left(\frac{f}{2000}\right) \quad \text{Eq. (54.9)}$$

for all frequencies from 100 MHz to 2.0 GHz. This includes the attenuation of the differential cabling pairs, and the assembly connector.

54.8.5.2.1 Multiple-Disturber Power Sum Equal Level Far-End Crosstalk (PSELFEXT) loss

PSELFEXT loss is determined by summing the magnitude of the three individual pair-to-pair differential ELFEXT loss values over the frequency range 100 MHz to 2.0 GHz as follows:

$$PSELFEXT(\text{f}) = -10\log_{10}\sum_{i=1}^{i=3} 10^{-(NL(f)i)/10} \quad \text{Eq. (54.10)}$$

where

NL(*f*)i is the magnitude of FEXT loss at frequency *f* of pair combination i
i is the 1, 2, or 3 (pair-to-pair combination)

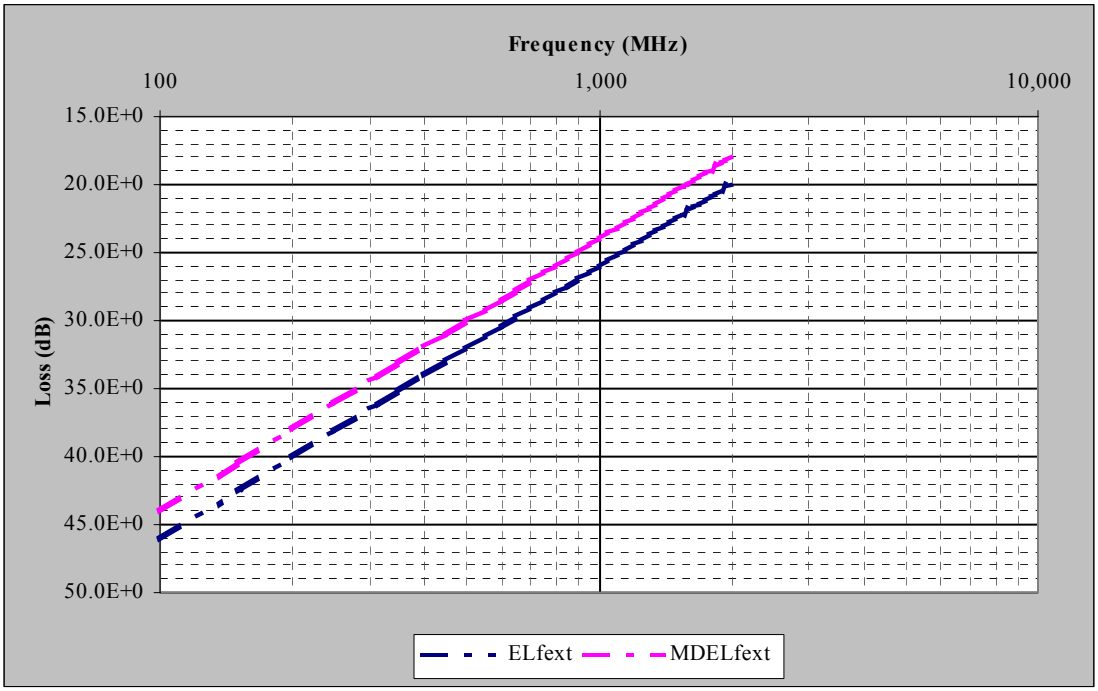


Figure 54–12—Cable assembly ELFEXT / MDELFEXT loss

54.8.6 Shielding

The cable assembly shall provide class 2 or better shielding in accordance with IEC 61196-1.

54.9 MDI specification

This sub-clause defines the Media Dependent Interface (MDI). The 10GBASE-CX4 PMD of 54.7 is coupled to the cable assembly of 54.8 by the media dependent interface (MDI).

54.9.1 MDI connectors

Connectors meeting the requirements of 54.9.1.1 shall be used as the mechanical interface between the PMD of 54.7 and the cable assembly of 54.8. The MDI connector shall be used on the cable assembly and the MDI receptacle on the PHY.

54.9.1.1 Connector specification

The connector for the cable assemblies shall be the latch type with the mechanical mating interface defined by SFF-8470, having pinouts matching those in Table 54–2, and the signal quality and electrical requirements of 54.7 and 54.8.

Editor's Note: replace SFF-8470 with IEC number prior to final approval.

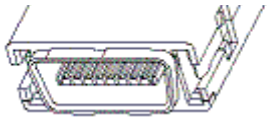


Figure 54–13—Example MDI connector

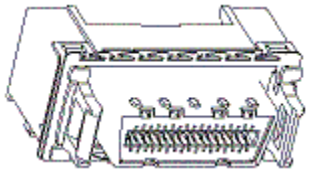
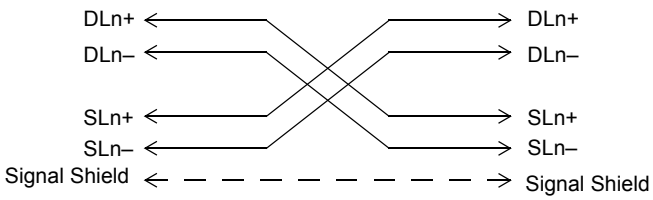


Figure 54–14—Example MDI receptacle

54.9.2 Crossover function

The default cable assembly shall be wired in a crossover fashion as shown in Figure 54–15, with each of the four pairs being attached to the transmitter contacts at one end and the receiver contacts at the other end.



Note: [SL*i*<P> and SL*i*<N> are the positive and negative sides of the differential signal pair for Lane *i* (*i*=0,1,2,3)]

Figure 54–15—Cable wiring

54.10 Electrical measurement requirements

54.10.1 Jitter test requirements

For the purpose of jitter measurement, the effect of a single-pole high pass filter with a 3 dB point at 1.875 MHz is applied to the jitter. The data pattern for jitter measurements is the CJPAT pattern defined in Annex 48A. All four lanes of the 10GBASE-CX4 transciever are active in both directions, and opposite ends of the link use asynchronous clocks. Jitter is measured with AC coupling and at 0 volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER bathtub curve such as that described in Annex 48B.

54.10.1.1 Transmit jitter

Transmit jitter is measured at the MDI output when terminated into the load specified in 54.7.3.2.

54.10.1.2 Jitter tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the required sum of deterministic and random jitter defined in 54.7.4.6 on any compliant transmit output waveform as define in 54.7.3.6 and then passing the signal through any compliant cable assembly as defined in 54.8.2. Random jitter is calibrated using a high pass filter with a low-frequency corner of 20 MHz and 20 dB/decade rolloff. The required sinusoidal jitter specified in 54.7.4.6 is then added to the signal and the far-end load is replaced by the receiver being tested.

54.11 Environmental specifications

All equipment subject to this clause shall conform to the applicable requirements of 14.7 and applicable sections of ISO/IEC 11801: 1995.

54.12 Protocol Implementation Conformance Statement (PICS) proforma for Clause 54., Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4[1]

54.12.1 Introduction

The supplier of a protocol implementation that is claimed to conform to IEEE Std 802.3ak-2003, Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4, shall complete the following Protocol Implementation Conformance Statement (PICS) proforma. A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

[1] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

54.12.2 Identification

54.12.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTES 1—Required for all implementations. 2—May be completed as appropriate in meeting the requirements for the identification. 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

54.12.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3ak-2003, Clause 54., Physical Medium Dependent (PMD) sublayer and baseband medium, type 10GBASE-CX4
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3ak-2003.)	

Date of Statement	

54.12.3 PICS proforma tables for 10GBASE-CX4 and baseband medium

54.12.3.1 Compatibility considerations

Item	Feature	Subclause	Value/Comment	Status	Support
CC1	Jitter test patterns	54.10.1	As per Annex 48A	M	Yes [ ]
CC2	Environmental specifications	54.11		M	Yes [ ]

54.12.4 Major capabilities / options

Item	Feature	Subclause	Value/Comment	Status	Support
CX4	10GBASE-CX4 PMD	54.1		O	Yes [ ] No [ ]
MC1	XGMII interface	54.1	Device integrates Clause 46 XGMII interface?	O	Yes [ ] No [ ]
MC2	XGXS & XAUI	54.1	Device integrates Clause 47 XGXS and XAUI interface?	O	Yes [ ] No [ ]
MC3	10GBASE-X PCS/PMA	54.1, 54.2	Device integrates Clause 48 10GBASE-X PCS/PMA?	M	Yes [ ]
MC4	XAUI lane to MDI lane assignment	54.3	Device supports connector pin assignments in Table 54–2	M	Yes [ ]
DC	Delay constraints	54.4	Delay no more than 512 BT	M	Yes [ ]
*MD	MDIO capability	54.5	Registers and interface supported	O	Yes [ ] No [ ]
TP1	Standardized reference point TP1 exposed and available for testing	54.6.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]
TP4	Standardized reference point TP4 exposed and available for testing	54.6.1	This point may be made available for use by implementers to certify component conformance	O	Yes [ ] No [ ]

54.12.4.1 PMD Functional specifications

Item	Feature	Sub clause	Value/Comment	Status	Support
PF1	Transmit function	54.6.2	Convey bits requested by PMD_UNITDATA.request() to the MDI	M	Yes [ ]
PF2	Delivery to the MDI	54.6.2	Supplies electrical signal streams for delivery to the MDI	M	Yes [ ]
PF3	Mapping between electrical signal and logical signal for transmitter	54.6.2	A positive differential votlage is a one	M	Yes [ ]
PF4	Receive function	54.6.3	Convey bits received from the MDI to PMD_UNITDATA.indicate(rx_bit<0:3>)	M	Yes [ ]
PF5	Conversion of four electrical signals to four electrical signals	54.6.3	Converts the four electrical signal streams into four electrical bit streams for delivery to the PMD service interface	M	Yes [ ]
PF6	Mapping between electrical signal and logical signal for receiver	54.6.3	A positive differential voltage is a one	M	Yes [ ]
PF7	Receive function behavior	54.6.3	Conveys bits from PMD service primitive to the PMD service interface	M	Yes [ ]
PF8	Global PMD Signal Detect function	54.6.4	Report to the PMD service interface the message PMD_SIGNAL.indicate(SIGNAL_DETECT)	M	Yes [ ]
PF11	Global PMD Signal Detect behavior	54.6.4	SIGNAL_DETECT is a global indicator of the presence of electrical signals on all four lanes	M	Yes [ ]
PF12	Global PMD Signal Detect OK threshold	54.6.4	SIGNAL_DETECT = OK for signal value >= 175mVppd for at least 1 UI	M	Yes [ ]
PF13	Global PMD Signal Detect OK response	54.6.4	SIGNAL_DETECT = OK indicated within 100µs	M	Yes [ ]
PF14	Global PMD Signal Detect FAIL threshold	54.6.4	SIGNAL_DETECT = FAIL for signal level < 50mVppd for 250µs to 500µs	M	Yes [ ] No [ ]
PF16	Lane-by-Lane Signal Detect function	54.6.5	Sets PMD_signal_detect_n values on a lane-by-lane basis per requirements of section 54.6.4	MD:M	Yes [ ] No [ ] NA [ ]
PF17	PMD_reset function	54.6.6	Resets the PMD sublayer	MD:M	Yes [ ] No [ ] NA [ ]
PF18	Loop Back	54.6.9	Loopback function provided	M	Yes [ ]

54.12.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Management register set	54.5		MD:M	Yes [ ] N/A [ ]
MF2	Global_PMD_transmit_disable	54.6.7	Disables all transmitters by forcing a constant output state	MD:O	Yes [ ] No [ ] NA [ ]
MF3	PMD_fault disables transmitter	54.6.7	Disables all transmitters by forcing a constant output state when a fault is detected	MD:O	Yes [ ] No [ ] NA [ ]
MF4	Effect on loopback of Global_PMD_transmit_disable	54.6.7	Global_PMD_transmit_disable does not affect loopback function	MD:M	Yes [ ] No [ ] NA [ ]
MF5	PMD_transmit_disable_n	54.6.8	Disables transmitter n (n=0:3) by forcing a constant output state	M	Yes [ ] No [ ]
MF6	PMD_fault disables transmitter n	54.6.8	Disables transmitter n (n=0:3) by forcing a constant output state when a fault is detected	O	Yes [ ] No [ ] NA [ ]
MF7	Effect on loopback of PMD_transmit_disable_n	54.6.8	PMD_transmit_disable_n does not affect loopback function	M	Yes [ ] No [ ] NA [ ]
MF8	PMD_fault function	54.6.10	Sets PMD_fault to a logical 1 if any local fault is detected	MD:M	Yes [ ] No [ ]
MF9	PMD_transmit_fault function	54.6.11	Sets PMD_transmit_fault_n to a logical 1 if a local fault is detected on the transmit path x	MD:M	Yes [ ] No [ ]
MF10	PMD_receive_fault function	54.6.12	Sets PMD_receive_fault_x to a logical 1 if a local fault is detected on the receive path x	MD:M	Yes [ ] No [ ]

54.12.4.3 Transmitter specifications

Item	Feature	Subclause	Value/Comment	Status	Support
DS1	Test performed at TP2	54.7.3		M	Yes [ ]
DS2	Test ficture	54.7.3.1	Test ficture of Figure 54–3 or equivalent used	M	Yes [ ]
DS3	Test load	54.7.3.2	2 x 50 ohm load used	M	Yes [ ]
DS4	Baud Rate	54.7.3.3	3.125GBd ± 100ppm	M	Yes [ ]
DS5	Maximum driver output amplitude	54.7.3.4	Less than 1600 mVppd	M	Yes [ ]
DS6	Minimum peak driver output amplitude	54.7.3.4	Greater than 800mVppd	M	Yes [ ]
DS7	Common mode output voltage	54.7.3.4	Between –0.4 and +1.9 V	M	Yes [ ]
DS8	Driver output impedance	54.7.3.5	Per Eq. (54.1a) and Eq. (54.1b)	M	Yes [ ]
DS9	Driver output template test pattern	54.7.3.6	Per 48A.2	M	Yes [ ]
DS10	Driver output normalization	54.7.3.6	Per process defined in 54.7.3.6	M	Yes [ ]
DS11	Driver output template	54.7.3.6	Lies within template	M	Yes [ ]
DS12	Transition time	54.7.3.7	Between 60-130ps	M	Yes [ ]
DS13	Jitter test requirements	54.10.1	Meet BER bathtub curve, See Annex 48B	M	Yes [ ]
DS14	Total jitter	54.7.3.8	less than ± 0.175 UIp	M	Yes [ ]
DS15	Deterministic jitter	54.7.3.8	less than ± 0.085 UIb	M	Yes [ ]
DS16	Random jitter	54.7.3.8	less than ± 0.09 UIp	M	Yes [ ]

54.12.4.4 Receiver specifications

Item	Feature	Subclause	Value/Comment	Status	Support
RS1	Bit Error Ratio	54.7.4.1	BER of better than 10^{-12}	M	Yes [ ]
RS2	Baud rate tolerance	54.7.4.2	3.125GBd ± 100ppm	M	Yes [ ]
RS3	A.C. Coupling	54.7.4.3		M	Yes [ ]
RS4	Input amplitude tolerance	54.7.4.4	Accepts signals compliant with 54.7.3, may be larger than 1600 mV_{ppd}	M	Yes [ ]
RS5	Input impedance	54.7.4.5	Per Eq. (54.2a) and Eq. (54.2b)	M	Yes [ ]
RS6	Jitter tolerance	54.7.4.6	Per 54.7.3.8	M	Yes [ ]
RS7	Additional sinusoidal jitter tolerance	54.7.4.6	Per Figure 54–8	M	Yes [ ]
RS8	Jitter test requirements	54.10.1	Meet BER bathtub curve, See Annex 48B	M	Yes [ ]

54.12.4.5 Cable assembly specifications

Item	Feature	Subclause	Value/Comment	Status	Support
CA1	Characteristic Impedance	54.8.1	100 Ω ± 10%	O	Yes [ ]
CA2	Insertion loss	54.8.2	Per Eq. (54.3)	M	Yes [ ]
CA3	Return loss	54.8.2	Per Eq. (54.4a), Eq. (54.4b) and Eq. (54.4c)	M	Yes [ ]
CA4	Near-End cross talk	54.8.4.1	Per Eq. (54.5)	M	Yes [ ]
CA5	MDNear-End cross talk	54.8.4.2	Per Eq. (54.6)	M	Yes [ ]
CA6	ELFar-End cross talk	54.8.5.1	Per Eq. (54.8)	M	Yes [ ]
CA7	MDELFar-End cross talk	54.8.5.2	Per Eq. (54.9)	M	Yes [ ]
CA8	Shielding	54.8.6	Class 2 or better in accordance with IEC 61196-1	M	Yes [ ]
CA9	MDI connectors	54.9.1	Used as the mechanical interface for 54.7 and 54.8	M	Yes [ ]
CA10	MDI connector	54.9.1	Used on the cable assembly	M	Yes [ ]
CA11	MDI receptacle	54.9.1	Used on the PHY	M	Yes [ ]
CA12	Connector type	54.9.1.1	SFF-8470 latch type	M	Yes [ ]
CA13	Crossover function	54.9.2	Per Figure 54–15	M	Yes [ ]