Analog Front Ends for Ethernet on Copper

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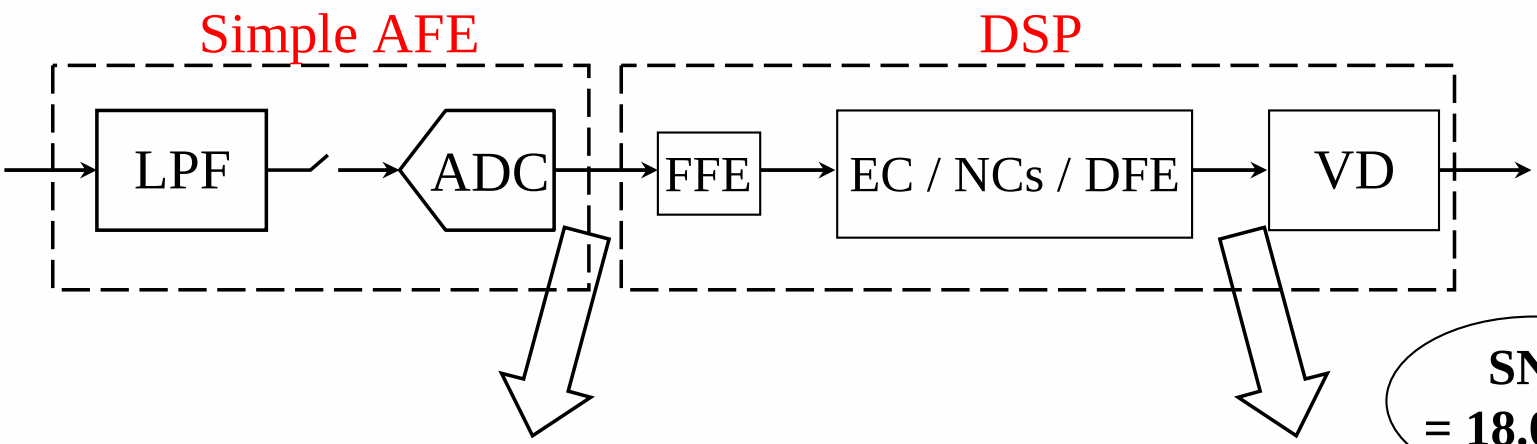
Outline

- Overview of high-speed Ethernet over UTP
- Quantization noise boosting
- State-of-the-art in CMOS ADC's
- Overview of our work on gigabit Ethernet AFE's
- Analog Filtering Techniques
- Overview of our Gm-C AFE filter work
- Gigabit Ethernet summary
- Comments on 10Gbit Ethernet

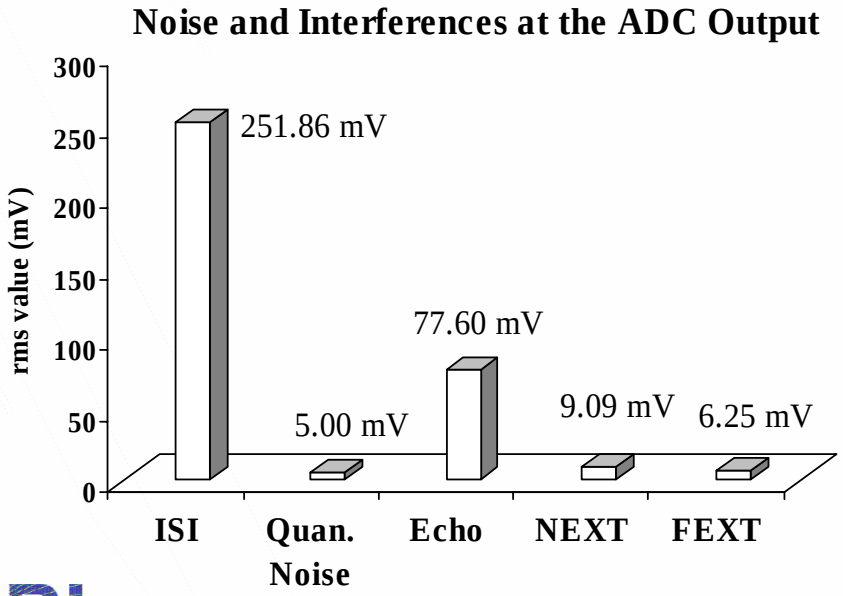
High-Speed Ethernet over UTP

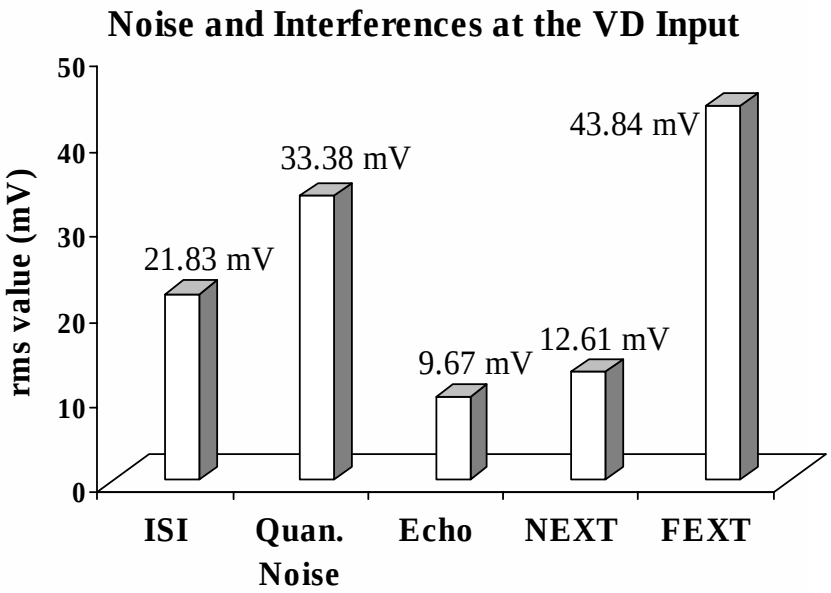
- Low SNR requires complex signal processing
  - Best handled in digital circuits (back-end DSP)
- All implementations require an analog front end, so the question is: What should be in the AFE?
  - An ADC of course
  - A LPF for anti-aliasing and to reject out of band noise
  - A VGA to handle variable signal levels
- But, a more complex AFE may be beneficial
  - Can do some echo cancellation
  - Can do some equalization
  - Net result may be a significant reduction in overall cost & power

Quantization Noise Boosting

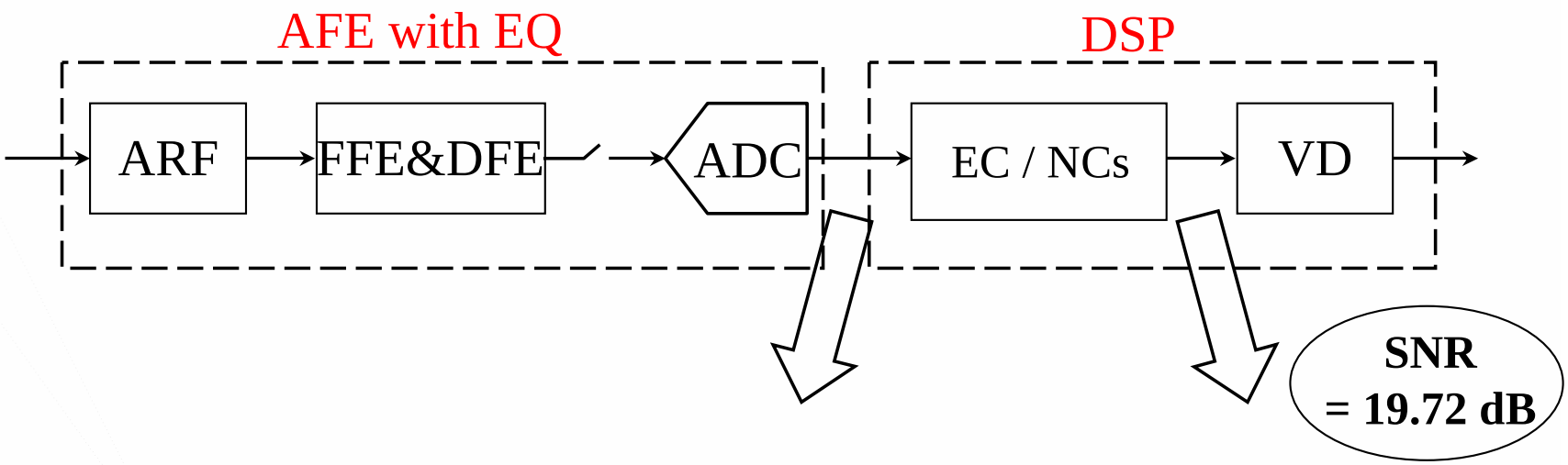


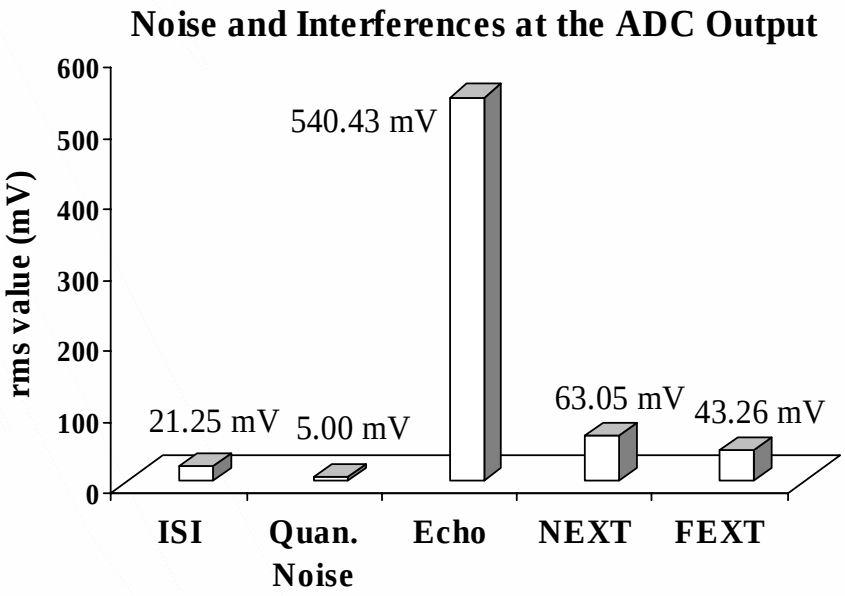
SNR = 18.00 dB

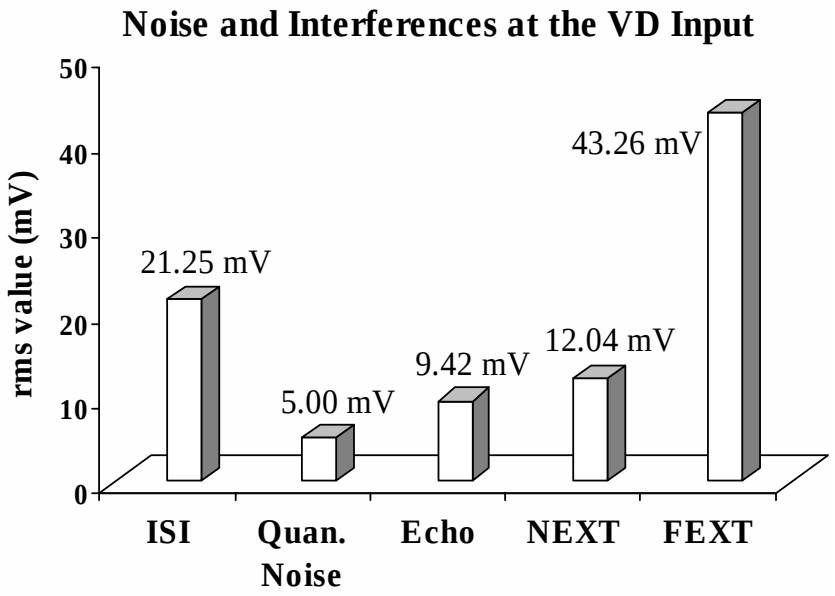




Reduced Quantization Noise Boosting



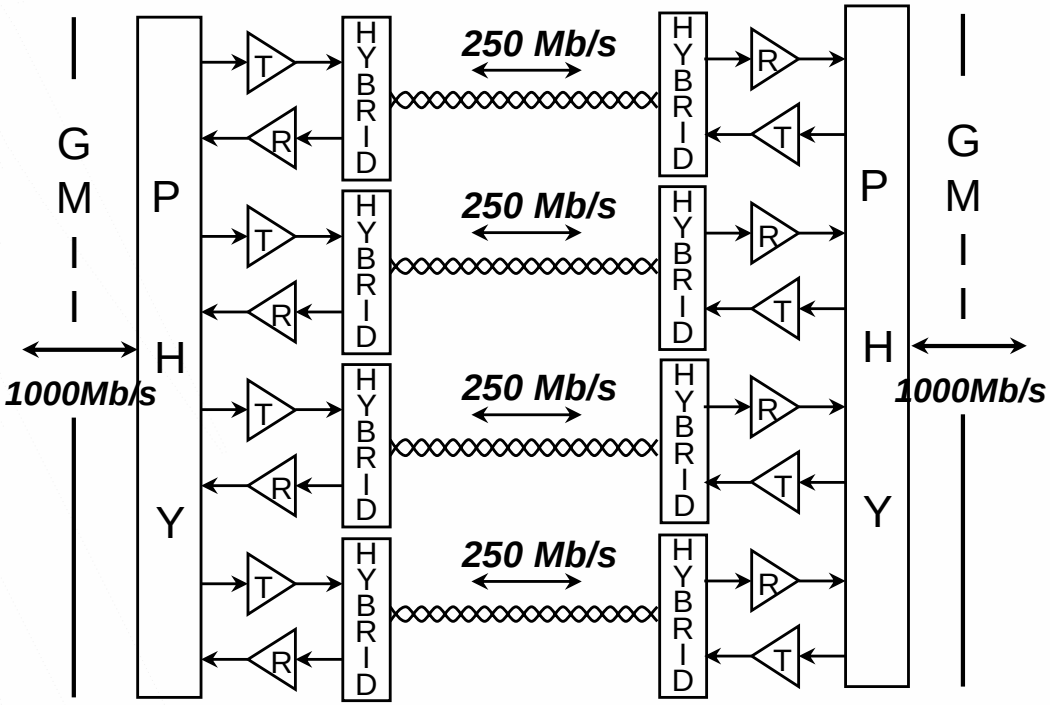




State of the Art in High-Speed CMOS ADC's

- 2 GS/s, 6b ADC in 0.18 μm CMOS
  - Jiang et. al., UCLA & Broadcom, ISSCC'03
  - No interleaving, 5.7 ENOB, 0.5 mm^2, 310 mW, 1.8 V
- 20 GS/s, 8b ADC in 0.18 μm CMOS
  - Poulton et. al., Agilent, ISSCC'03
  - Uses interleaving, 4.6-6.5 ENOB, 196 mm^2, 9 W
  - Requires BiCMOS buffer chip
- What would 1 GS/s at 11 ENOB require?
  - Huge sampling capacitors to keep KT/C noise down (~4 pF)
  - Extremely low jitter sampling clock (~100 fs)
  - These specifications are not attainable in the near future in standard digital CMOS processes

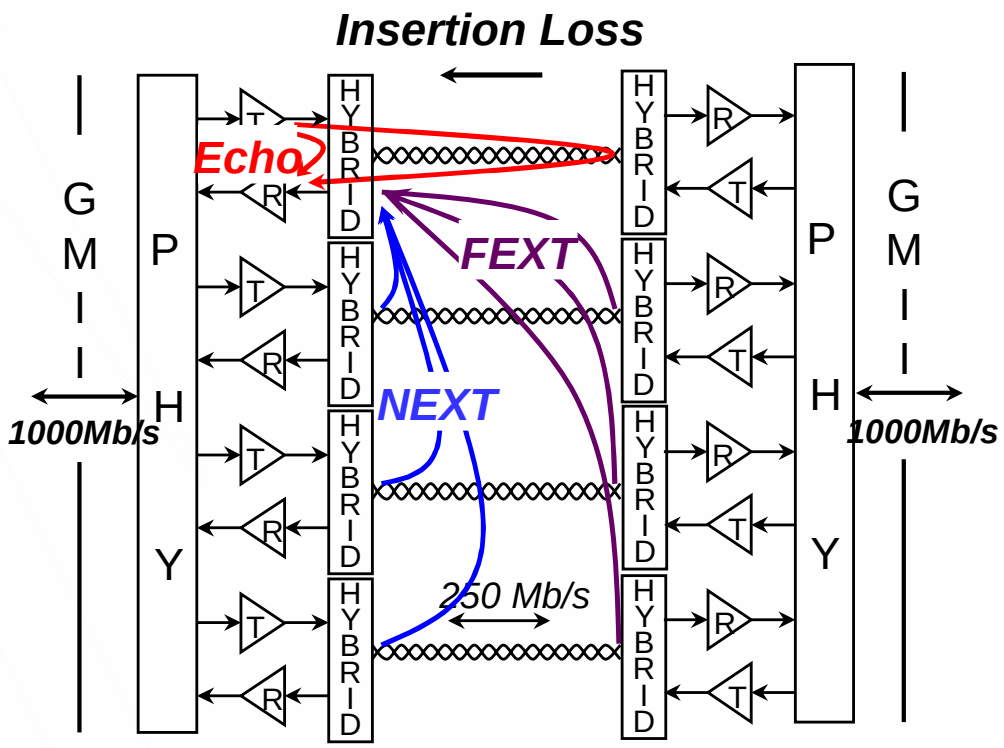
Gigabit Ethernet 1000BASE-T (I)



1000BASE-T:

- Provides 1000 Mb/s Ethernet service
- Uses 4 cat-5 UTP's
- 5-level TCM symbols sent at 125 MS/s per UTP
- Distance: up to 100 meters

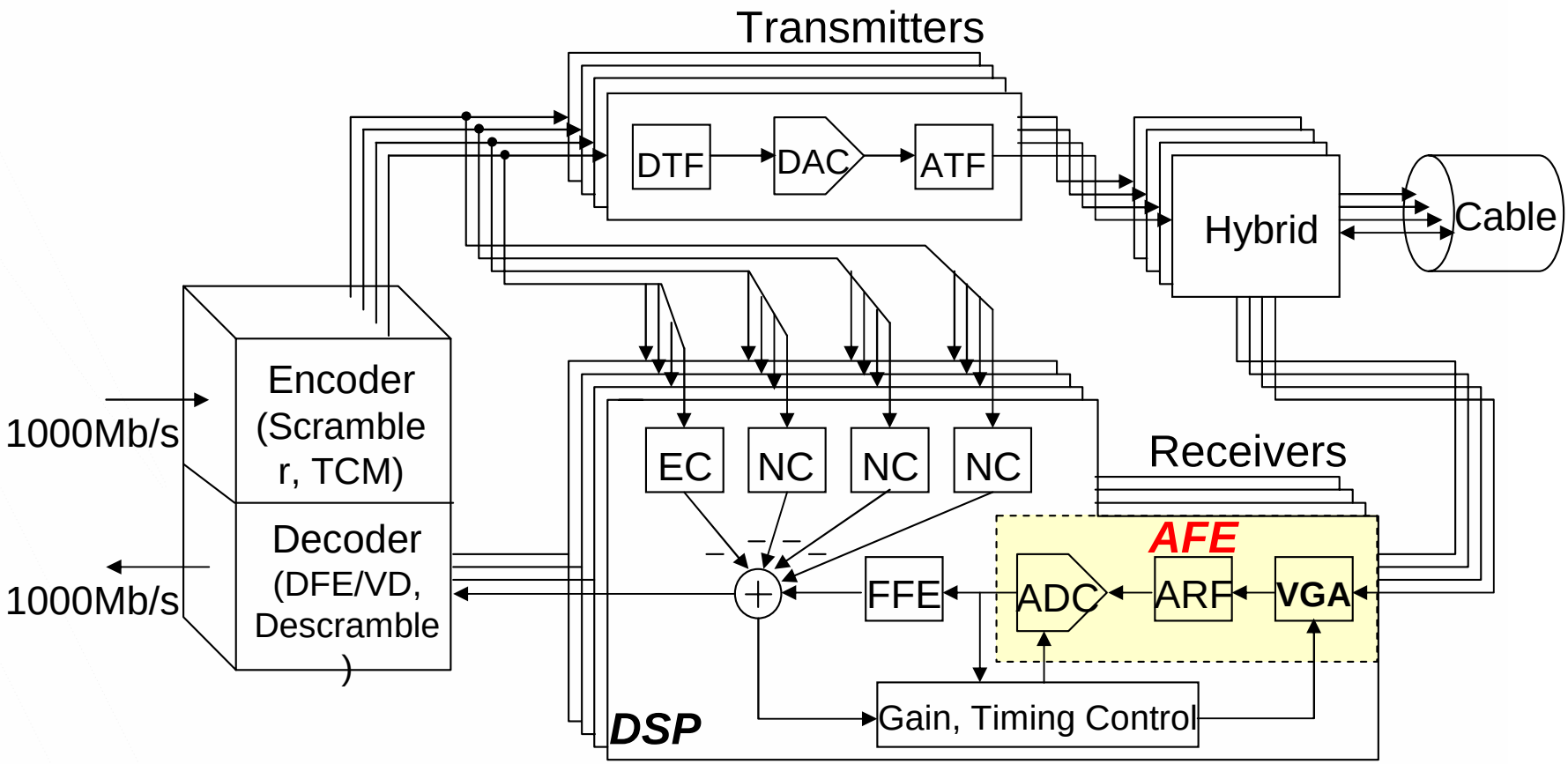
Gigabit Ethernet 1000BASE-T (II)



Major impairments:

- Insertion loss
- Interference
  - Echo
  - Near-end crosstalk (NEXT)
  - Far-end crosstalk (FEXT)

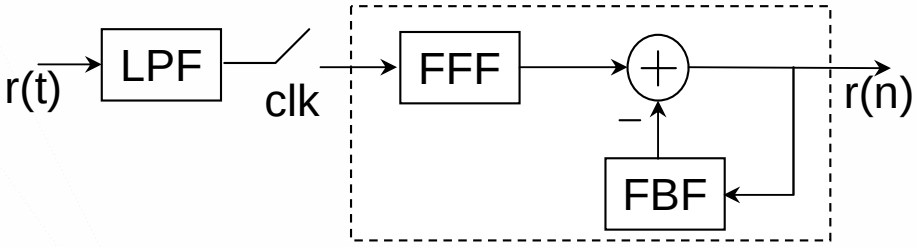
A Mostly Digital Transceiver



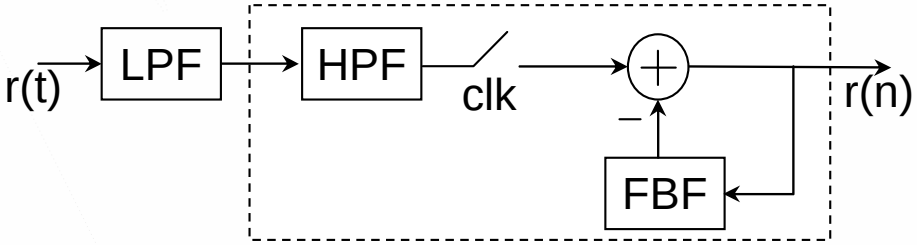
AFE Architectures Compared

- **AFE with partial equalization**

IIR Pre-EQ:



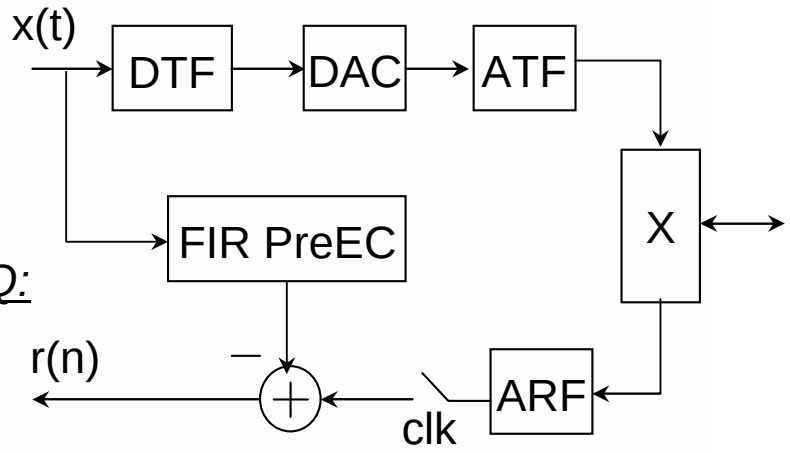
High pass filter-feedback filter (HPF-FBF) Pre-EQ:



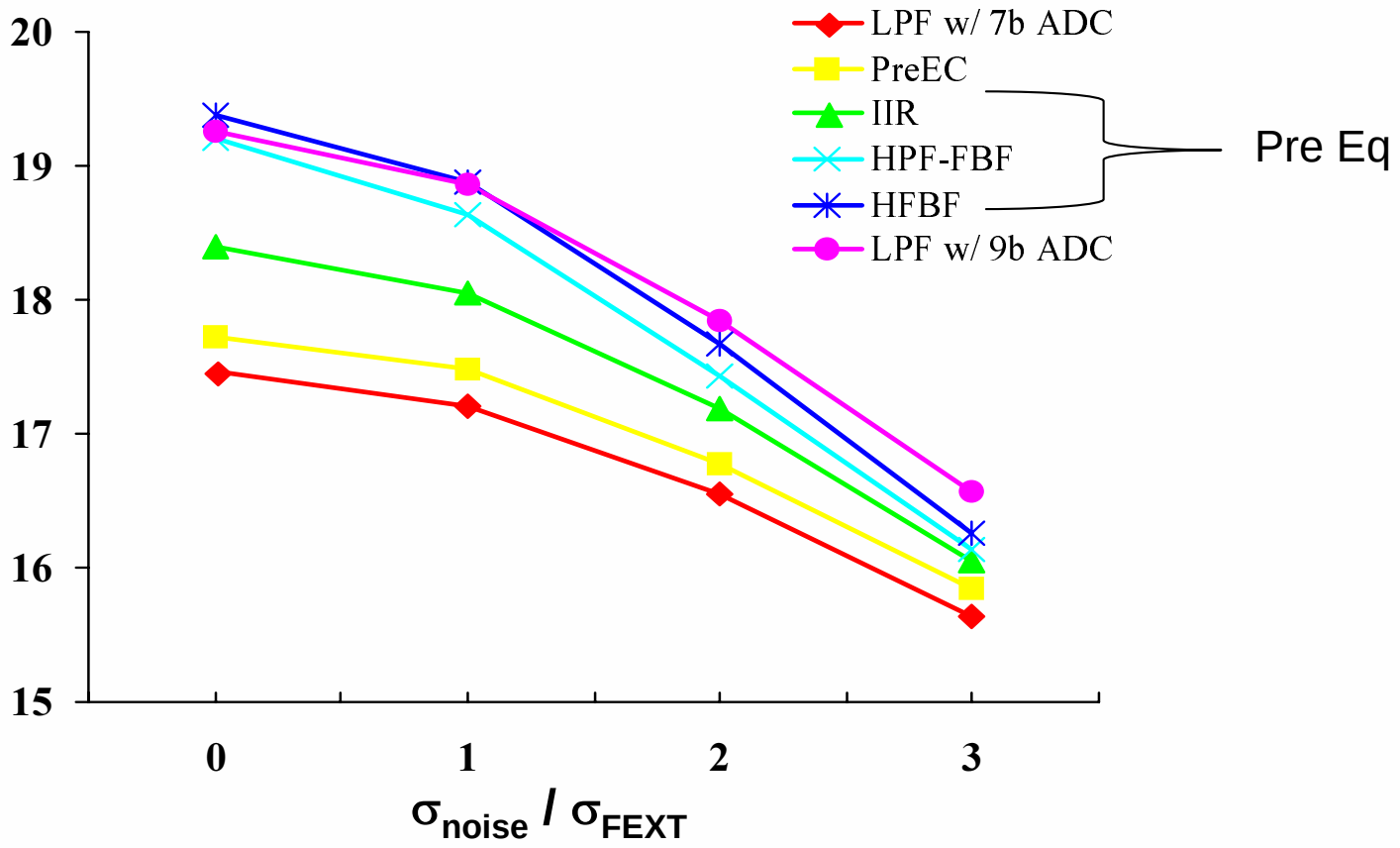
High-frequency boost filter (HFBF) Pre-EQ:

- **AFE with partial Echo cancellation**

FIR PreEC:

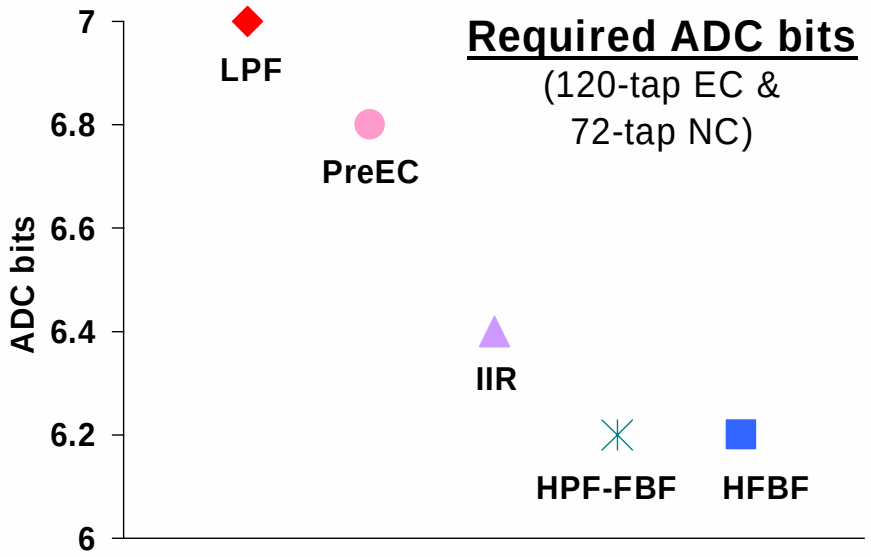


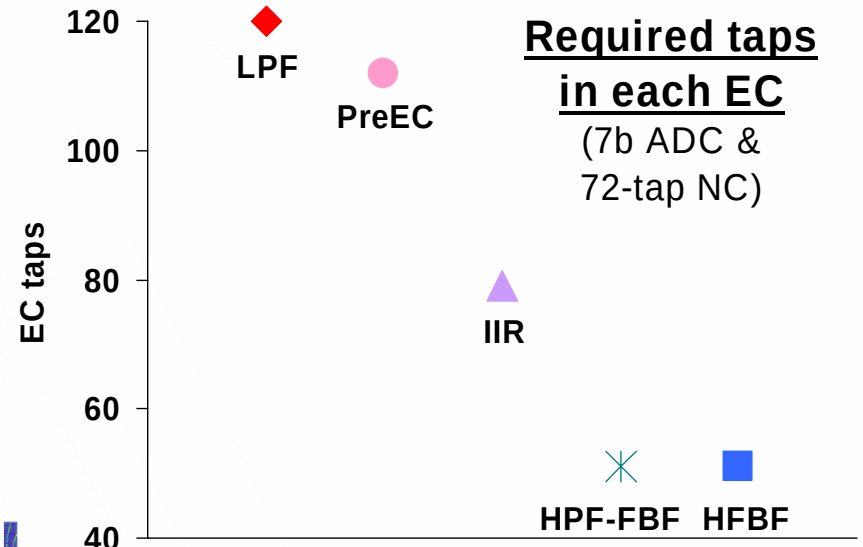
Simulation Results

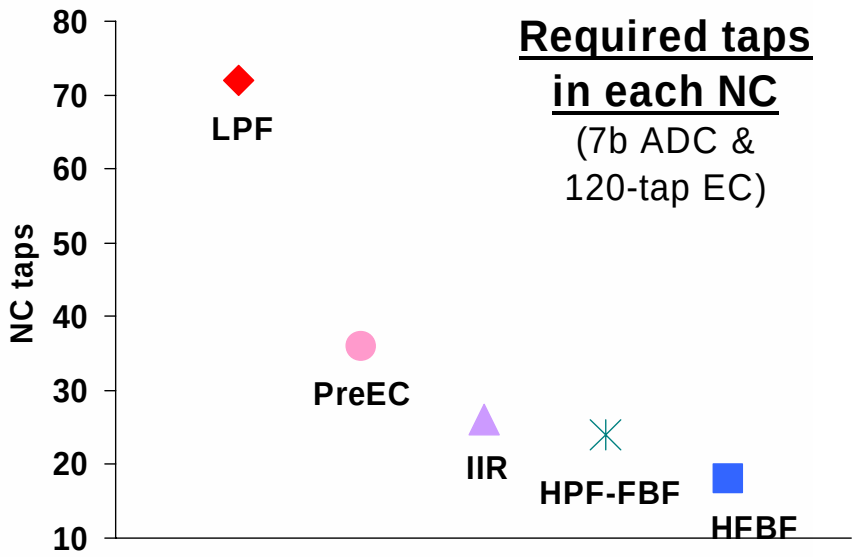


- All proposed AFE architectures can improve the SNR
- PreEC has moderate performance improvement
- HFBF and HPF-FBF increase the detection SNR by nearly 2dB

Simplifications of ADC and Digital Filters







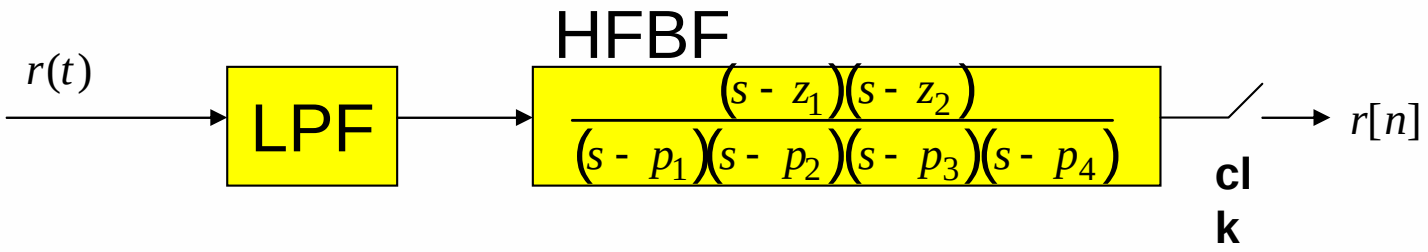
High-Frequency Boost Filter (HFBF)

- Purpose
  - Perform HF boost for partial equalization prior to the ADC quantization noise being added to the signal
- Performance [3]
  - Detection SNR can be increased by almost 2dB
  - Receiver DSP simplifications:
    - ADC effective bits: 7 bits $\rightarrow$ 6.2 bits
    - *Or* each EC filter: 120 taps $\rightarrow$ 51 taps
    - *Or* each NC filter: 72 taps $\rightarrow$ 18 taps

[3]: J.Huang and R.Spencer, *"Simulated Performance of 1000BASE-T Receiver with Different Analog Front End Designs"*, Proc. of 35th Asilomar Conf. on Signals, Systems, and Computers, 2001

HFBF Topology

- HFBF topology [3]

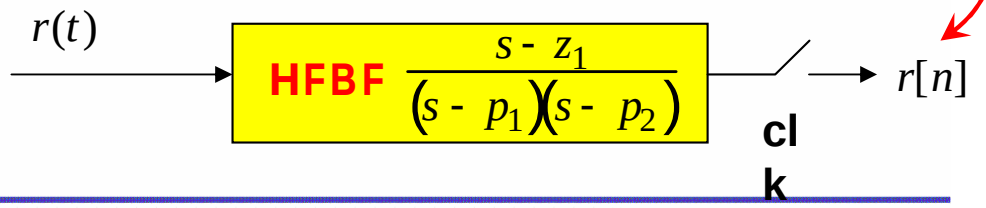


- Optimization of HFBF topology
  - Combine the function of LPF and HFBF together
  - Select proper number and type of poles and zeros

Performances of Different HFBF Topologies

HFBF Topologies	Transfer Function	SNR (dB)
One-stage filter with real poles	$\frac{s-z_1}{(s-p_1)(s-p_2)}$	18.94
Two-stage filter with real poles	$\frac{s-z_1}{(s-p_1)(s-p_2)}\frac{s-z_2}{(s-p_3)(s-p_4)}$	19.18
One-stage filter with complex poles	$\frac{s-z_1}{(s-p_1)(s-p_1^*)}$	18.92
Two-stage filter with complex poles	$\frac{s-z_1}{(s-p_1)(s-p_1^*)}\frac{s-z_2}{(s-p_2)(s-p_2^*)}$	19.05
LPF + One-stage filter with real poles	$H_{LPF}(s)\frac{s-z_1}{(s-p_1)(s-p_2)}$	18.97
LPF + Two-stage filter with real poles	$H_{LPF}(s)\frac{s-z_1}{(s-p_1)(s-p_2)}\frac{s-z_2}{(s-p_3)(s-p_4)}$	19.23

- ***A one-stage filter with real poles and no separate LPF*** is the most promising topology overall.



Integrated Analog Filtering Techniques; Discrete Time

- Switched-Capacitor filters

Advantages	Disadvantages
accurate transfer function	need CT LPF
easily programmable	need high-BW opamps
	need clocks
	need timing recovery

  - Not practical at these frequencies

- Finite-Impulse Response Filters

Advantages	Disadvantages
accurate transfer function	need CT LPF
easily programmable	need clocks
easily adaptable	need timing recovery
	need multipliers
	need large S/H caps

  - Can also be continuous time

Integrated Analog Filtering Techniques; Continuous Time

- Finite-Impulse Response Filters

Advantages	Disadvantages
accurate transfer function	need multipliers
easily programmable	limited total delay
easily adaptable	hard to get accurate delay
	can be noisy

- Transconductance-Capacitance (Gm-C) Filters

Advantages	Disadvantages
open loop (high speed)	need tuning control loop
programmable	difficult to adapt
	sensitive to parasitics
	can be noisy

- MOSFET-C filters

Advantages	Disadvantages
lower noise	need high-BW opamp
	slower & nonlinear
	need tuning control loop

Integrated Analog Filtering Techniques; Continuous Time II

- Active RC filters

Advantages	Disadvantages
lower noise	need high-BW opamp need resistors need tuning control loop

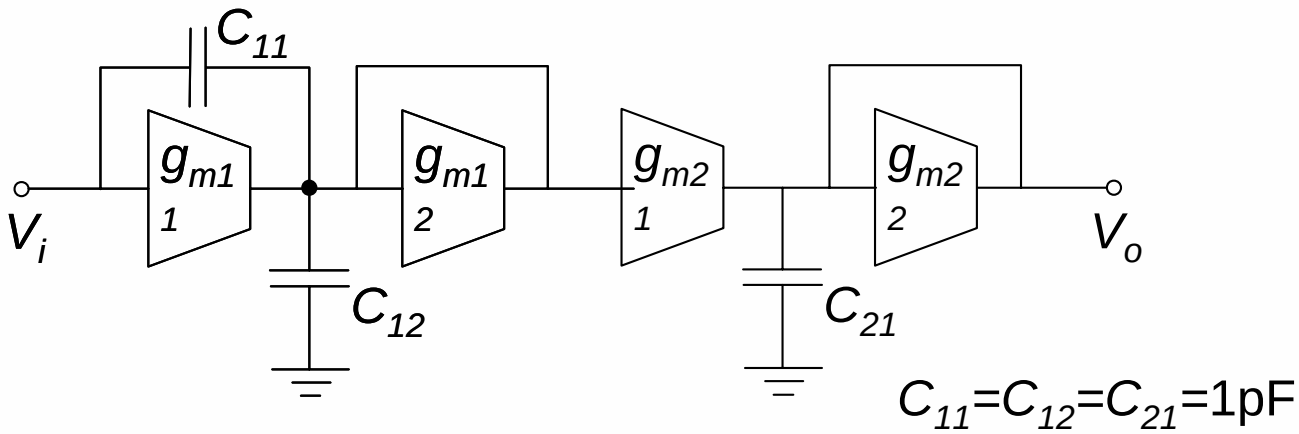
- LC filters

Advantages	Disadvantages
low noise low power high frequency	inductors are large low Q not adaptive nonstandard process

- Other types of filters are also possible. The key point is that there are ways to implement analog filters (either continuous-time or discrete-time) that can perform partial equalization and, if necessary, be adapted.

Example: Nonidealities in Gm-C Filter Design

- g_m-C filter implementation



- Nonidealities
  - Finite Bandwidth in the g_m cells
  - Finite output resistance in the g_m cells
  - Errors in the magnitudes of the g_m's
  - Nonlinearity in the g_m's
  - Parasitic capacitance

Effects of Non-ideal Factors (I)

- Effect of g_m-cell bandwidth

BW (MHz)	100	200	**300**	500	900
SNR(dB)	18.77	18.63	18.61	18.57	18.53

- Effect of g_m-cell output resistance

Rout(MΩ)	0.1	0.5	**1**	5	10
SNR(dB)	18.62	18.59	18.61	18.60	18.61

- Effect of error in g_m value

Gm error	0%	5%	**10%**	15%
SNR(dB)	18.61	18.61	18.61	18.57

Effects of Non-ideal Factors (II)

- Effect of parasitic capacitance

Cp (pF)	0	0.05	**0.1**	0.2	0.4
SNR(dB)	18.71	18.67	18.61	18.41	17.81

- Effect of distortion in the g_m cell

THD (dB)	-40.23	-43.23	**-44.70**	-45.53
SNR(dB)	17.76	18.24	18.61	18.65

- Parasitic capacitance and distortion are the most important factors affecting the system performance

HFBF AFE

- Tolerable nonidealities

BW	Rout	Cp	Gm error	THD
300 MHz	1 MΩ	0.1 pF	10%	-44.41 dB

- Filter specifications:
  - -3dB BW: 377MHz
  - Boost: 10.55dB @ 74MHz
  - THD (1Vpp @ 10MHz): -44.41dB
  - SNR: 18.61dB (*17.46 dB is achieved with an ideal LPF AFE*)
- Receiver reductions:
  - ADC effective bits: 7 bits → 6.4 bits
  - *Or* each EC filter: 120 taps → 78 taps
  - *Or* each NC filter: 72 taps → 23 taps

Gigabit Ethernet AFE Summary

- Purpose:
  - Explore AFE design to reduce overall complexity
- Chosen AFE topology:
  - One-stage real-pole HFBF without a LPF
- Filter design:
  - Examine the effects of circuit nonidealities
- Conclusion:
  - It is feasible to implement the proposed HFBF AFE, in CMOS, and reduce the overall power and area without sacrificing performance
- We are currently implementing this AFE

10 Gbit Ethernet for copper - Comments

- A mostly-digital solution will severely tax state-of-the-art ADC capabilities
- The AFE could include significant equalization to reduce the burden on the ADC and back end DSP
  - The AFE could probably be implemented in CMOS given the frequency limitations imposed by CAT5 cables
- The AFE might also include some echo cancellation and/or NEXT cancellation
  - Echo and/or NEXT cancellation might be beneficial if significant high-frequency boost is added since the boost would also enhance these terms (echo dominates in gigabit Ethernet)

Further Comments

- One promising filter topology for 10 Gigabit Ethernet might be a continuous-time analog FIR filter
  - We built one for disk drives in 2000 [1], it had 5 taps with 6b weights and an effective "sampling" rate of 600 MS/s. It used 51 mW from 3V and was fabricated in 0.5 μm CMOS
  - We are currently working on one for an ultra-wideband receiver correlator
  - The weights can be digital or analog quantities
    - Digital weights are good for adaptation, but the multipliers are much larger and consume more power (we use MDACs)
    - Analog weights allow the use of fully analog multipliers, but then weight storage and adaptation are more difficult

[1] E. Burlingame and R. Spencer, "An analog CMOS high-speed continuous-time FIR filter," Proc. of the 26th European Solid-State Circuits Conf., Sept., 2000, pp 260-262