# ADC Jitter

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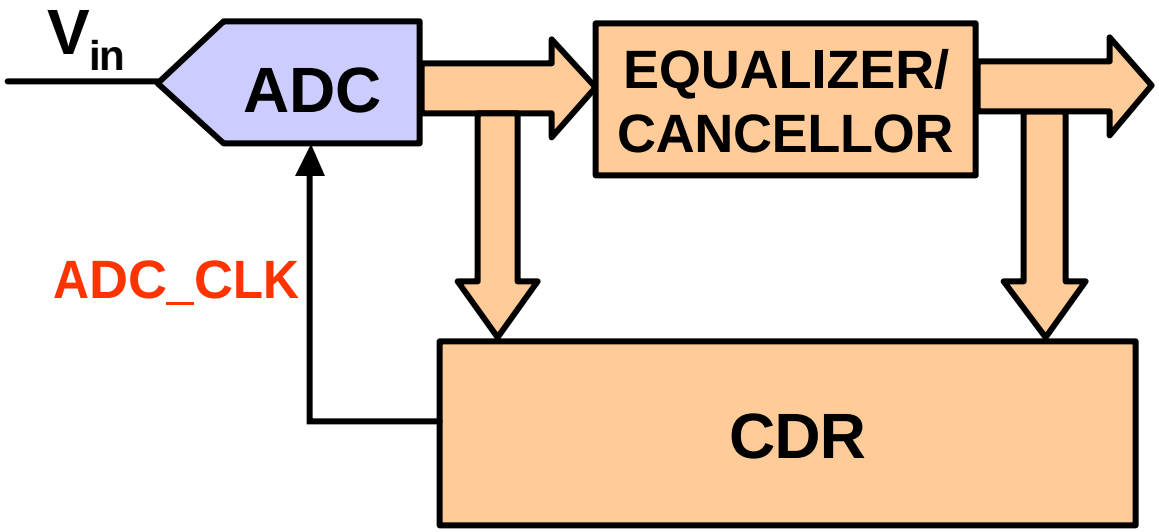
# ADC in a DSP-based Receiver

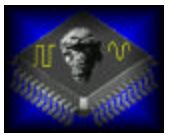


# ENOB with ADC_CLK jitter ($f_{max}$=625 MHz)

| | $J_{rms}$=0.1ps | $J_{rms}$=0.3ps | $J_{rms}$=1ps | $J_{rms}$=3ps | $J_{rms}$=10ps |
|---|---|---|---|---|---|
| n=5 | 4.99 | 4.99 | 4.96 | 4.68 | 3.56 |
| n=6 | 5.99 | 5.98 | 5.84 | 5.14 | 3.64 |
| n=7 | 6.99 | 6.94 | 6.50 | 5.33 | 3.66 |
| n=8 | 7.97 | 7.78 | 6.83 | 5.39 | 3.67 |
| n=9 | 8.89 | 8.35 | 6.95 | 5.40 | 3.67 |
| n=10 | 9.64 | 8.62 | 6.98 | 5.41 | 3.67 |
| n=11 | 10.08 | 8.70 | 6.99 | 5.41 | 3.67 |
| n=12 | 10.25 | 8.72 | 6.99 | 5.41 | 3.67 |

$$J_{rms} < 1 / (4\pi f_{max} 2^{ENOB})$$

# ADC Jitter Components



- **According to [1] ADC's total jitter can be expressed as:**

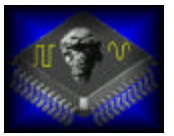
$$J_{ADC}^2 = J_{APJ}^2 + J_{CLK}^2 + J_{AIN}^2$$

**$J_{ADC}$ total ADC jitter, $J_{APJ}$ aperture jitter**

**$J_{CLK}$ clock jitter & $J_{AIN}$ analog input jitter**

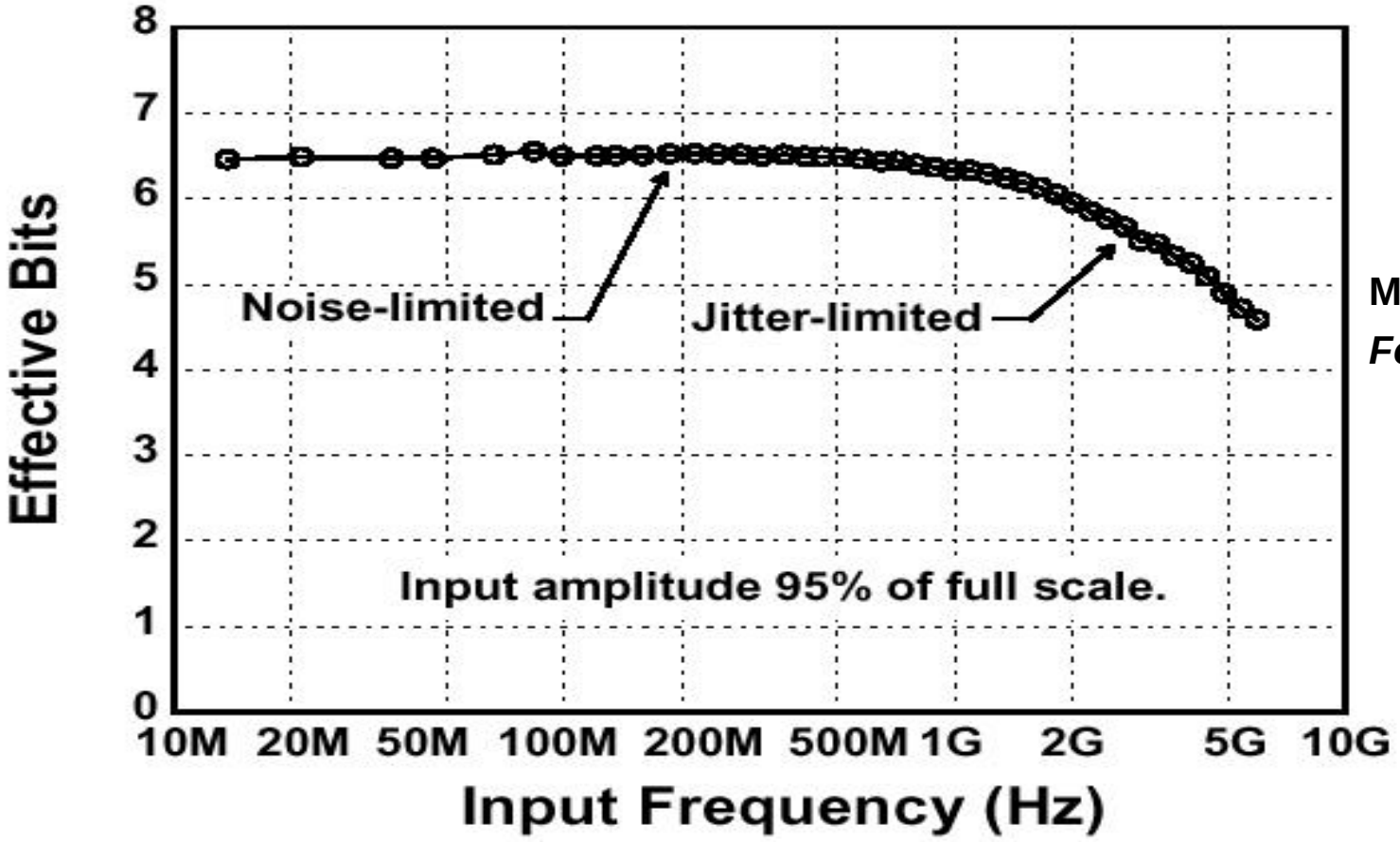
[1] M. Shinagawa *et al*, "Jitter analysis of high-speed sampling systems", *IEEE JSSC*, vol.25, pp. 220-224, Feb. 1990.

# ATMEL's TS8388 ADC Jitter



- **According to ATMEL's TS8388 ADC data-sheet (1GS/s, 8-bit & ENOB=7.1-bit), cited by Bill Jones, $J_{APJ}$=0.6 ps $J_{CLK}$=0.5 ps.**
- **Assuming $J_{AIN}$=0.5 ps then $J_{ADC}$=0.93 ps**
- **From formula ENOB=7.4-bit**
- **High-speed ADC ENOB's are jitter limited**
- **GS/s, ENOB > 6.5-bit ADCs are hard to integrate on a VLSI CMOS chip due to excess recovered clock's jitter**
- **Recovered clock period:**
  **1200 ps (PAM-10), 800 ps (PAM-5)**

# ADC ENOB vs. Input Frequency




**Measured = 0.7*ps***

***Formula = 0.44ps***

[2] K. Poulton, R. Neff, B. Setterberg, *et. al.* ,"A 20 GS/s 8b ADC with a 1MB memory in 0.18µm CMOS", *ISSCC pg. 318-319, Feb. 2003*