10 GIGABIT TRANSFORMER MODEL

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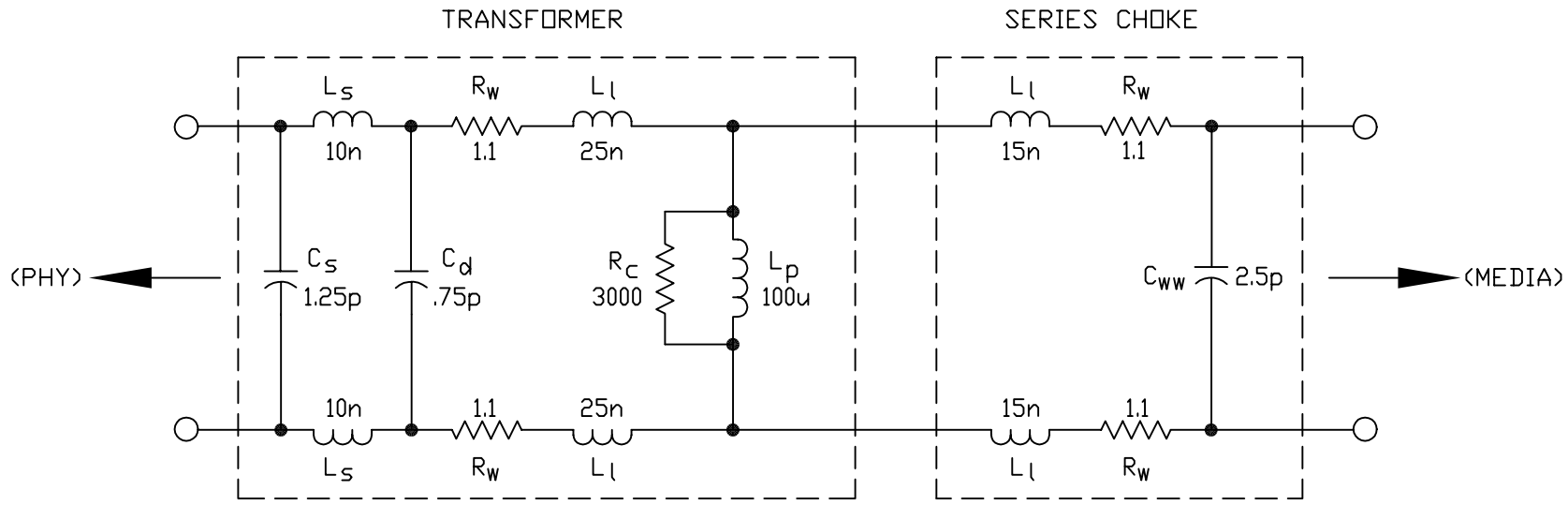
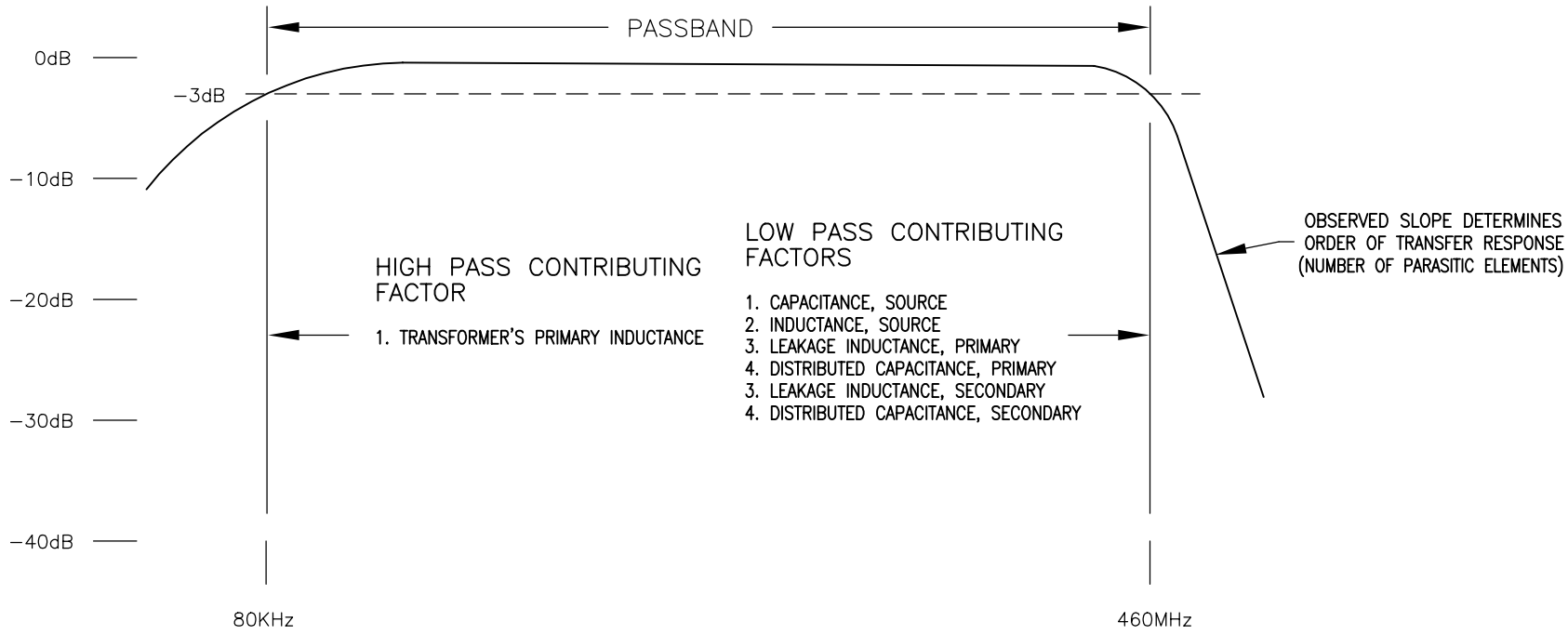


C_s = INPUT CAPACITANCE
L_s = INPUT INDUCTANCE
R_w = COIL RESISTANCE
L_l = LEAKAGE INDUCTANCE

C_d = DISTRIBUTED CAPACITANCE
C_{ww} = CAPACITANCE, WINDING-WINDING
L_p = OPEN CIRCUIT INDUCTANCE
R_c = CORE LOSS

EQUIVALENT TRANSFORMER CIRCUIT



FREQUENCY RESPONSE, TRANSFORMER

10GIG, 10 Gigabit Transformer with Series Common Mode Choke

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*   Synopsis:   The following represents what will be necessary to implement a 10 Gigabit transceiver.
*               Model has a 1:1 turns ratio and includes a series common mode choke and centertaps
*               on both the chip and media sides.

*       Date: 3/03/03           Author: H. Hinrichs

*       Filename:                       10GIG.cir

* ------------------------------------------------------------------------------------------------------------------------
*       First the S21 (Insertion Loss) model

*       Source (100 ohm differential input)

VAC1            1       0       AC      1
VAC2            0       4       AC      1

RS1             1       2       50              ; Differential impedance of source
RS2             4       5       50

*       Transformer input

LRS1            2       3       10nH            ; Wire inductance
LRS2            5       6       10nH

CS              3       6       1.25pF          ; Input capacitance

RLLP1  3        7       1.1
RLLP2  6        8       1.1

CDP1            7       8       .75pF           ; Capacitance, distributed

LLP1            7       9       25nH            ; leakage inductance
LLP2            8       10      25nH

RCORE           9       10      3000            ; Core loss

*       Ideal center-tapped transformer with 100uH primary and a 1:1 turns ratio (sets high pass pole
*       at 80 KHz)

LP_Tran1        9       30      25uH
LS_Tran1        11      40      25uH
LP_Tran2        30      10      25uH
LS_Tran2        40      12      25uH
K_Tran LP_Tran1   LS_Tran1   LP_Tran2   LS_Tran2   .99999

RLLS1  11       13      1.1
RLLS2  12       14      1.1

LLS1            13      15      15nH
LLS2            14      16      15nH

CDS             15      16      2.5pF   ; Includes capacitance of common mode choke
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*       Output load

RL1             15      0       50
RL2             16      0       50

* ------------------------------------------------------------------------------------------------------------------------------
*       Next the S11 (Return Loss) model

*       NOTE: This is actually the above model driven from the media side with the chip side source
*             terminated in 100 ohms.

VAC3            21      0       AC      1
VAC4            0       22      AC      1

RS4             21      23      50
RS5             22      24      50

*       Media side parasitics

CDSR            23      24      2.5pF

LLS1R           23      25      15nH
LLS2R           24      26      15nH
RLLS1R          25      27      1.1
RLLS2R          26      28      1.1

LS_Tran1r       27      41      25uH
LP_Tran1r       29      42      25uH
LS_Tran2r       41      28      25uH
LP_Tran2r       42      30      25uH
K_Tranr         LS_Tran1r  LP_Tran1r  LS_Tran2r  LP_Tran2r  .99999

*       Chip side parasitics

RCORER          29      30      3000

LLP1R           29      31      25nH
LLP2R           30      32      25nH

CDPAR1          31      32      .75pF

RLLP1R          31      33      1.1
RLLP2R          32      34      1.1
CDPR            33      34      1.25pF

LRS1R           33      35      10nH
LRS2R           34      36      10nH

*       Source termination

RSR1            35      36      100

.probe
.ac     dec     100     100k    1000meg

.end
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