10GBASE-T Line Signaling

Joseph N. Babanezhad

jobaba@platolabs.com

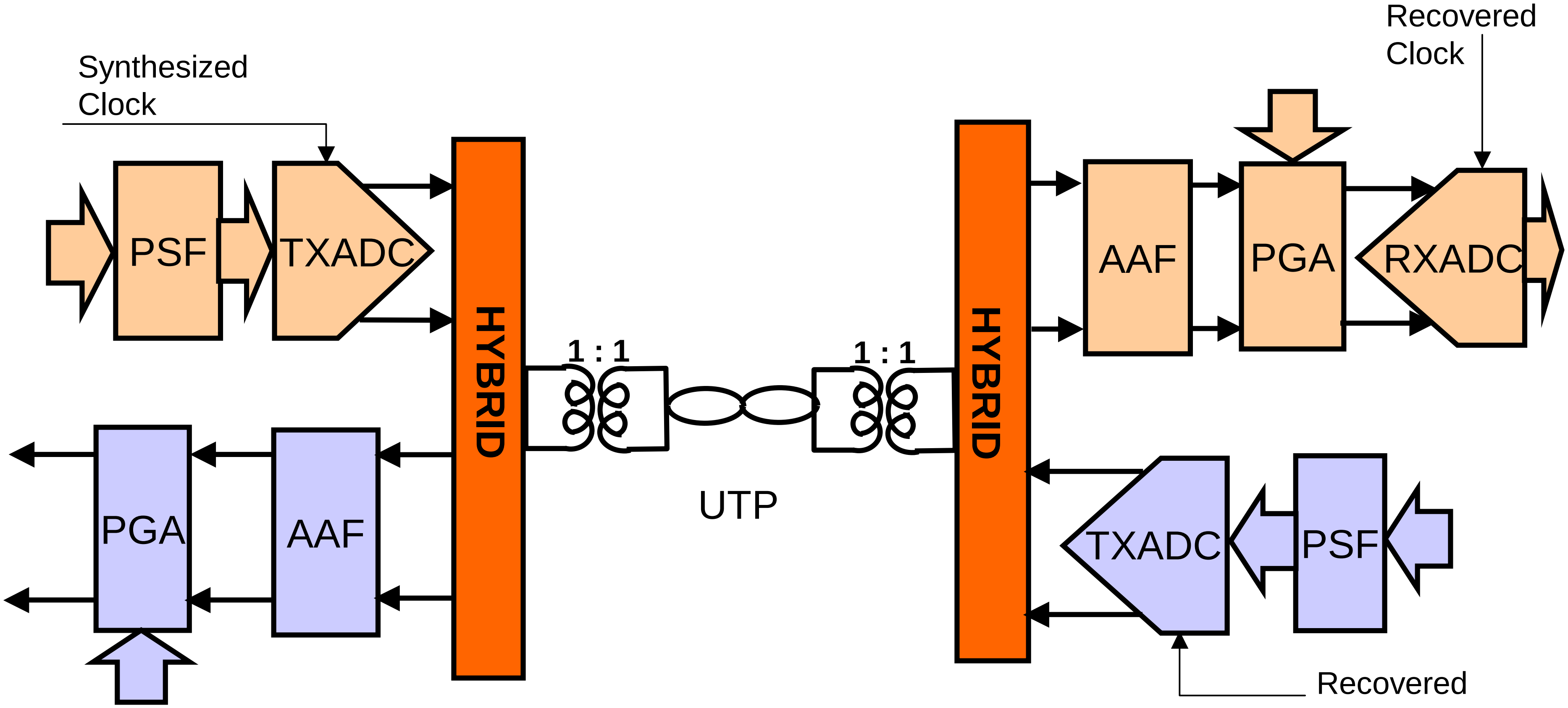
(408)-379-5115

Samir Thosani

samir@platolabs.com

Plato Labs

Analog Front End (AFE) model for DSP Solution



Assumptions for AFE Linearity Analysis

- 2 V_p peak-to-peak PAM-M launch signal
- Analog differential blocks have only odd non-linearity
- Analog blocks are characterized by:

$$Y = \beta X(1+\alpha X^2)$$

- β block gain
- α 3rd order non-linearity coefficient

Worst-case Non-linearity Error (0m)

For l (cable length)=0 cascading seven $X(1+\alpha X^2)$ blocks and retaining only 1st three terms assuming:

$$\beta_{1-to-7} = 1$$

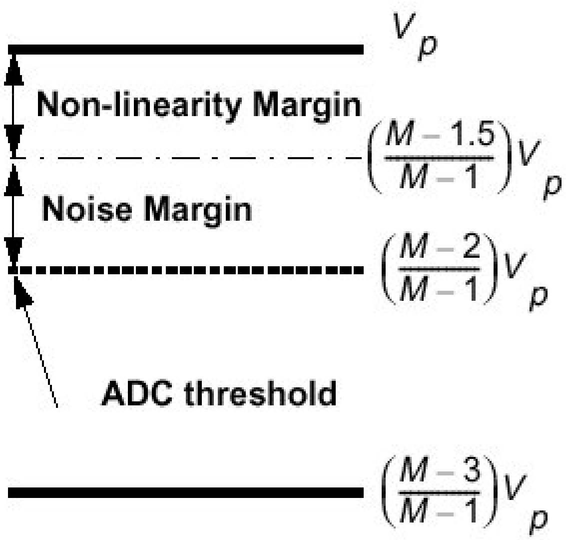
The slicer input becomes:

$$Y = X(1 + 7\alpha X^2 + 63\alpha^2 X^4) = X + error$$

The maximum error happens when α is negative and $X=V_p$, then:

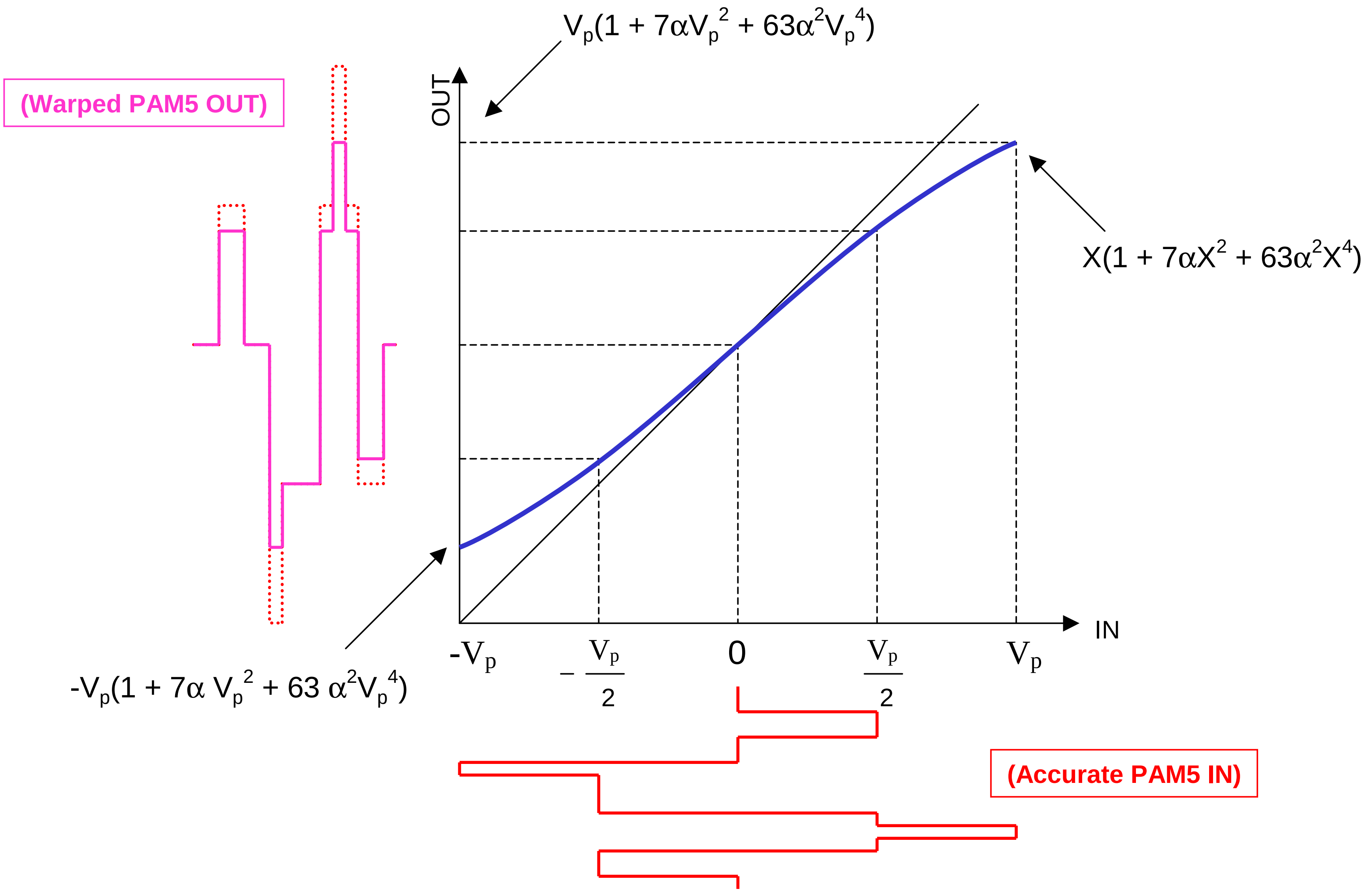
$$error \le \frac{V_p}{2(M-1)}$$

(half the ADC threshold)



$$|\alpha| \le \frac{1}{14.4(M-1)V_P^2}$$

Combined AFE Non-linearity (7 blocks)



AFE Linearity Requirement vs. Line-Signal

Line Code	Peak-to-Peak (V)	Launch Power (dBm)	|α| Formula (%)	|α| Simulation (%)
PAM-5 (Plato Labs)	**2.000**	**7.00**	**1.74**	**2.00**
PAM-10 (Solar Flare)	**3.134**	**10.00**	**0.31**	**0.35**
PAM-17 (Cicada 1/00)	**2.000**	**5.74**	**0.43**	**0.45**

Worst-case Non-linearity Error (Normalized - 0m)

For l (cable length)=0 cascading seven $X(1+\alpha X^2)$ blocks and retaining only 1st three terms assuming:

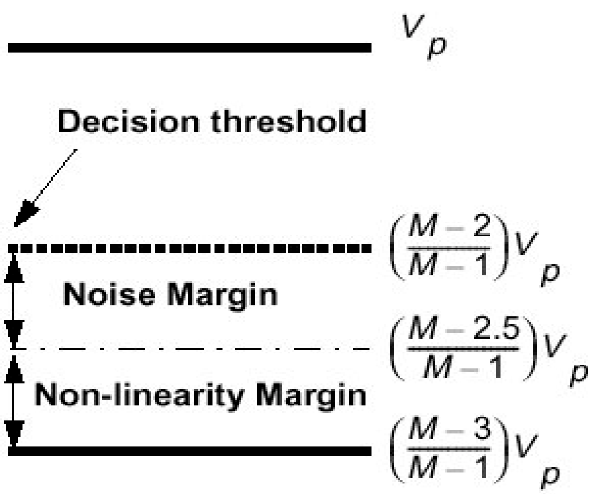
$$\beta_{1-to-6} = 1 \qquad \beta_{7(PGA)} = \frac{1}{1 + 7\alpha V_p^2 + 63\alpha^2 V_p^4}$$

The slicer input becomes:

$$Y = \frac{X(1 + 7\alpha X^2 + 63\alpha^2 X^4)}{1 + 7\alpha V_p^2 + 63\alpha^2 V_p^4}$$

The maximum error happens when

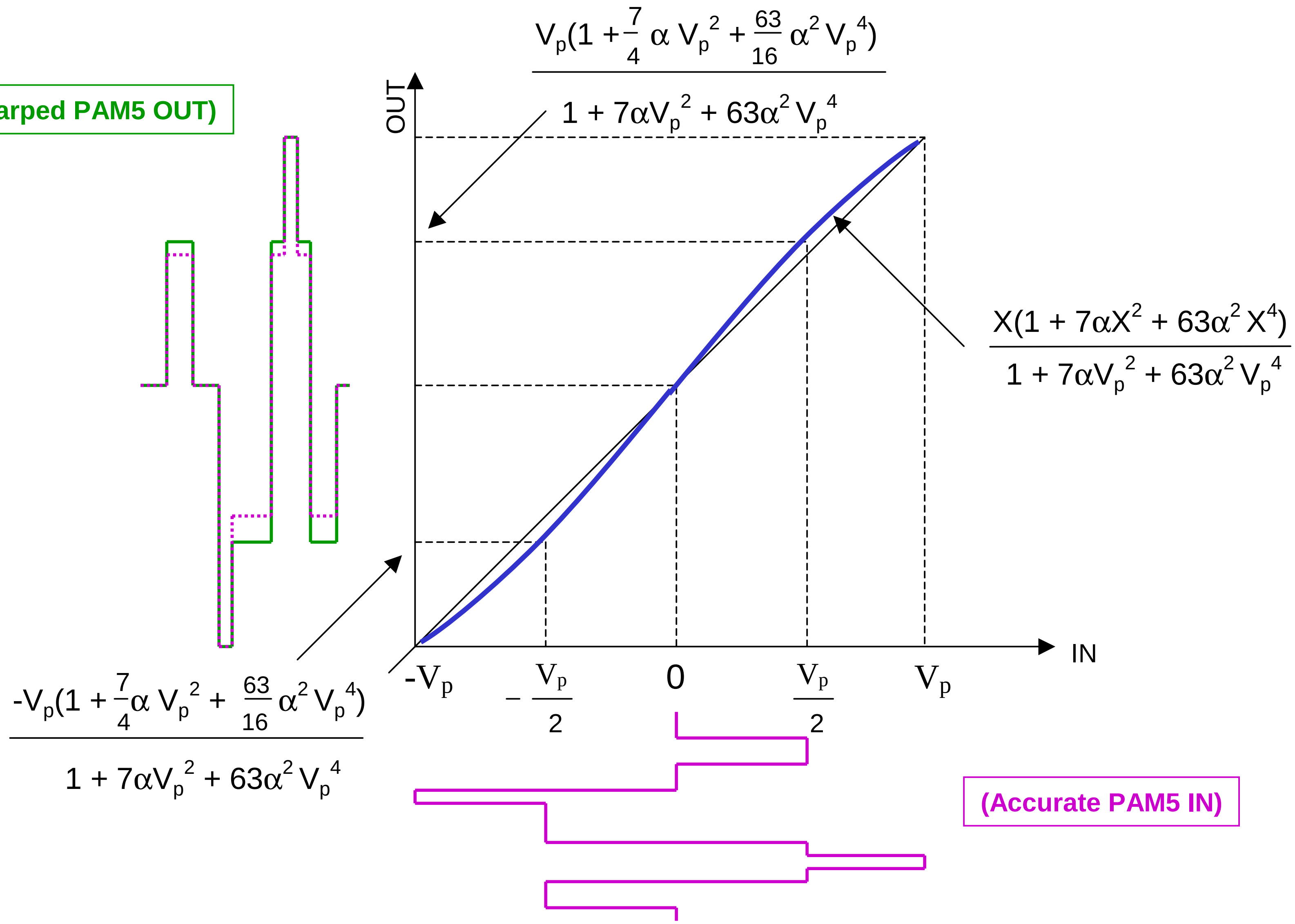
$$X = \pm\left(\frac{V_p}{\sqrt{3}}\right)\sqrt{1 + 9\alpha V_p^2}$$



$$error \le \frac{V_p}{2(M-1)}$$

$$|\alpha| \le \frac{1}{5.39(M-2.30)V_P^2}$$

Combined AFE Non-linearity (7 blocks normalized)



AFE Linearity Requirement (Normalized) vs. Line-Signal

Line Code	Peak-to-Peak (V)	Launch Power (dBm)	$\lvert\alpha\rvert$ Formula (%)	$\lvert\alpha\rvert$ Simulation (%)
PAM-5 (Plato Labs)	**2.000**	**7.00**	**7.10**	**6.00**
PAM-10 (Solar Flare)	**3.134**	**10.00**	**1.00**	**1.30**
PAM-17 (Cicada 1/00)	**2.000**	**5.74**	**1.30**	**2.75**

Class-E 4-Connector Channel Model1

$$IL = 1.9910\sqrt{f} + 0.0177f + \frac{0.2625}{\sqrt{f}}$$ **(59.4dB @ 600 MHz)**

$$PSNEXT = 20\log\left(10^{\frac{72.3-15\log f}{20}} + 2\times10^{\frac{90-20\log f}{20}}\right)$$

$$PSELFEXT = 20\log\left(10^{\frac{64.8-20\log f}{20}} + 4\times10^{\frac{80.1-20\log f}{20}}\right)$$

$$ANEXT = 60 - 10\log\left(\frac{f}{100}\right)$$

$$RL = 32 - 10\log(f)$$

$$NOISE = -150\frac{dBm}{Hz}$$

Channel Capacity 1

NEXT Cancellation (dB)	50	50	100
ECHO Cancellation (dB)	65	65	100
FEXT Cancellation (dB)	50	50	100
NOISE (dBm/Hz)	-143	-150	-150
Capacity (Gbps)	14.75	15.46	15.52

- Avaya ANEXT model: $-60+10\log_{10}\left(\frac{f}{100}\right)$
- No ANEXT Cancellation is considered

Modified Class-E 4-Connector Channel Model2

IL= Avaya Measurement (53dB @ 600 MHz)

$$PSNEXT = 20\log\left(10^{\frac{72.3-15\log f}{20}} + 2\times 10^{\frac{90-20\log f}{20}}\right)$$

$$PSELFEXT = 20\log\left(10^{\frac{64.8-20\log f}{20}} + 4\times 10^{\frac{80.1-20\log f}{20}}\right)$$

$$ANEXT = 60 - 10\log\left(\frac{f}{100}\right)$$

$$RL = 32 - 10\log(f)$$

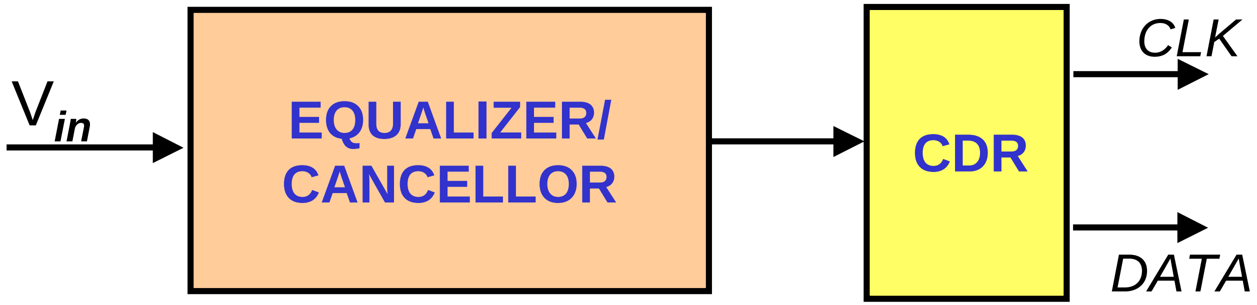
$$NOISE = -150\frac{dBm}{Hz}$$

Channel Capacity 2

NEXT Cancellation (dB)	50	50	100
ECHO Cancellation (dB)	65	65	100
FEXT Cancellation (dB)	50	50	100
NOISE (dBm/Hz)	-143	-150	-150
Capacity (Gbps)	17.77	18.52	18.59

- Avaya ANEXT model: $-60+10\log_{10}\left(\frac{f}{100}\right)$
- No ANEXT Cancellation is considered

Analog Approach



Class-E 4-Connector Channel Model3

$$IL = 1.9910\sqrt{f} + 0.0177f + \frac{0.2625}{\sqrt{f}}$$ **(59.4dB @ 600 MHz)**

$$PSNEXT = 20\log\left(10^{\frac{72.3-15\log f}{20}} + 2\times 10^{\frac{90-20\log f}{20}}\right)$$

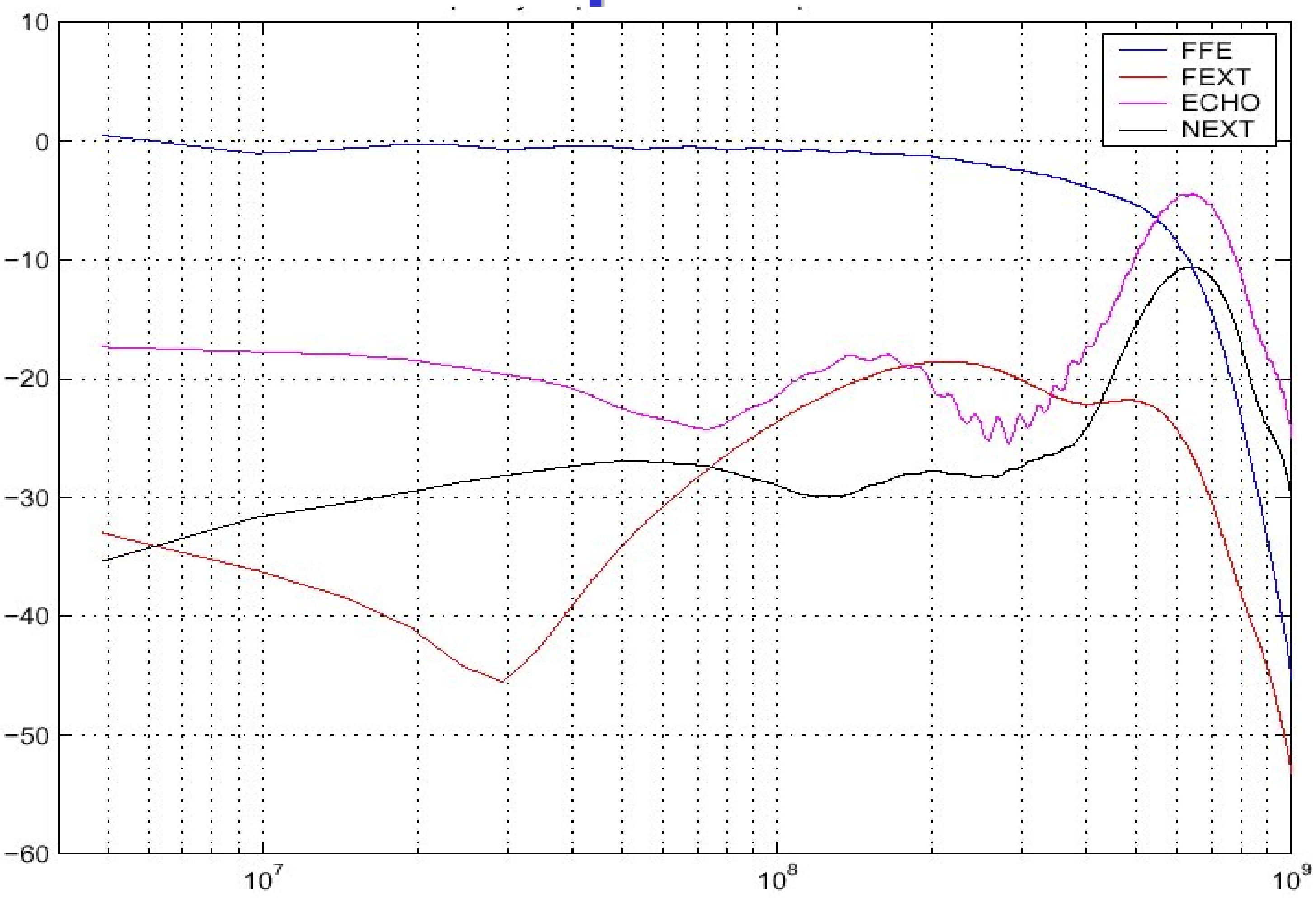
$$PSELFEXT = 20\log\left(10^{\frac{64.8-20\log f}{20}} + 4\times 10^{\frac{80.1-20\log f}{20}}\right)$$

$$ANEXT = 60 - 10\log\left(\frac{f}{100}\right)$$

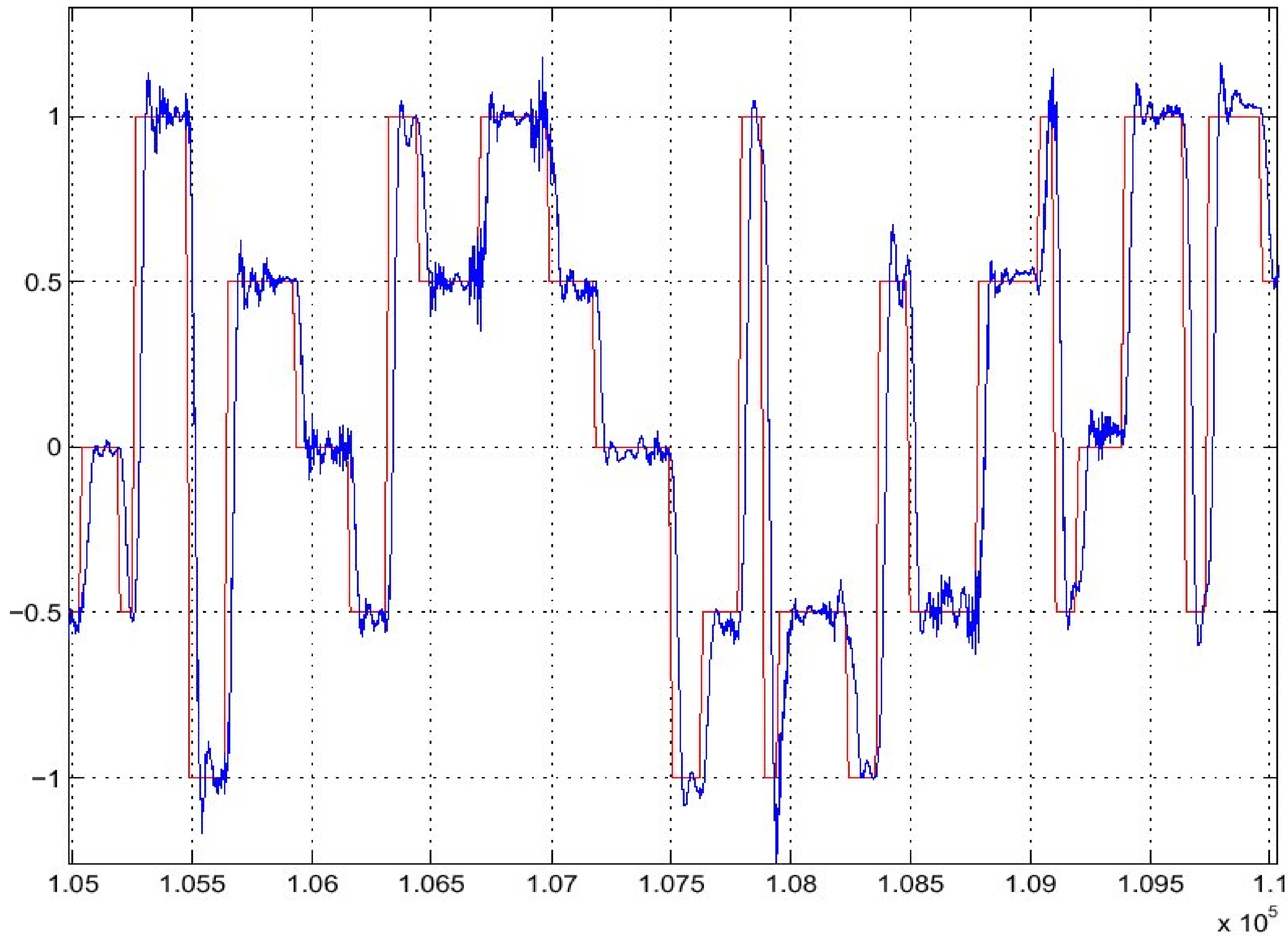
$$RL = 42 - 10\log(f)$$

$$NOISE = -150\frac{dBm}{Hz}$$

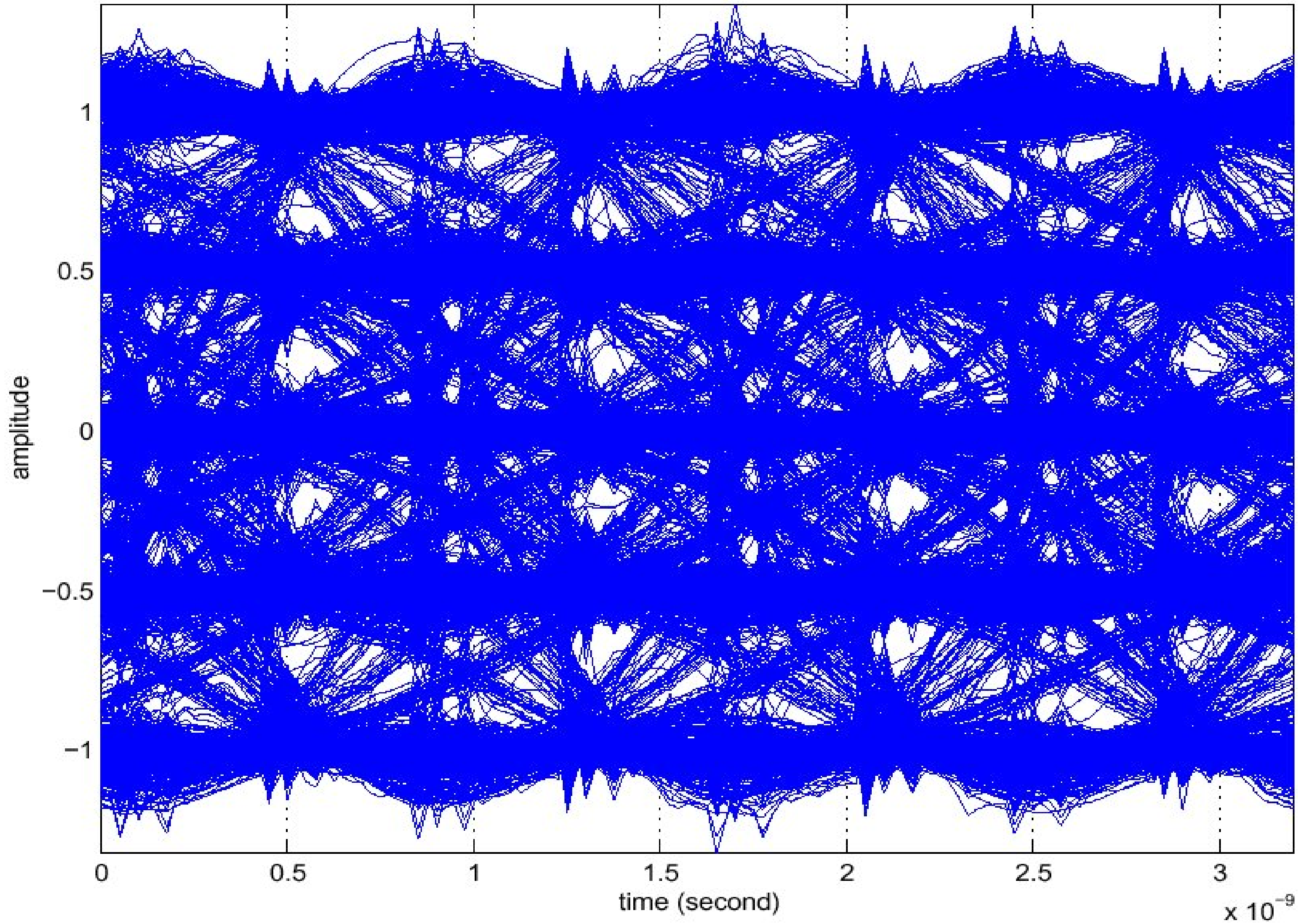
Frequency responses at Slicer Input



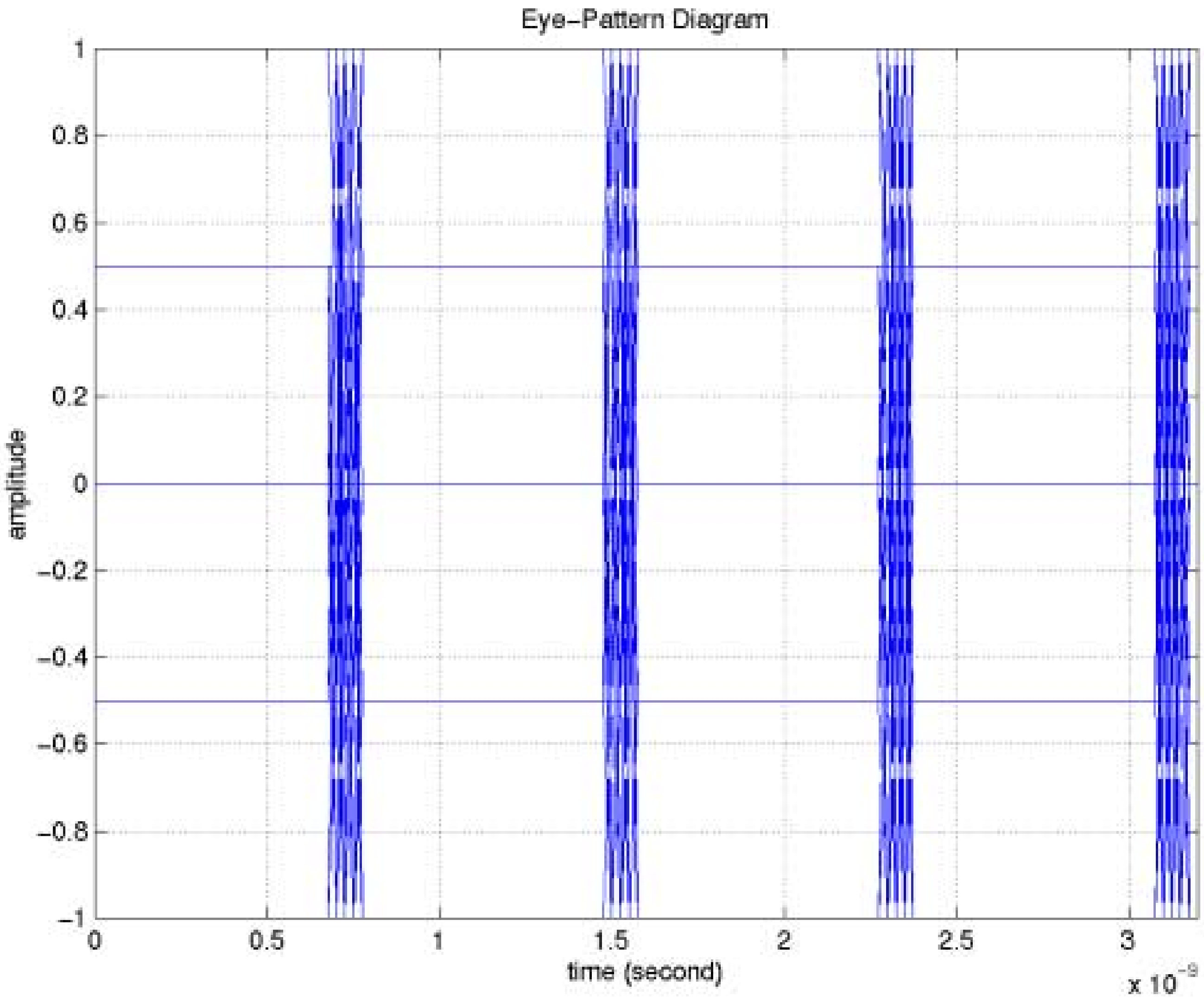
Original PAM5 and Slicer Input



Slicer Input Eye Diagram



Retimed CDR PAM5 Data Output



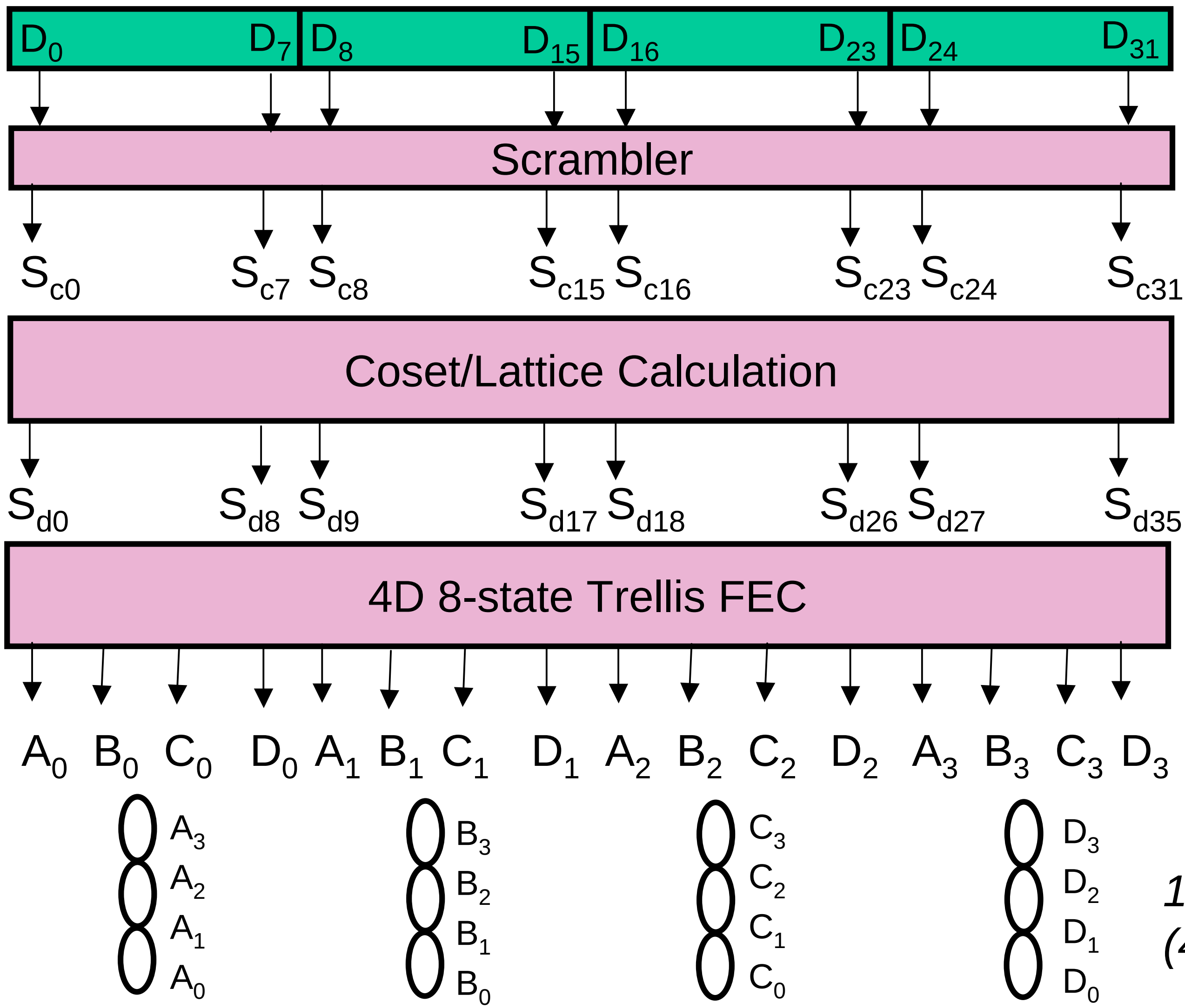
May 2003

Plato Labs

FEC

XGMII

312.5 MHz



1.25GBaud/sec
(4x312.5MHz)

Coset/Lattice Calculation

$$\begin{cases} S_{dn}(t) = S_{cn}(t) & n=0,\ldots,7 \\ S_{d8} = S_{c7}(t-1) \oplus S_{c6}(t-2) \oplus S_{d8}(t-3) & \\ S_{dn}(t) = S_{c(n-1)}(t) & n=9,\ldots,16 \\ S_{d17} = S_{c16}(t-1) \oplus S_{c15}(t-2) \oplus S_{d17}(t-3) & \\ S_{dn}(t) = S_{c(n-1)}(t) & n=18,\ldots,25 \\ S_{d26} = S_{c25}(t-1) \oplus S_{c24}(t-2) \oplus S_{d26}(t-3) & \\ S_{dn}(t) = S_{c(n-1)}(t) & n=27,\ldots,34 \\ S_{d35} = S_{c34}(t-1) \oplus S_{c33}(t-2) \oplus S_{d35}(t-3) & \end{cases}$$

Implementation Feasibility

- PHY achieves 10Gb/s over 100m Cat6
- Single-chip CMOS implementation (0.18µ)
- Power/Cost is 2-3X of 1000BASE-T
- PAM5 line-signaling
- $2V_{pp}$ launch voltage
- Interface to MAC via XGMII