10GBASE-T Objectives

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10GBASE-T Objective Proposal

- **Modify current objectives:**
  - **–to establish link distances for cabling channels**
  - **–to clarify EMC compliance**

July 2003 10GBASE-T Study Group Objectives

- Preserve the 802.3/Ethernet frame format at the MAC Client service interface
- Meet 802 Function Requirements, with the possible exception of Hamming Distance
- Preserve min. and max. frame size of current 802.3 Std.
- Support full duplex operation only
- Support star-wired local area networks using point-to-point links and structured cabling topologies
- To not support 802.3ah (EFM) OAM unidirectional operation
- Support coexistence with 802.3af
- Support Clause 28 auto-negotiation
- Support a speed of 10.000 Gb/s at the MAC/PLS service interface
- Select copper media from ISO/IEC 11801:2002, with any appropriate augmentation to be developed through work of 802.3 in conjunction with SC25/WG3
- Support 100 m over 4-connector structured 4-pair, twisted-pair copper cabling

IEEE P802.3 10GBASE-T Objectives (proposal)

- Preserve the 802.3/Ethernet frame format at the MAC Client service interface
- Meet the requirements of IEEE Std 802-2001
- Support a BER objective of 10E-12
- Preserve minimum and maximum frame size of the current 802.3 standard.
- Support full duplex operation only
- Support a speed of 10.000 Gb/s at the MAC/PLS service interface
- To not support 802.3ah (EFM) OAM unidirectional operation
- Support coexistence with 802.3af
- Support Clause 28 auto-negotiation

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- **Select copper media from ISO/IEC 11801:2002, with any appropriate augmentation to be developed through work of 802.3 in conjunction withSC25/WG3**
- **Support operation over 4-connector structured 4-pair, twisted-pair copper cabling**
- **Define a single 10 Gb/s PHY which support links of:**
  - **At least 100 m on four-pair Class F balanced copper cabling**
  - **At least 55 m to 100m on four-pair Class E balanced copper cabling**
  - **At least 45 m to 100m on four-pair Class D balanced copper cabling**
- **Meet CISPR/FCC Class A**

Supporting Slides

IEEE P802.3 10GBASE-T Objectives (proposal)

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Capacity and Margin vs. Cabling length

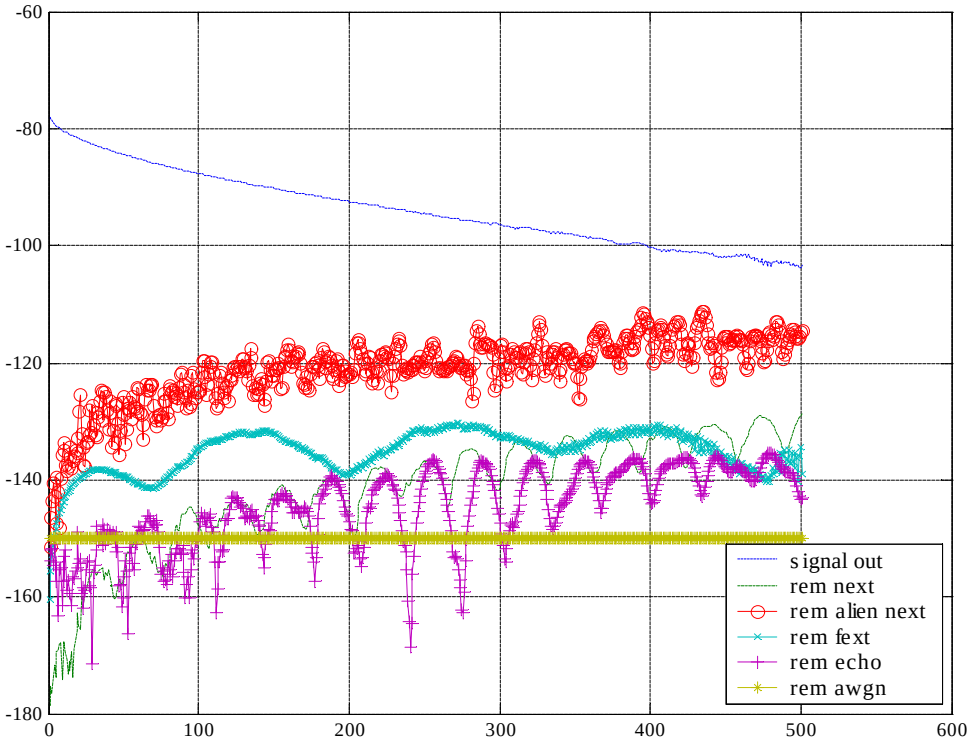
- **Model Assumptions:**
  - **Cabling AdHoc 4-connector models**
    - **IL and ELFEXT scaled for length**
  - **No ANEXT mitigation assumed**
    - **-150 dBm/Hz background noise**
    - **55 dB RL Cancellation**
    - **40 dB NEXT, 25 dB FEXT cancellation**
    - **Flat TX spectrum across bandwidth**

Capacity and Margin vs. Cabling length

- Capacity 18-20 Gbps used as metric for feasibility (roth_1_0503)
- Implementation metric:
  - PAM-10 DFE margin with example code (jones_2_0103 slide 14)
  - Detailed time-domain simulations shown for this case, including cancellation to levels shown
- Matlab code available for use with models from cabling adhoc

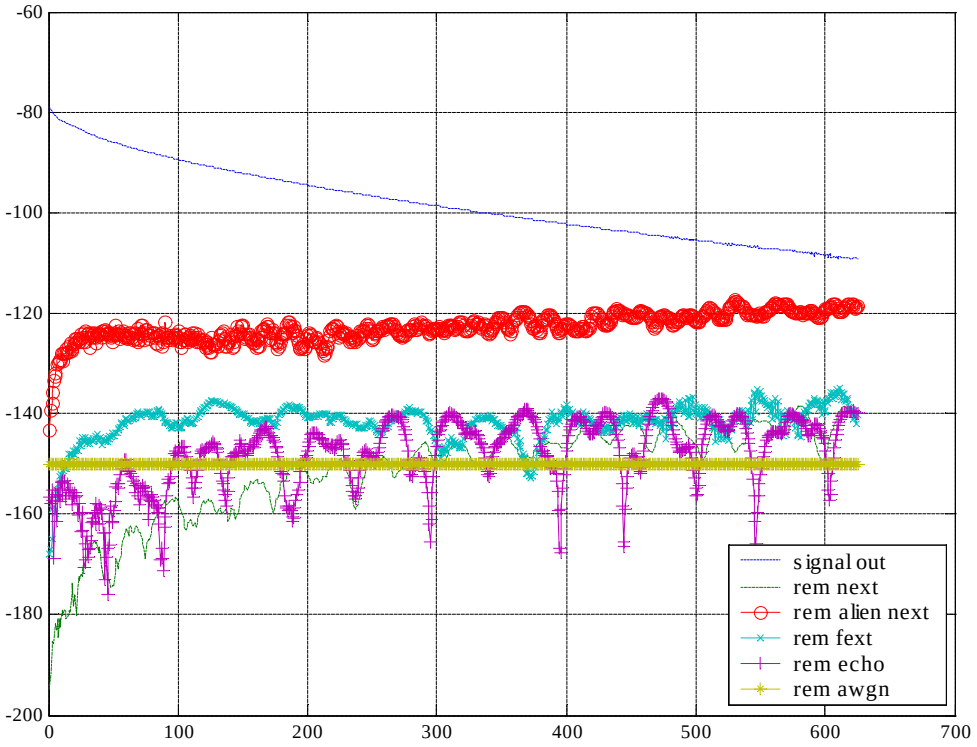
Class D/Cat 5e UTP: 45 meters Capacity & Margin

- **Capacity > 18.0 Gbps**
- **>3.8 dB PAM-10 margin at 1e-12 BER**



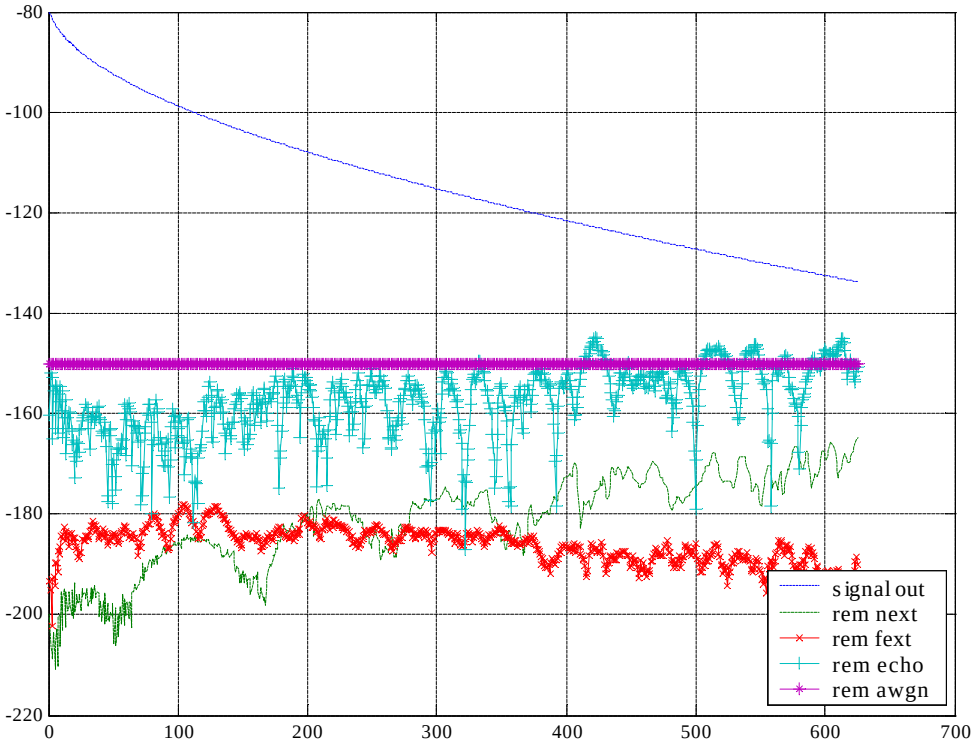
Class E/Cat6 UTP: 55 meters Capacity & Margin

- **Capacity > 19.8 Gbps**
- **>3.4 dB PAM-10 margin at 1e-12 BER**



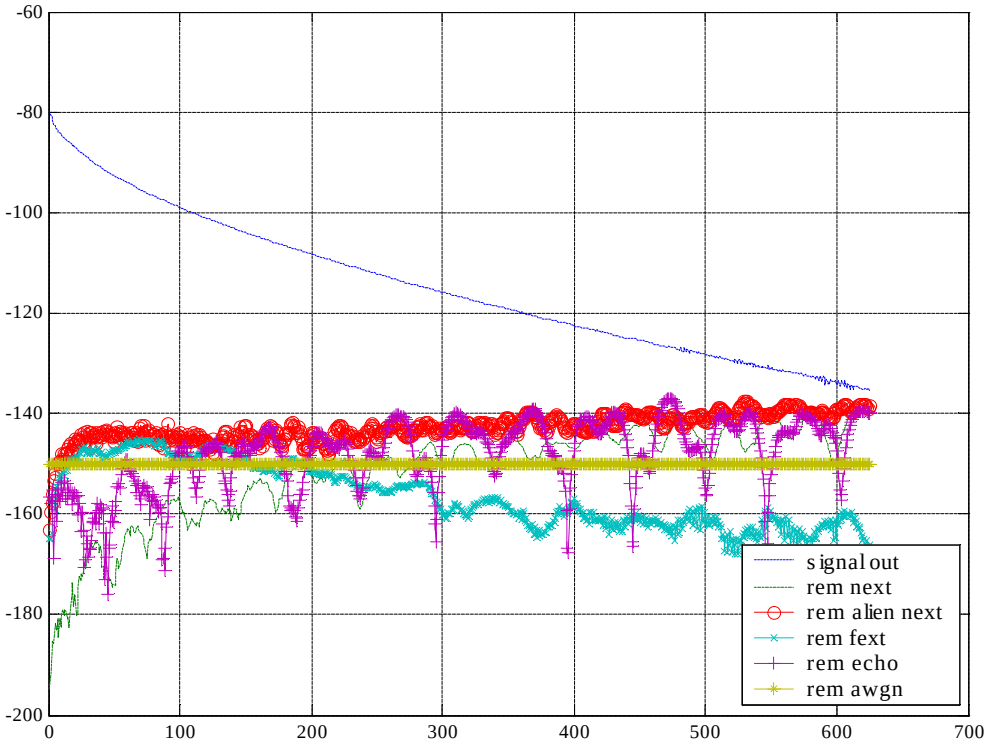
Class F/Cat7: 100 meters Capacity & Margin

- **Capacity > 28.6 Gbps**
- **> 16 dB PAM-10 margin at 1e-12 BER**



Class E/Cat6 ScTP: 100 meters Capacity & Margin

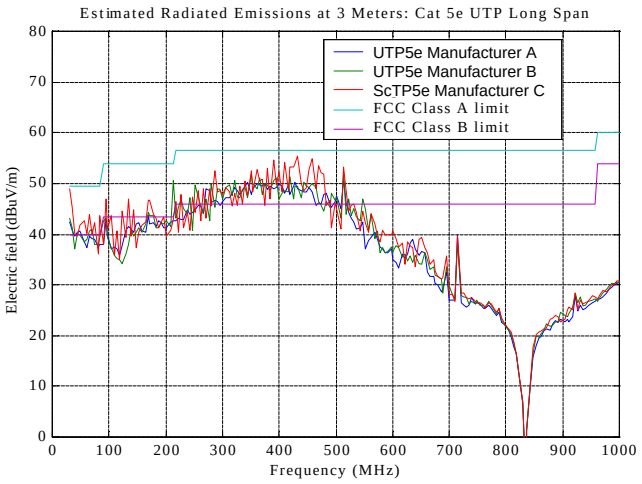
- (ref cohen_1_0703)
- Capacity > 20.6 Gbps
- >7 dB PAM-10 margin at 1e-12 BER



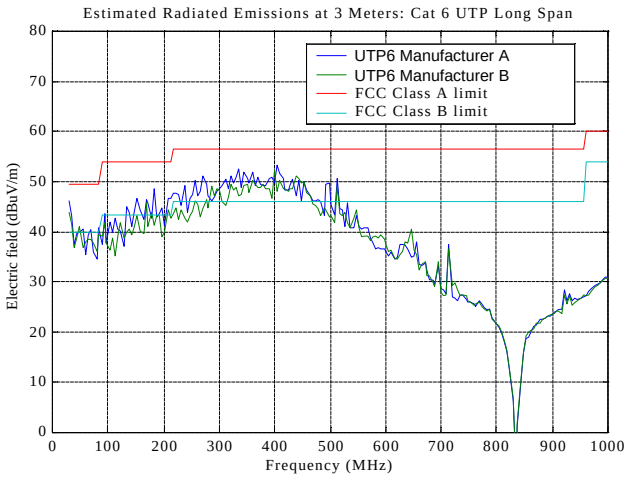
EMC Compliance:Class D/Cat5e & Class E/Cat6 Cabling

- **References: wjones_2_0103 slide 10, lcohen_1_0903**
- **Class D & E cabling systems can meet FCC class A emissions over 500MHz BW**
  - **Augmented specifications will be useful in guaranteeing this**

Class D



Class E



Estimating ADC Power Consumption

- **Extrapolating from commercial silicon, as has been done in previous presentations, yields high estimates**
  - **Sample of available technology:**

AD12400	**10.3 ENOB**	**400Msps**	**7W**
MAX108	**7.5 ENOB**	**1500Msps**	**6.5W**
TC1200	**8.0 ENOB**	**1000Msps**	**5.5W**

  - **Extrapolation yields (4 pair) x (5W/ADC) = 20W**
- **However, the same approach applied to 1000BASE-T:**
  - **Sample of commercial 8 bit ADC silicon:**

AD9054A	**8 bit**	**200Msps**	**640mW**
AD9480	**8 bit**	**250Msps**	**425mW**
ADC08200	**8 bit**	**200Msps**	**210mW**

  - **Yields erroneous result of (4 pair) x (425mW/ADC) = 1.7W**

Estimating ADC Power Consumption

- One example of a more efficient ADC approach
  - Time Interleaved ADC Array
- The technology has been presented within IEEE

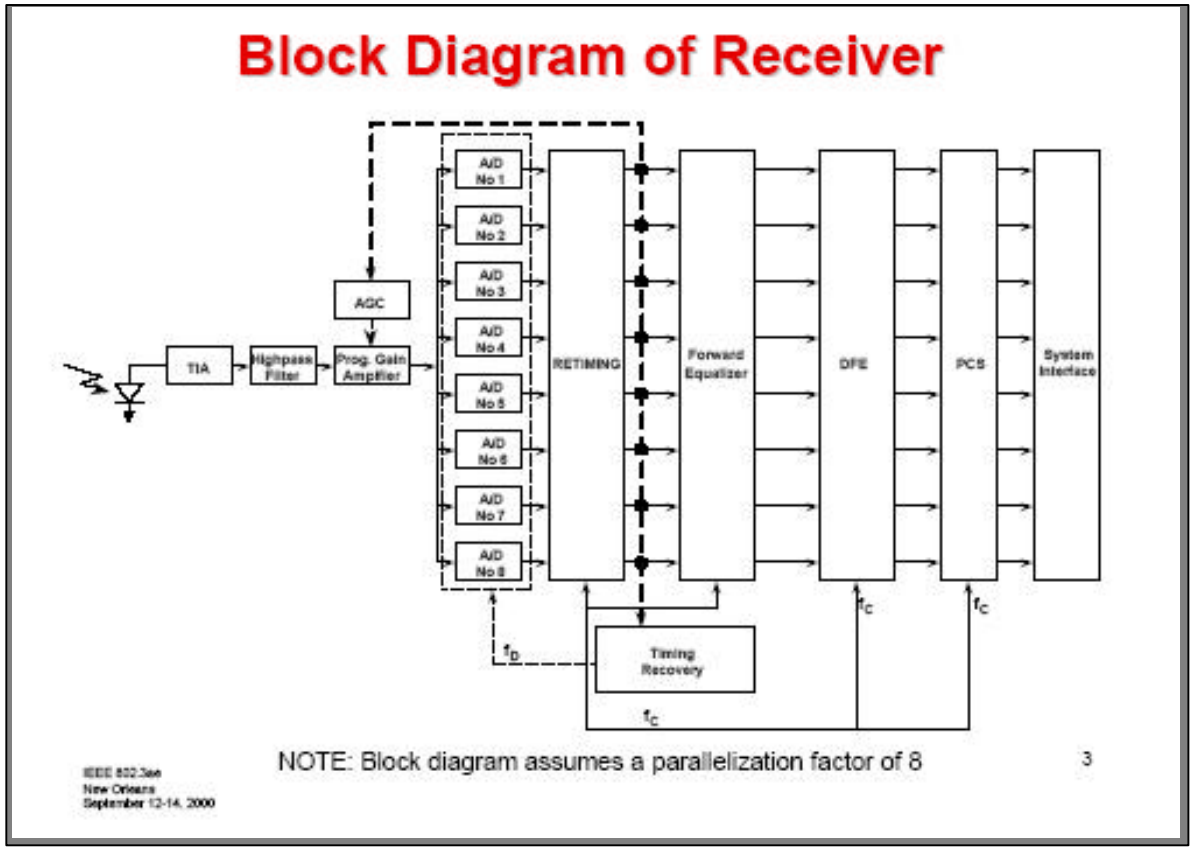
Time Interleaved Converter Arrays
Black, W.C.; Hodges, D.A.
Solid-State Circuits, IEEE Journal of, Volume: 15 Issue: 6, Dec 1980
Page(s): 1022-1029

DSP Based Equalization for Optical Channels
O Agazzi, V Gopinathan, K Parhi (Broadcom); K Kota (Cicada); A Phanse (National) September 2000, IEEE 802.3ae
http://www.ieee802.org/3/ae/public/sep00/agazzi_1_0900.pdf

A 900MS/s 6b Interleaved CMOS Flash ADC
Yu, B.; Black, W.C., Jr
Custom Integrated Circuits, 2001, IEEE Conference on, 6-9 May 2001
Page(s): 149-152

Example of Time Interleaved ADC

- **"DSP Based Equalization for Optical Channels" September 2000**



6bit
10GHz
800mvP-P
8 parallel ADCs
.18u
1.8V
450mW

Power Estimates for Time Interleaved ADC

- **Sample of available technology:**

nAD10120-13a	**10bit**	**120Msps**	**90mW**	**new**
MAX1449	**9.3 ENOB**	**105Msps**	**157mW**	**1 yr old**
AD9215-105	**10bit**	**105Msps**	**175mW**	**1 yr old**

- **Achievable ADC power *today*:**

  (8 ADC / pair) x (90mW / ADC) x 4 pairs < 2.88W

- **Process advances should improve this to < 1.5W by 2005**

Power Consumption & Complexity

- Based on an existing detailed design, we estimate:
  - 1.5 TOPs computation (1.5X Quad 1000BASE-T)
  - 6M Gates DSP
  - PAM-10 computation
  - Cancellation per simulations
  - Analog components & A/D converters in CMOS
- 90nm process mature & 65nm technology as commercial in 2006 at ASIC foundries
- Based on silicon in the lab today:
  - we estimate power for 10GBASE-T in 2006 to be <7W with 90nm technology

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