Lower complexity architectures for implementing 10GBT XTalk cancellers and equalizers FIRs

Jose Tellado
jtellado@teranetics.com
Sanjay Kasturia
sanjay@teranetics.com

Teranetics Inc.

IEEE 802.3 10G Base-T
Interim Meeting
Portonovo, Italy
Sept, 2003

Overview

Teranetics

- Background
- Lower complexity alternatives
- DFT FIR implementation

Background

Teranetics

- The bulk of the 1G and 10G computation is in the Finite Impulse Response (FIR) filters:
  - Echo cancellers (4), NEXT cancellers (12), FEXT cancellers (12) and Equalizers (4)
- For a direct form implementation of an FIR, the number of operations is proportional to:
  - The update rate (i.e. sampling rate)
  - Number of coefficients (i.e. time span)
- The complexity of the direct form implementation is roughly proportional to the square of the sampling rate
- For long FIRs, there are lower complexity alternatives

Lower Complexity FIR Alternatives

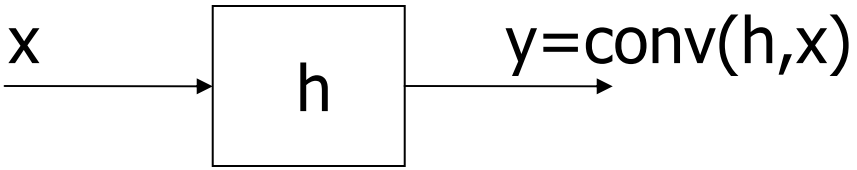
Teranetics

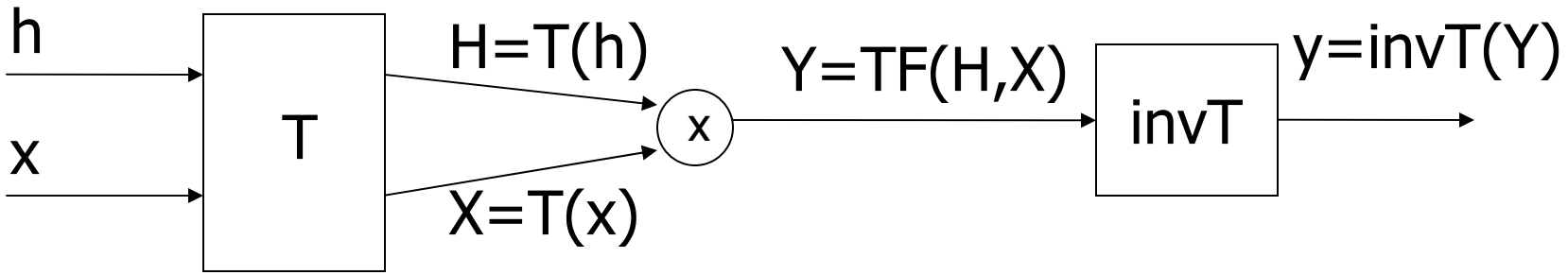
- Autoregressive Moving Average (ARMA) models of FIRs
  - Replace FIR with more compact FIR/IIR model
  - See e.g. "Stable Pole-Zero Modeling of Long FIR Filters with Application to MMSE-DFE", N. Al-Dhahir, A. Sayed and J. Cioffi, IEEE Trans on Comm, pp 508-513, May 97
- Multi-rate filters
  - See e.g. "Multirate Systems and Filter Banks", P.P. Vaidyanathan
- Domain transformation
  - E.g. DFT

FIR implementation in DFT domain

Teranetics

- E.g. Discrete-Time Signal Processing (2nd Ed.), A.V. Oppenheim, R.W. Schafer
- FIR Filtering can be implemented in the DFT domain with DFT multiplication
  - Initialization: DFT of FIR coefficients, H=T(h)
  - DFT of data block, X=T(x)
  - Multiplication of DFT data and DFT of FIR, Y=H*X
  - IDFT of product, invT(Y)
- Overlap-and-add or Overlap-and-save are used to correct for edge effects





FIR lengths for 1G and 10G

Teranetics

- The FIR lengths below are from a survey of tutorials, white papers and data sheets from 802.3 participants, PHY vendors, etc.
- The estimates for 10G are based on choosing the average reported 1G FIR lengths and increasing them by the relative sampling clock increase (800MHz/125MHz)
- The sizes of the filters and the assumed sampling clock rate are illustrative and not specific recommendations that we are making

	Echo		NEXT		FEXT	FF DFE	
	min	max	min	max		min	max
1G FIR length (surveys)	40	120	20	75	N/A	10	15
10G FIR length (estimates)	500		300		100	80	

FIR savings from DFT FIR implementation

Teranetics

	ECHO	NEXT	FEXT	FF EQ	**Total FIR**
FIR length	500	300	100	80	
BlockSize or net samples	524	724	156	176	
FFTsize	1024	1024	256	256	
log2N	10	10	8	8	
Real operations/sample for FIR	**500**	**300**	**100**	**80**	**7120**
Total operations/block for DFT FIR (4*(N/2)log_2(N)*2+4*N)/2	22528	22528	4608	4608	
Real operations/sample for FFT	**43**	**31**	**30**	**26**	**1005**
Approx Savings	**91%**	**90%**	**70%**	**67%**	**86%**
Gain	**11x**	**10x**	**3x**	**3x**	**7x**

New Issues

- Block processing Latency
- Increased memory
- Increased precision

Conclusion

Teranetics

- The bulk of 1G/10G computation is FIR filters
- Direct form FIR implementation results in high complexity as many have pointed out repeatedly in the email reflector
- Alternative lower complexity solutions are available that provide Mult/ADD gains of up to 10x (i.e. 90% savings)