A Feasibility Study for 10 Gbps over Class D,E and F

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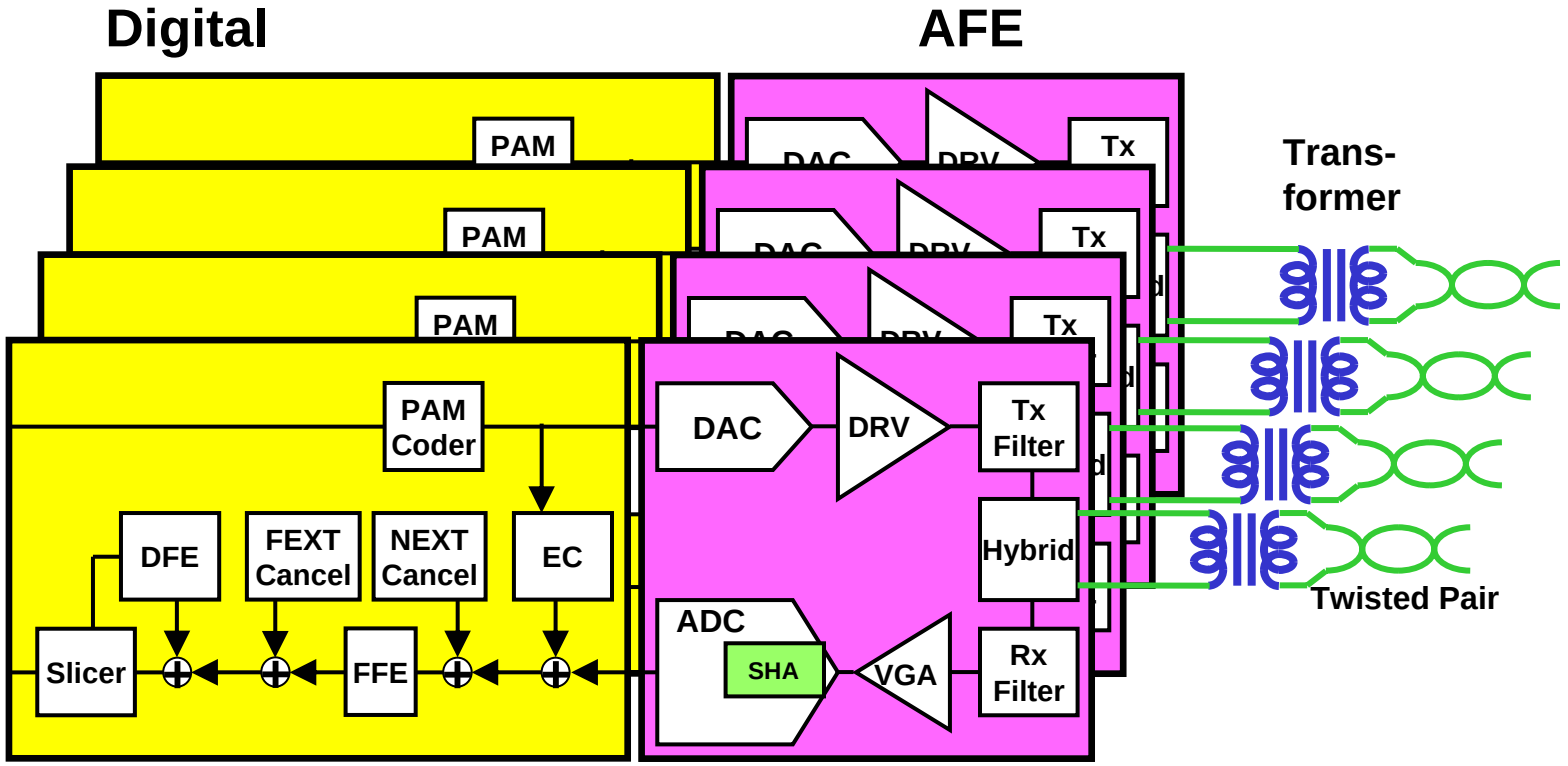
Structure of Transceiver



Receiver Parameters

Echo Cancellers:	500 taps
FFE:	60 taps
DFE:	60 taps
NEXT Canceller:	200 taps
FEXT Canceller:	30 taps

System Model

Number of PAM: ***10***

Symbol Rate: ***833Mbaud***

Tx Power: ***+10dBm, Flat PSD, 417MHz bandwidth***

BGN: ***-150dBm/Hz***

ANEXT Mitigation: ***5dB (Patch Cords, Channel Placement, etc.)***

Cable Models

- **Class D**
  - **IL, RL, NEXT, FEXT, ANEXT:** ***10GBASE-T Study Group Material***
- **Class E**
  - **IL, RL, NEXT, FEXT:** ***10GBASE-T Study Group Material***
  - **ANEXT:** ***Class D ANEXT Model - 3dB***
- **Class F**
  - **IL, RL, NEXT, FEXT:** ***10GBASE-T Study Group Material***

Note: IL,FEXT were scaled by length.

Design Concept

Target SNR:

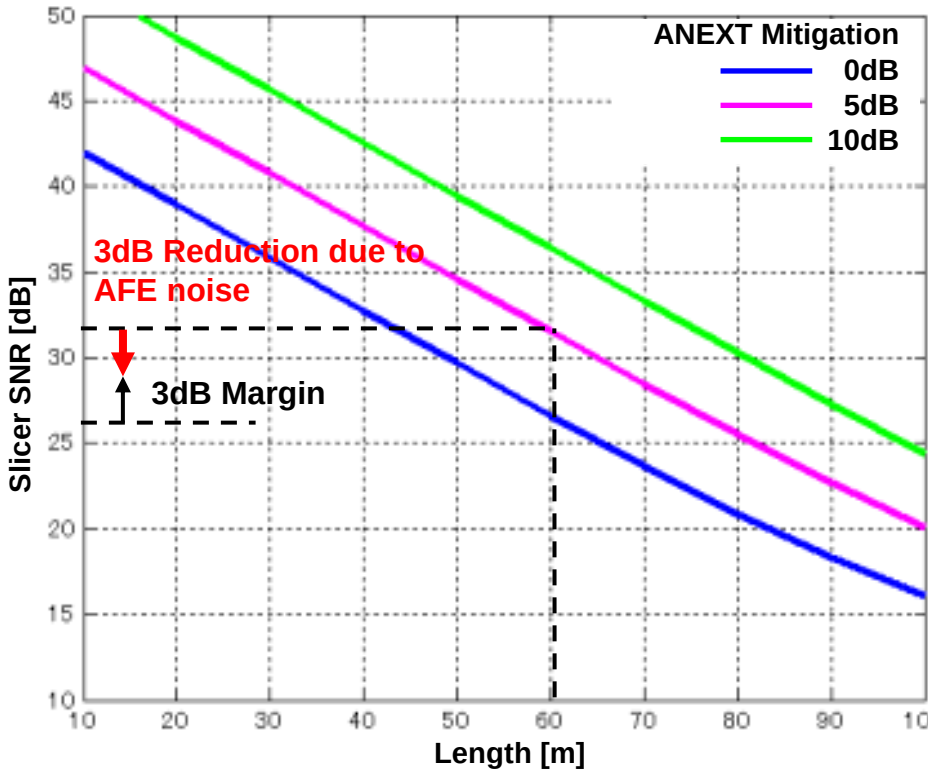
29.2 dB with ANEXT, BGN, AFE

Required SNR: 26.2 dB for 1e-12 BER
with 6dB Coding Gain
3 dB Margin for Jitter and Residual Impediments

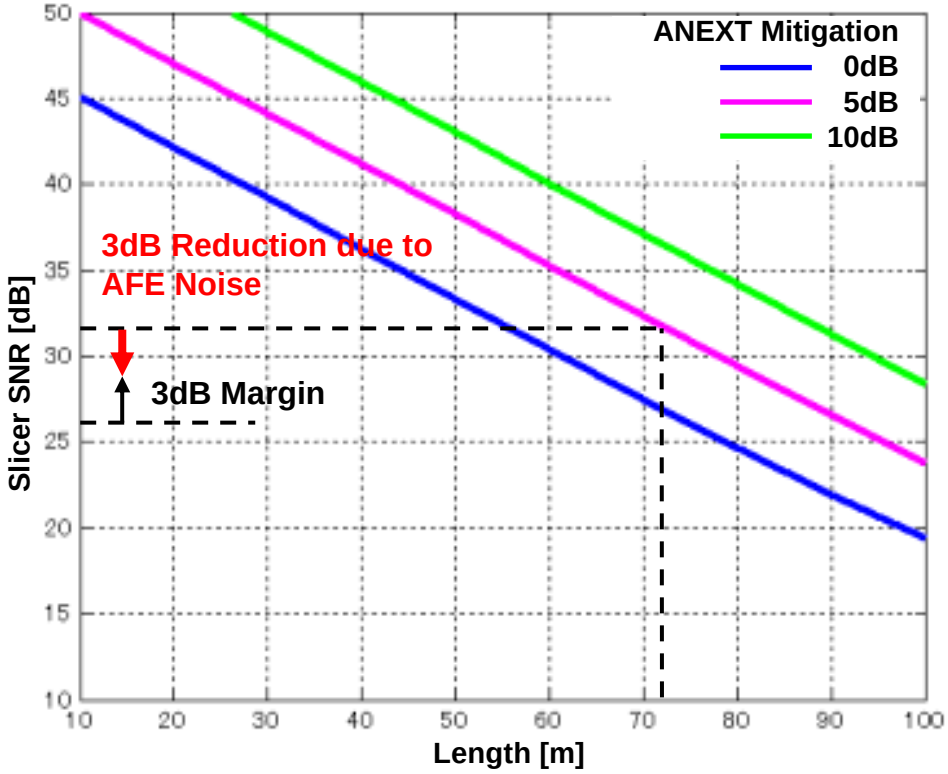
- **ANEXT is a dominate noise for Class D,E.**
- **ISI, Echo, NEXT, FEXT can be canceled up to be ignored.**

Slicer SNR for Class D, E, F

Class D -> 60m



Class E -> 70m



Class F has a large enough SNR over 100m. **(sallaway_1_0531.pdf)**

Summary of AFE Requirements

Building Block		Parameter	Values		AFE SNR	Note
			within Vrms	within Vpp*		
Transmitter		Nonlinear Distortion	-60dB		55dB	
Re-ceiver	Hybrid	Echo Suppression	20dB		Referred to VGA/ADC/Jitter Spec	
	VGA	Nonlinear Distortion	-58dB	-30dB	59dB	
	A/D	SHA nonlinear Distortion	-143dB	-29dB	144dB	Feasibility of 833MS/s ADC with 8 time interleave of 9.5bit, 100MS/s ADC.
		Quantization Noise	9.5bit ENOB		42.5dB	
	Sub-total		—		42.0dB	
Total Jitter			3ps rms		Degeneration in 1dB Slicer SNR	

*Vpp is set to be the overload of each building block.

Chip Power Estimation

Analog

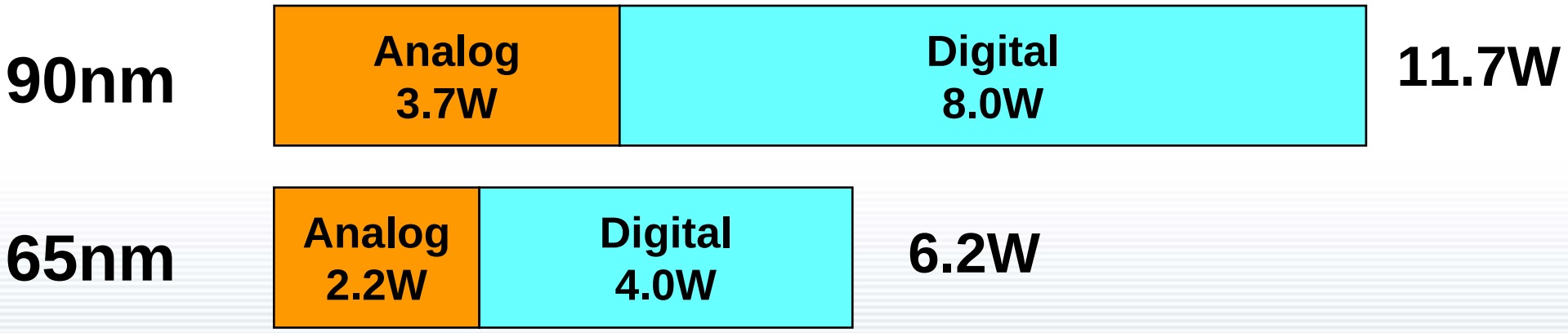
	Now Available	3 year later
ADC	2.0W*	1.0W
Driver	1.4W**	1.0W
Others	0.3W	0.2W

*9.5bit ENOB, 100MS/s ADC x8 time interleave

**With 1:1.4 transformer turns ratio, VDD=3.3V

Digital

	90nm	65nm
Gate Counts	8.5M	8.5M
Frequency	833M	833M
Power	8.0W	4.0W



Conclusion

- **With this typical transceiver structure**
  - **Class D: 60m**
  - **Class E: 70m**
  - **Class F: 100m**
- **Power Consumption**
  - **90nm: 11.7W**
  - **65nm: 6.2W**