

# **Feasibility Study for 10G Over 100m Cat 7 and <100m UTP**

**PAM-10 Solution**

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# Supporters

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- **Vivek Telang, Cicada**
- **Kok-Wui Cheong, Marvell**
- **P.J. Sallaway, Vativ**

# Topics for 10Gbps Feasibility

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- 1) ADC requirements for 100m Cat 7 cable**
- 2) Maximum cable reach on Cat 5e/6**
- 3) Power estimation**

# Assumptions for ADC and Reach Analysis

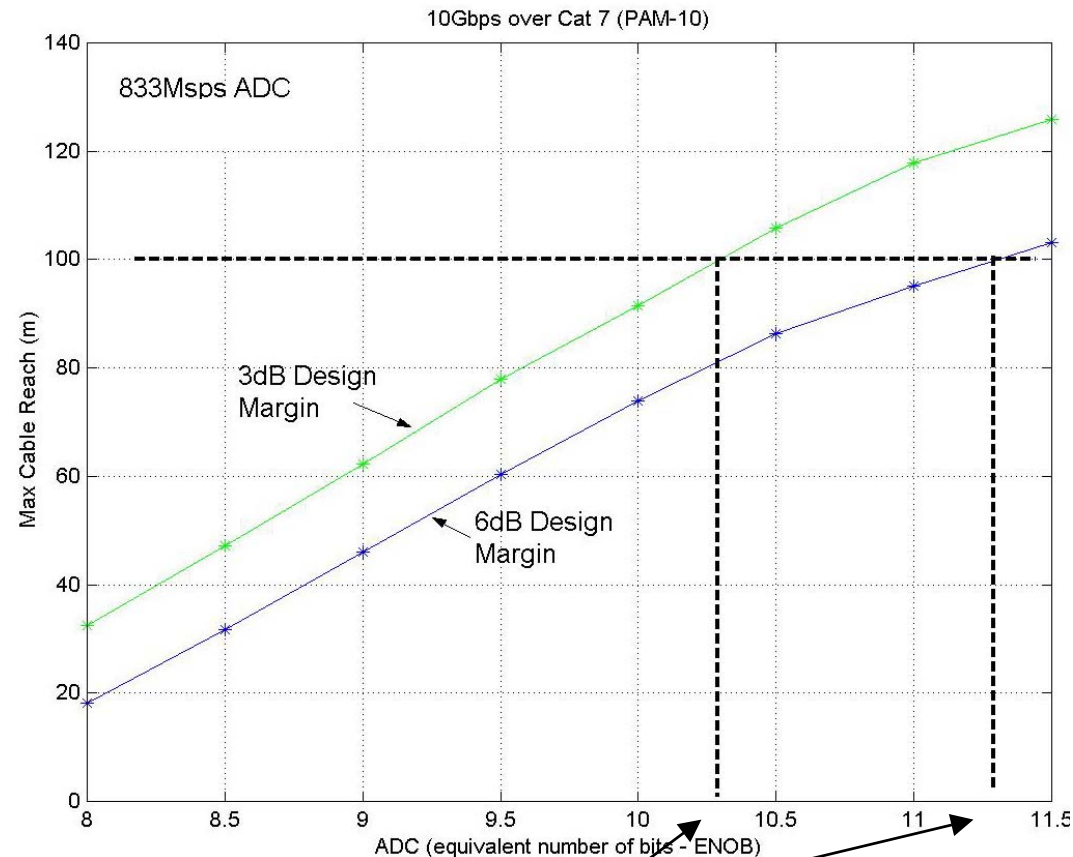
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- **PAM-10 architecture (baseline)**
  - Ideal analog hybrid echo canceller
  - Digital echo, NEXT, and FEXT cancellation (no round-off noise)
  - Digital equalization with DFSE (no round-off noise)
  - Ideal transmit and receive amplifiers (no noise or distortion)
- **Measured channel model**
  - Scaled to ISO/IEC 11801 limit lines within the specified bandwidth
  - Measured ANEXT data was not scaled - it already touches the proposed limit line
    - See May 2003 10GBASE-T presentation Sallaway\_1\_0503.pdf page 10
- **Minimum MSE solution with actual noise and cable characteristics\***
  - Best theoretical performance achievable for a given channel, given filter lengths and ADC/jitter specifications
  - Previously shown to closely match end-to-end time domain simulations

\* Standard analysis: See, for example pp521-524 in “Digital Communication” by Edward Lee and David Messerschmitt

# 10Gbps Over 100m Cat 7

- No NEXT or FEXT cancellation filters required



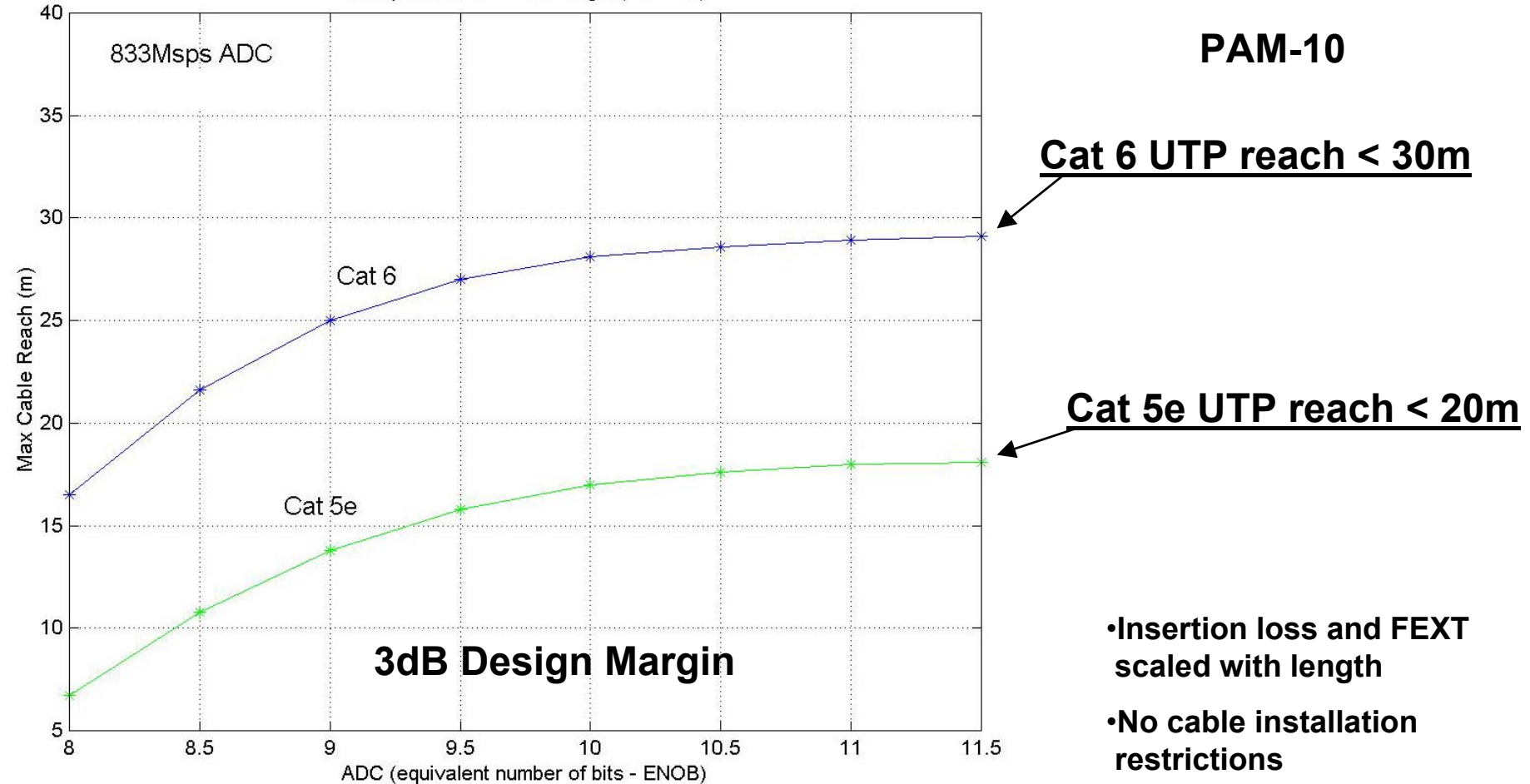
- Cable reach is limited by maximum achievable ADC ENOB at 833Mps
- Example: if ENOB=9bits is best achievable ADC at 833Mps, Cat 7 cable reach will be limited to 45-60m

- ENOB of 10.5-11.5 bits required for 10Gbps over 100m Cat7

# 10Gbps Over Reduced Length Cat 5e and Cat6 UTP

- >200 tap NEXT cancellation filters required (12x)

10Gbps with 3dB SNR Margin (PAM-10)



# Power Estimation

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- **Target rate: 10 Gbps**
- **Target media: 100m Cat 7 and 30m Cat 6**
  - 100m Cat 7 drives ADC spec and echo canceller complexity
  - 30m Cat 6 drives NEXT/FEXT canceller complexity
- **Baseline Architecture: PAM-10**
  - Cancellers and equalizer sized using MMSE analysis
- **First order power analysis based on public information and aggressive assumptions on future scaling**

# 10Gbps Over 100m Cat 7 and 30m Cat 6 UTP

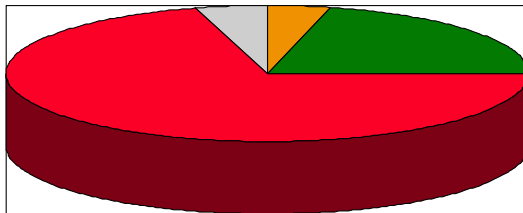
- PAM-10, Fbaud = 833.3Mpsps, Target slicer SNR = 32 dB

BER =  $10^{-11}$

Filter	# Taps
FFE+DFE	36
Echo	800
NEXT	200
FEXT	10

ADC Param.	
ENOB	10.5 bits
Bandwidth	417 MHz

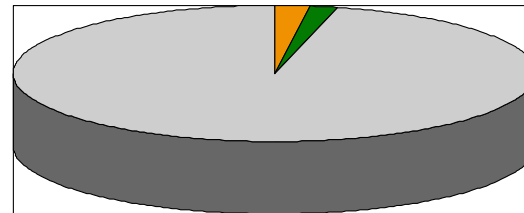
30m Cat 6



Total Slicer SNR = 27.7dB

(30.5dB @ 20meters)

100m Cat 7



Total Slicer SNR = 30.4dB



# 10G ADC Power

- **Require ENOB  $\approx$  10.5 bits at 833Msps**

- For power estimation purposes, assume alternate approach may be found to provide 1 bit relief in ENOB requirement

- **Current State of the Art:**

<u>Part</u>	<u>ENOB (bits)</u>	<u>Speed (Msps)</u>	<u>Power (W)</u>	
AD12400	10.3	400	7	← ENOB $\approx$ ok but too slow
TC1200	8	1000	5.5	←
TS83102	7.8	3000	4.6	← Speed ok but ENOB too low
MAX108	7.5	1500	8.5	←

- **Assume in 5 years that either**

- Resolution (ENOB) can increase 4x-8x with no increase in power
- Speed can increase 2x with no increase in power

- **ADC power is projected to be about  $4W \times 4 = 20W$  (4 ADC's)**

- Assume an “as-yet to be discovered” design trick can reduce this 50%

**$P_{adc_{2008}} \approx 8W$**

May be closer to 16W<sup>+</sup>

IEEE 802.3 Interim Sept 2003 10GBASE-T

# 10G DSP Power

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- **Assume echo/NEXT cancellers account for roughly  $\frac{1}{2}$  of DSP power in 1G phy**
  - Assume DSP of today's gig phy requires approx 0.25W ( $\approx 0.125$ W for echo/NEXT)
  - $(833/125) = 6.7$ x more taps running 6.7x faster  $\Rightarrow$  5.6W for echo/NEXT (0.13 $\mu$ m)
- **Assume complexity of other 1G operators (DFE etc) double for 10G**
  - Power of "other" 1G operators  $\approx 0.125$ W
  - 2x more circuitry running 6.7x faster = 1.7W (0.13 $\mu$ m)
- **Assume FEXT canceller is roughly  $\frac{1}{4}$  echo/NEXT cancellers**
  - Approx 1.5W (0.13 $\mu$ m)
- **Assume 0.13 $\mu$ m  $\rightarrow$  90nm  $\rightarrow$  65nm results in 4x power reduction**
  - $0.25(5.6+1.7+1.5) =$  total DSP power in 5 years

$$P_{dsp_{2008}} \approx 2.2W$$

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**Total 10G Transceiver Power**  
**= 10 – 18W in 5 years**

**Depends heavily on significant reduction  
in analog circuit power**

# Conclusions (PAM10)

- Cable reach limitations may not warrant support for 10G over Cat 5e/6

	<u>Cat 6 UTP</u>	<u>Cat 5e UTP</u>
Max reach	30m	20m

- Feasibility over 100m Cat 7 critically dependent on feasibility of 833Msps ADC\*

<u>100m Cat 7</u>	
ADC ENOB	>10.5* bits @ 833Msps

\* Or feasibility of alternate implementation to reduce ENOB

- Power dissipation may limit applications

10-18W\*\* per port in 5 years

\* "Cat 7-only" reduces power approx 1W/port