Framework For Upstream Synchronization and Alignment

Jeff Mandin
PMC-Sierra

Agenda

1. Design Criteria
2. Logical stack
3. Data Detector
4. Burst mode locking sequence
5. Annex: Rate Adaptation

Design Criteria – System

- ONU transmits 10101… pattern during AGC and CDR phases
- ONU transmits Barker Sequence for upstream lock
- Data elements based on 66bit width
  - consensus in Monterey
- Self-synchronous scrambler

Design Criteria – ONU Upstream PCS

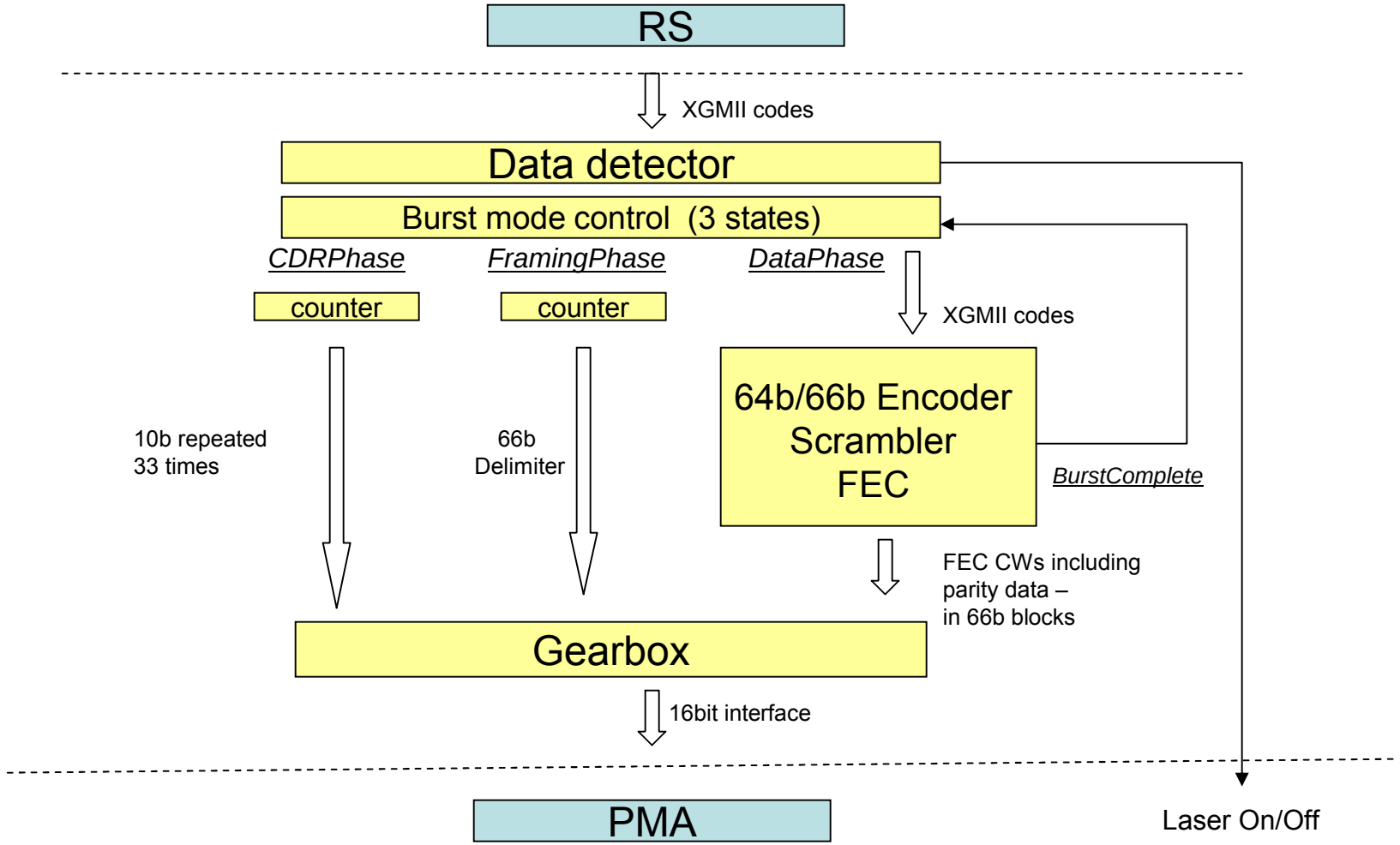
- Data phase functions (ie. Rate Adaptation, codeword build, FEC, and Scrambler) are not applicable during the time that the laser is off and during the burst initialization sequence
- Alignments and (in most cases) state machines need to be reset at the beginning of a burst
- Consequently the specification should make these functions (Rate Adaptation, codeword build, FEC, and Scrambler) inactive during laser-off and burst-init, and reset them at each upstream burst
    - Implementations can of course do things however they choose

Design Criteria – Data Detector

- Burst initialization and Laser Activation depend on XGMII codes
  - Necessary for proper initialization sequences and alignment
- Laser deactivation – in contrast - must be triggered by the transmission of the final FEC codeword
  - Once we are initialized we are working in FEC CW units

Logical Stack

Logical stack at ONU (transmit direction)



Main Elements of the Logical Stack

- *Data Detector*
  - Determines whether or not non-IDLE data is pending (as in GEPON)
- *Burst Mode Control* entity
  - Maintains the *BurstModeControlState* variable
  - Path thru the PCS depends on *BurstModeControlState (3 states -> 3 paths)*
  - Responsible for invoking “laser-on/laser-off” function in PMA
- *Counter*
  - Counts 4 XGMII codes and then sends a 66 bit word down to PMA
- *Gearbox*
  - Interworks 66bit PCS with 16bit PMA per Clause 49

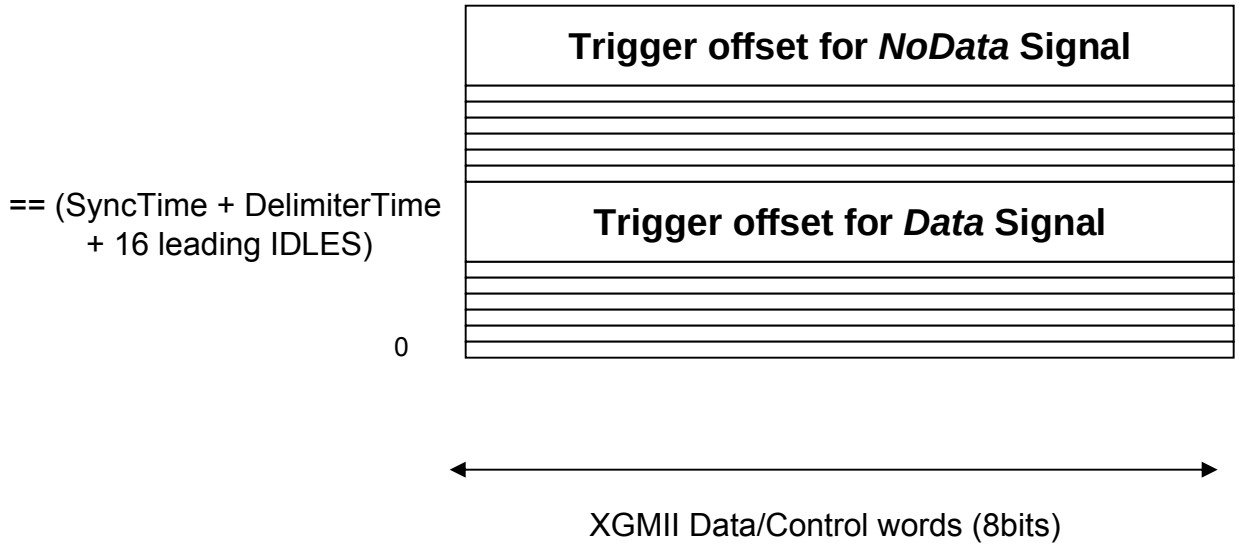
Data Detector

Data detector

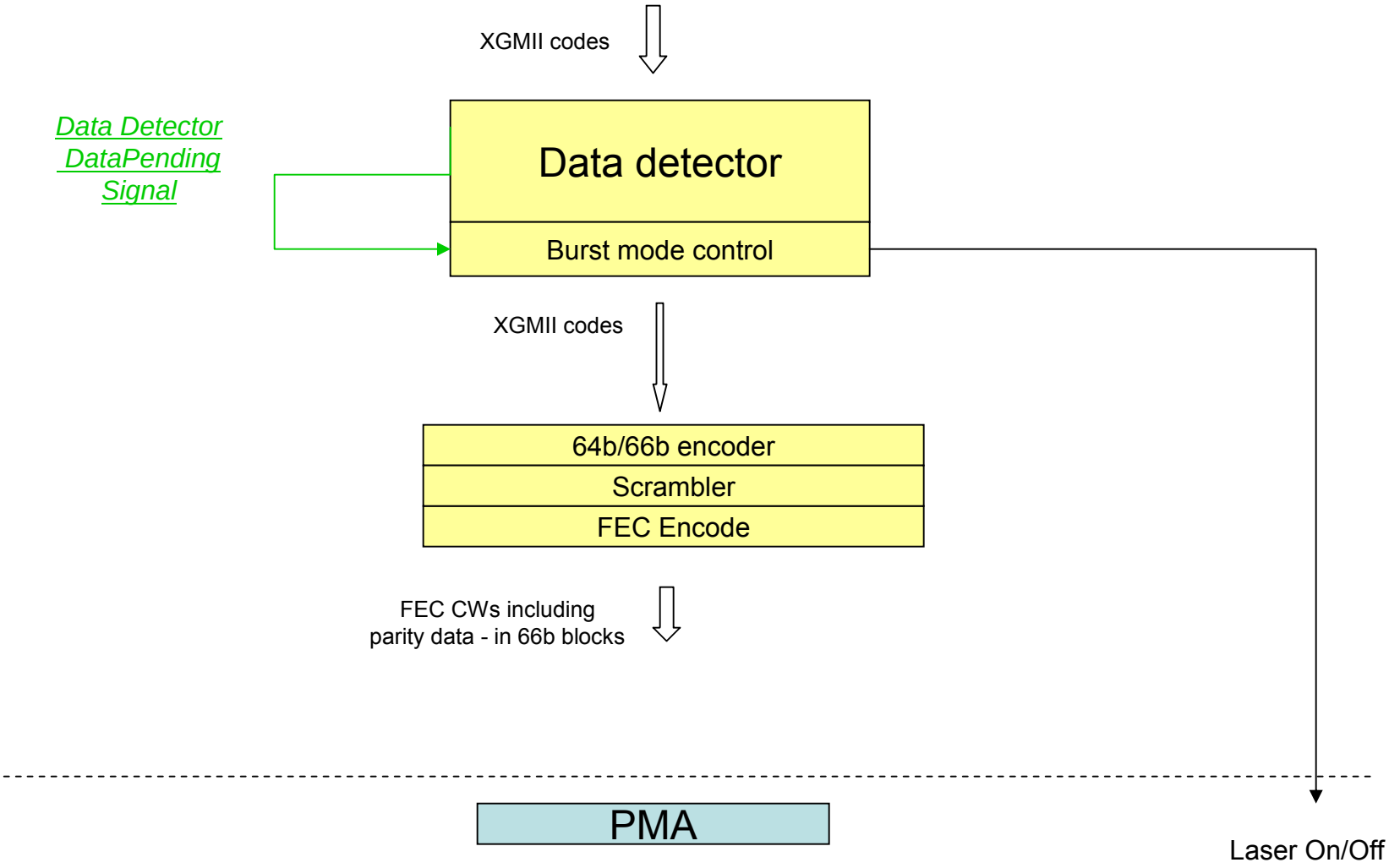
- Determines whether or not data is pending by delaying data in a FIFO and examining whether there is a non-IDLE code anywhere in the queue (ie. follows data detection model from GEPON)

- Sets logical signals that are used by Burst Mode Control entity

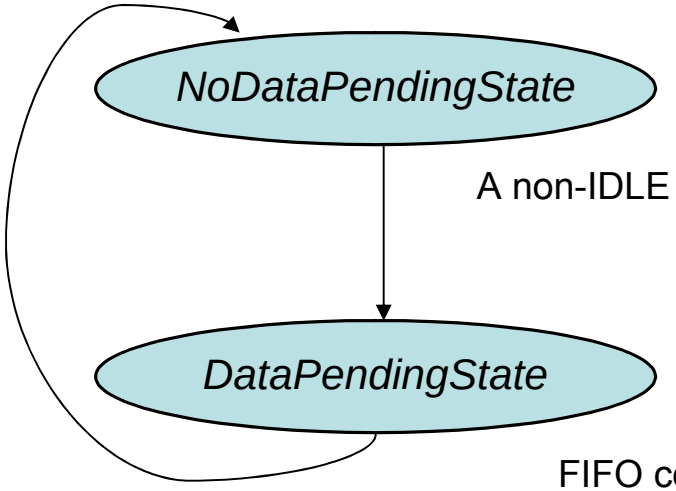
Data Detector Delay Line (FIFO)



Data detector interfaces



Data Detector State Transitions



A non-IDLE code enters the Data Trigger position of the FIFO
=> Turn on *DataPending* signal and advance to *DataPendingState*

FIFO contains only IDLE codes between NoData trigger position and the front of the FIFO
=> Turn off *DataPending* signal and return to *NoDataPendingState*

Data detector – laser on sequence

- Non-IDLE enters FIFO – causing Data Detector to raise the *DataPending* signal

- Burst Mode Control entity in *CDRPhase* state (see below) checks if *DataPending* signal is on and if so invokes PMD_Signal.Request(true)

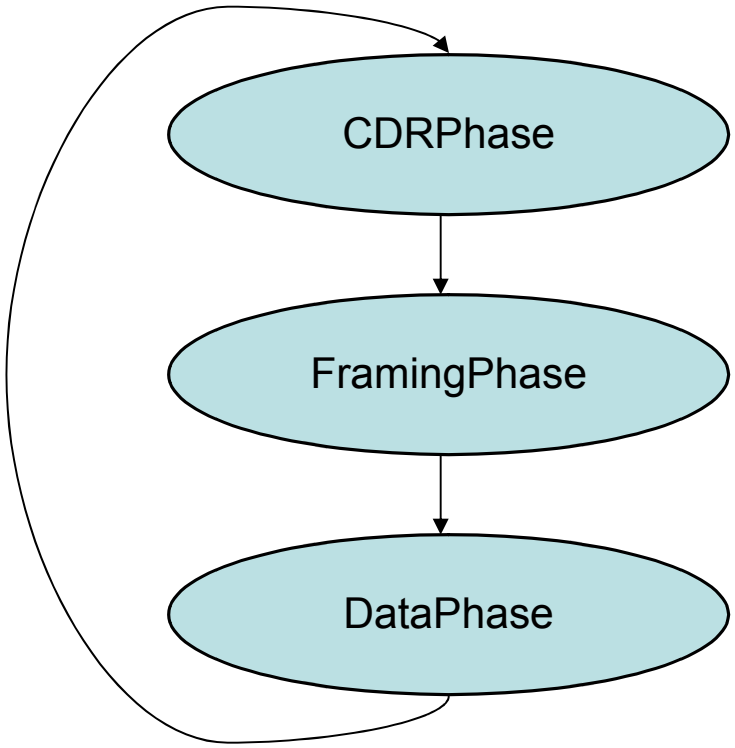
Data detector – laser off sequence

- When FIFO contains only IDLEs, Data Detector resets the *DataPending* signal

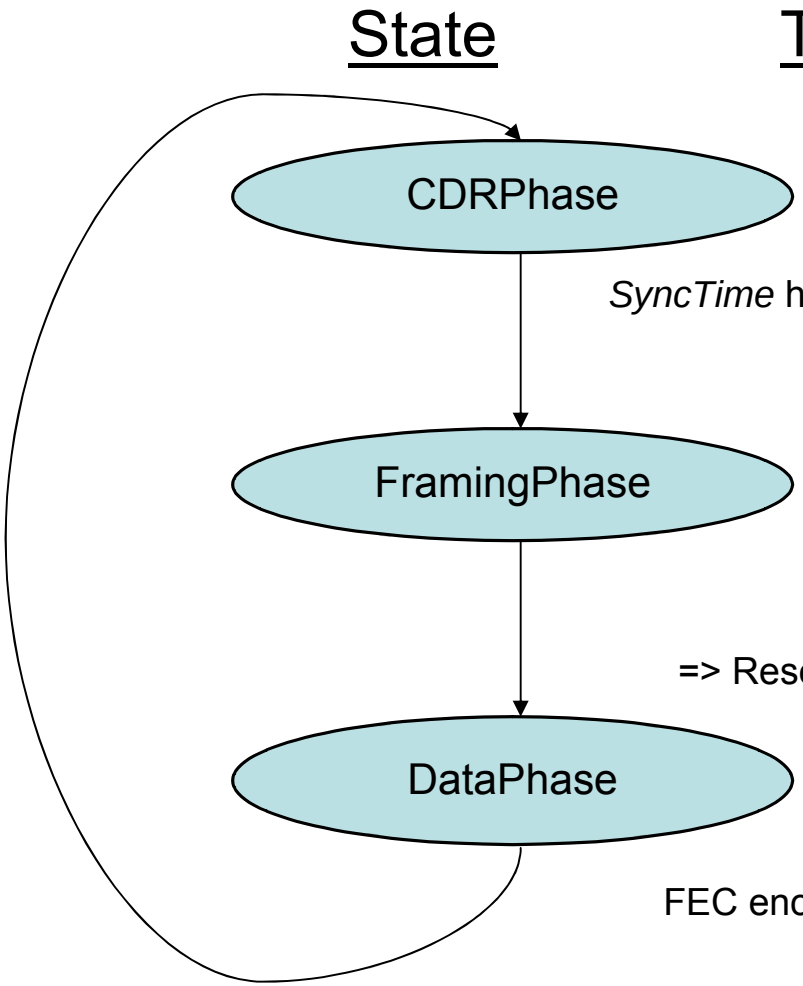
- When Burst Mode Control entity recieves *BurstComplete* signal from the FEC Encoder, it checks the *DataPending* signal and – if signal is false - invokes PMD_Signal.Request(false)

Burst Mode Locking sequence

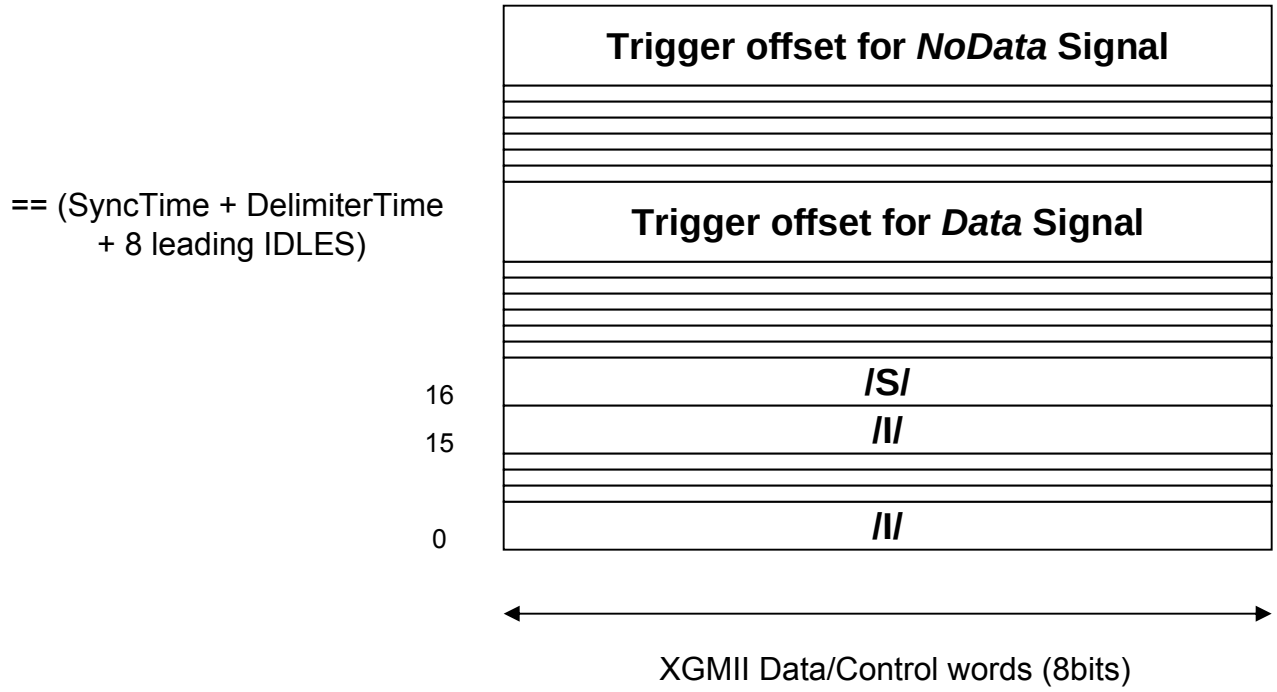
PCS operates according to Burst Mode Control State



Burst Mode Control State Transitions

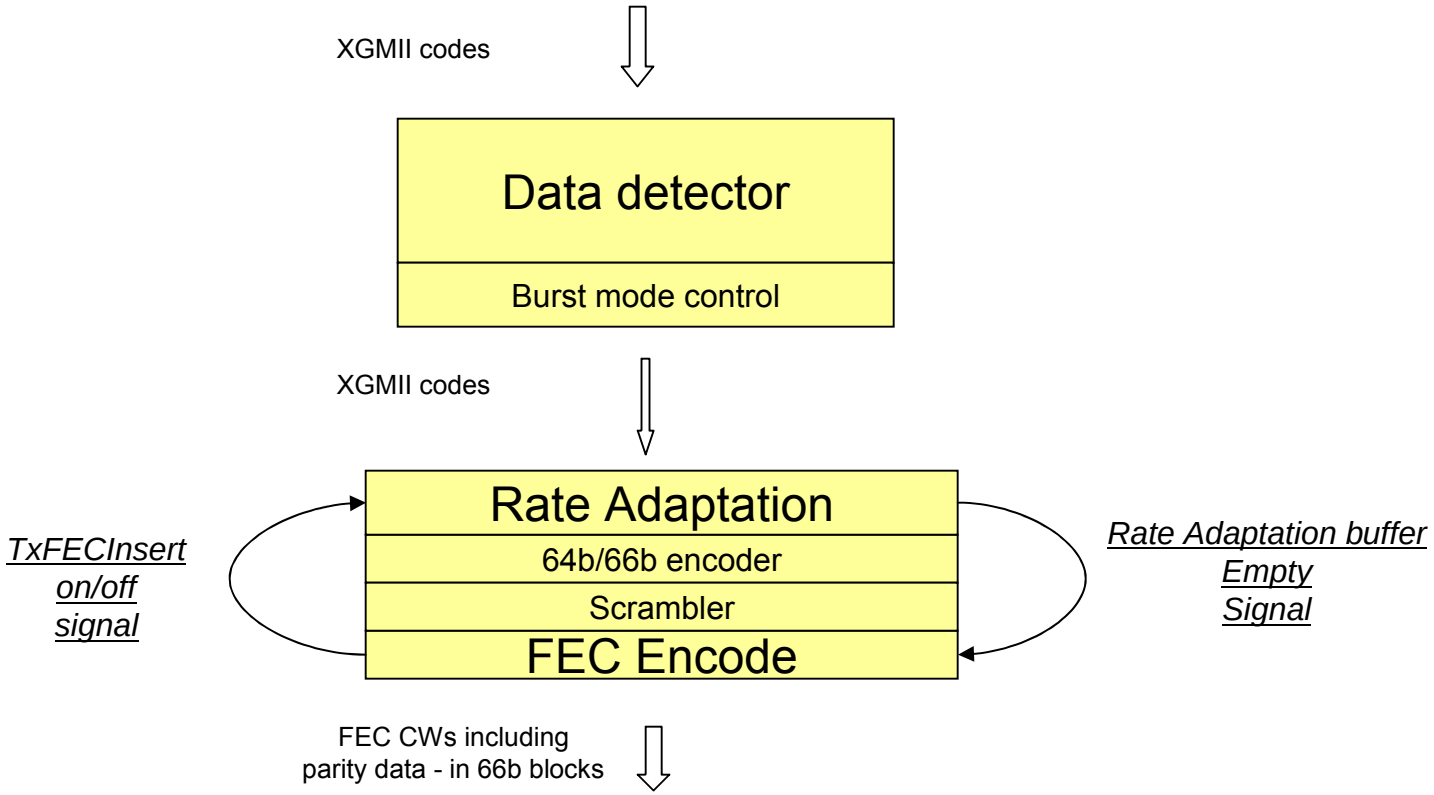


Data Detector Delay Line (FIFO) at start of Data Phase



Rate Adaptation

Sublayer Signals for Rate Adaptation



Rate Adaptation Sublayer

- *TxFECInsert On signal* from FEC encoder tells sublayer to stop downward transmission of codes (so codes received from above accumulate at end of buffer)
- *TxFECInsert Off signal* from FEC encoder tells sublayer to resume downward transmit of codes from front of buffer (so arriving codes from above will be added to the end of the buffer at the same rate that they clear from the front)
- When the buffer is non-empty, the sublayer deletes each arriving IDLE. The queued XGMII codes are concurrently dequeued from the front and transmitted to the 64b/66b encoder.

FEC encoder

- FEC encoder sends *TxFECInsert On* signal to Rate Adaptation sublayer when it is sending parity blocks.
- FEC encoder sends *TxFECInsert Off* signal to Rate Adaptation sublayer when it is ready to receive more 66b blocks.
- FEC encoder checks *RateAdaptationBufferEmpty* signal before turning on *BurstComplete* signal

Thank you