Scintera NETWORKS

EDC in a Module:
Practical considerations and pitfalls

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Module Design Considerations

- **Cost!**
- **Power/ Thermal Budget**
- **Size**
- **Ease of integration**

Module Consideration 1: Cost

Module vendor cost:

Objective: Cost of 10G-BASE-L* < cost of 10G-BASE-LR/ LX-4

- **Absolute cost of the EDC. Cost of ancillary circuitry. Will it require a more/less expensive receiver and transmitter?**
- **Will this improve or decrease margins?**
- **Resources required for design and test. How much more/less effort will it require over a competing solution?**

- **As compared to a 10GBASE-L module cost, $L, an EDC enabled 10GBASE-S-EDC module cost $S-EDC will break down as:**

$S-EDC = $L + $EDC chip + $EDC support circuitry - $LA ± $ΔRX ± $ΔTX

Module Consideration 1: Cost

- **A significant savings in the TX and RX can be realized as the required bandwidth is lower, allowing for cheaper packaging and components. TX eye requirements may also be relaxed allowing for FP and LW-VCSELs.**

- **Link cost may be reduced by eliminating the offset patch cord by using offset launch compliant TOSAs.**
  - **Also use of LW-VCSELs obviating need for offset launch patch cord.**

- **However, RX specifications must still address the appropriate link budget and overload constraints.**
  - **Linearity v/s bandwidth**

- **A simple, cost effective link compensation test methodology is required to reduce the cost of module volume manufacture. A worst-case link emulation scheme is required for this.**
  - **Use FIR filter with LMS-based coeff selection**
  - **Should this include dynamic compensation?**

Module Consideration 2: Power/ Thermal Budget

Thermal Power Budget:

Objective: Fit within power budget of small form factor modules.

- **How much power dissipation will it add?**
- **What is the limit?**
- **How much current may the module draw? Will this put it over the limit of that power rail?**

Module Consideration 2: Power/ Thermal Budget

Thermal dissipation limits of applicable 10G module MSAs

- **X2, XPAK → 4W**
- **XFP Type 1,2,3 and 4 → 1.5W, 2.5W, 3.5W, and >3.5W**

Examples of dominant sources of power dissipation:

- **XFP Retimer = 0.6 or 0.8W, avg. 0.7W**
- **XAUI SERDES = 0.9 to 1.5W, avg. 1.1W**
- **1310 laser (uncooled) = 0.10, 0.15 or 0.25W, avg. 0.15W**
- **Driver, 1310nm = 0.5, 1.3 or 1.5W, avg. 0.8W**
- **RX = 0.18, 0.22, 0.35, 0.50 or 0.82, avg. 0.6W**

Module Consideration 2: Power/ Thermal Budget

- **XAUI module power dissipation = 1.7 to 4.85W!**

Typical = 2.65W

- **XFP Typical = 2.25W, XFP Minimum (VCSEL and VCSEL driver) = 1.4W**

- **Power left for EDC in XAUI module**
  4.0 – 0.5 (overhead) – 2.65 ≈ 0.9W max
- **Power left for EDC in Type 3 XFP**
  3.5 – 0.3 (overhead) – 2.25 ≈ 0.9W max
- **Power left for EDC in Type 2 XFP**
  2.5 – 0.3 (overhead) – 1.4 ≈ 0.8W max
- **LW-VCSEL-based module may make it easier to meet Type 2 XFP reqs.**
- **A Type 1 XFP with EDC may require an integrated CDR and EDC device**

- **Any EDC solution should require less than 0.9W.**

Module Consideration 3: Size

Size considerations:

- **Objective: Size aggressive enough to fit into small form-factor MSAs**

- **Size of chip including space requirement of thermal management (thermal vias, pedestals)**

- **Size of extra support circuitry**
  - **Extra voltage supplies?**
  - **Additional bypass and power planes**
  - **Any power sequencing requirements?**

Module Consideration 4: Ease of integration

AC Interface to the EDC, Input:

- **What are the optical RX constraints?**
- **How does EDC affect the RX sensitivity, especially in the presence of a poor channel?**
- **How does EDC affect the RX overload, especially in the presence of a poor channel?**
- **Is there a back-to-back penalty/improvement?**
- **What is the minimum requirement on the RX bandwidth? Is there a maximum? Direct-modulation 1310 lasers often have high-frequency relaxation oscillation induced over and undershoots which can cause errors, particularly at overload. No efforts to quantify guidelines for this issue have been made, instead, maximums on receiver bandwidth have been set.**
- **There have been several contributions dealing with link budgets and required sensitivity, these must take TIA linearity into account.**

Module Consideration 4: Ease of integration

Overload

For proper RX with EDC operation, a TIA operating in its linear regime is required.

This must be taken into consideration when selecting a maximum received power.
IEEE 10GBASE-S-EDC $\rightarrow$ P_{rx} (max) = ? dBm

Optical Receiver output = V_{out} (mVpp) = P_{rx}(mW) x $\Re$ (A/W) x R_{TIA} (V/A)

For commercial receivers, V_{comp} is the 1dB compression point of the output. This may be as low as 400mVpp (single ended).

Assuming $\Re$ = 0.9 A/W, For an R_{TIA} range of 600 to 1500 V/A,
P_{max} < (V_{comp} / ($\Re$ x r_{TIA})), which depending upon r_{TIA} can be -1.3 to -5.3dBm.

Module Consideration 4: Ease of integration

AC Interface to the EDC, Output:

- **Is the output swing compliant to commercial CDRs?**
  - **EDC chip single ended output minimum and maximum should be >50mVpp and <800mVpp to interface with currently available XFP CDRs.**

Module Consideration 4: Ease of integration

- **What is the jitter tolerance?**
  - **EDC must be compliant with IEEE, and optionally, in addition, Fiber Channel, SONET and ITU jitter tolerance standards.**
- **An EDC solution should be data rate and protocol agnostic.**
- **For ease of integration, it should not require a reference clock.**

Module Consideration 4: Ease of integration

- **An EDC solution must be link adaptive. The minimum rate of adaptation depends upon the dominant non-ideality. e.g. In the case of single-mode fiber, 1kHz for PMD.**
  - **A minimum MMF EDC adaptation rate based on time-varying modal noise is required.**

- **An EDC solution must be able to adapt to all the types of dominant linear and non-linear phenomena present in MMF links.**
  - **What about non-correlated sources of noise?**

Recommendations

- In order to reduce cost, a 10GBASE-L* module standard should recognize that TX and RX specifications may be relaxed.
- A simple link compliance test methodology is required for volume manufacture.
- As a target, the power budget of an EDC solution should be less than 0.9W.
- P_{rx} (min) and P_{rx} (max) specifications must take into account the requirement of TIA linearity within the framework of commercially available TOSAs and ROSAs.
- The EDC should be compliant with the input requirements of commercial XFP retimers and XAUI SERDES.
- It should also require a minimum of microcontroller overhead.