Link Status Reporting: Request For Comment

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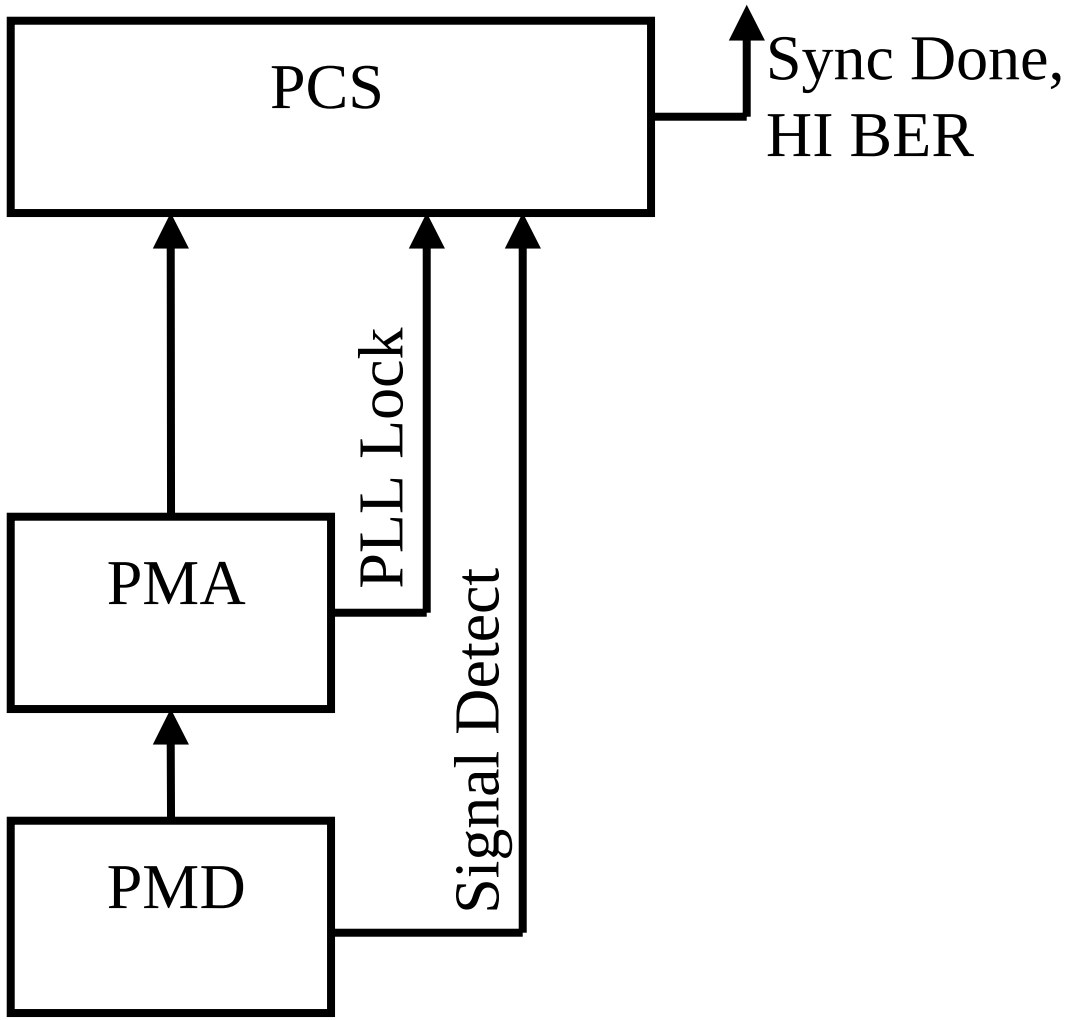
Issues

- What kinds of status are available from all the layers?
- What needs to go “up the stack” in real time?
- What needs to be available for debug?
- Where can that debug information be found?

Serial LAN

- PMD reports Signal Detect via pin;
- PMA reports PLL Lock via pin;
- PCS takes in both Signal Detect & PLL Lock using the logical AND of these signals to enable the Lock state machine;
- Signal Detect & PLL Lock reporting via MDIO may physically occur within PCS chip using PMA/PMD device type.

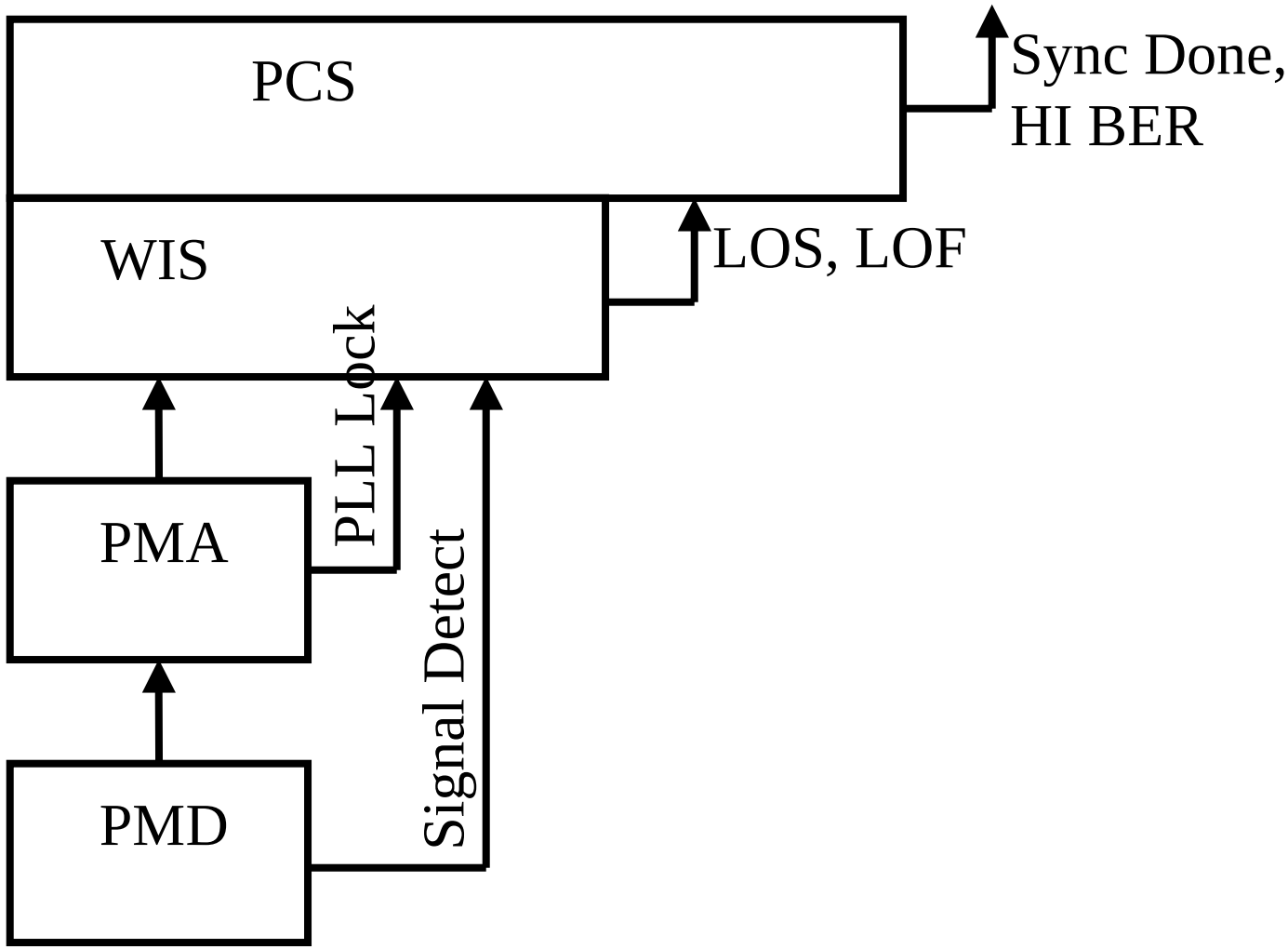
Serial LAN



Serial WAN

- PMD reports Signal Detect via pin;
- PMA reports PLL Lock via pin;
- WIS takes in both Signal Detect & PLL Lock using the logical NAND of these signals to report LOS;
- WIS reports LOS & LOF via MDIO status and makes them directly available to PCS;
- PCS uses the logical NOR of LOS & LOF to enable the Lock state machine;
- Signal Detect & PLL Lock reporting via MDIO may physically occur within PCS/WIS chip using PMA/PMD device type.

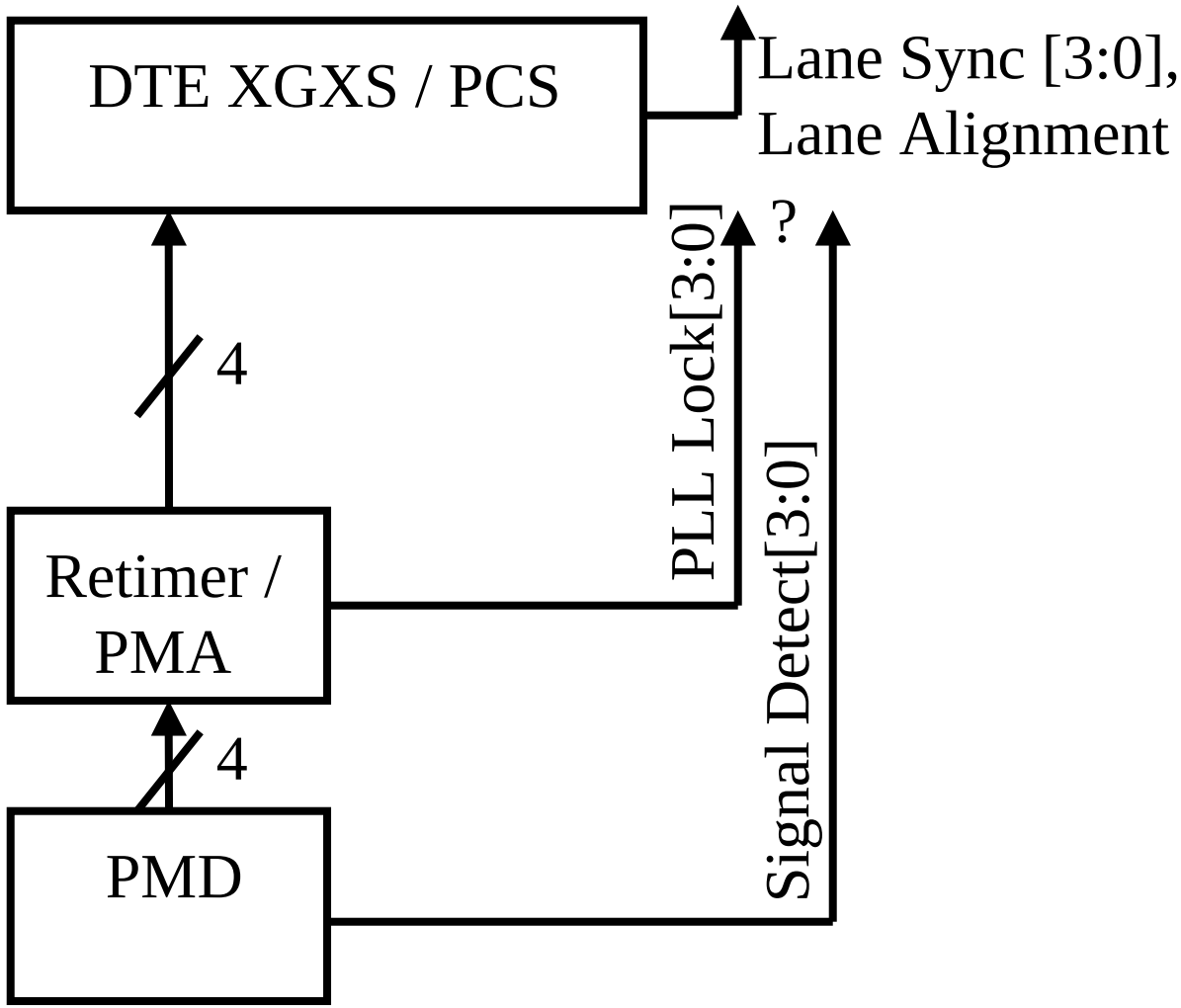
Serial WAN


PCS
Sync Done,
HI BER
WIS
LOS, LOF
PLL Lock
Signal Detect
PMA
PMD

WWDM LAN

- PMD reports Signal Detect [3:0] via pins or reports Signal Detect (a logical AND of the 4 individual Signal Detects) and implements an MDIO to report the individual signals;
- Retimer (PMA?) reports PLL Lock [3:0] via pins or reports PLL Lock (a logical AND of the 4 individual PLL Locks) and implements an MDIO to report the individual signals. (Does a retimer also have Lane Alignment?);
- DTE XGXS (PCS?) reports Lane Sync [3:0] and Lane Alignment, does not use Signal Detect or PLL Lock to inhibit alignment;
- Where are Signal Detect [3:0] and PLL Lock [3:0] reported when implemented as pins?

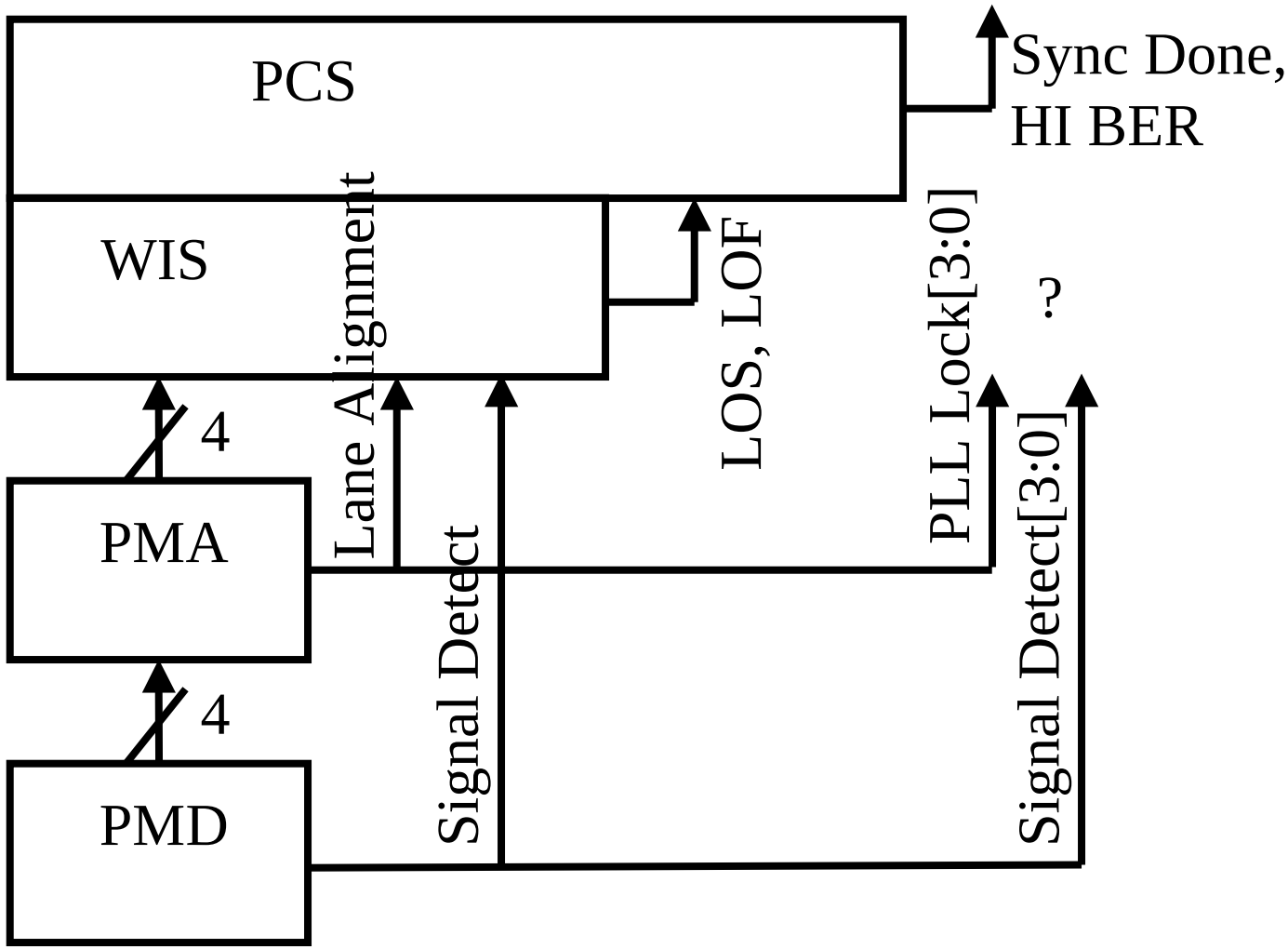
WWDM LAN


DTE XGXS / PCS
Lane Sync [3:0],
Lane Alignment
?
4
PLL Lock[3:0]
Retimer /
PMA
4
Signal Detect[3:0]
PMD

WWDM WAN

- PMD reports Signal Detect [3:0] via pins or reports Signal Detect (a logical AND of the 4 individual Signal Detects) and implements an MDIO to report the individual signals;
- PMA reports PLL Lock [3:0] and Lane Alignment via pins or reports Lane Alignment only (via pin) and implements an MDIO to report the PLL Lock signals;
- WIS takes in both Signal Detect (logical AND must occur outside or WIS has 4 input pins) & Lane Alignment using the logical NAND of these signals to report LOS;
- WIS reports LOS & LOF via MDIO status and makes them directly available to PCS;
- PCS uses the logical NOR of LOS & LOF to enable the LOCK state machine;
- Where are Signal Detect [3:0] and PLL Lock [3:0] reported when implemented as pins?

WWDM WAN


PCS
WIS
PMA
PMD
4
4
Lane Alignment
Signal Detect
LOS, LOF
PLL Lock[3:0]
Signal Detect[3:0]
Sync Done,
HI BER
?