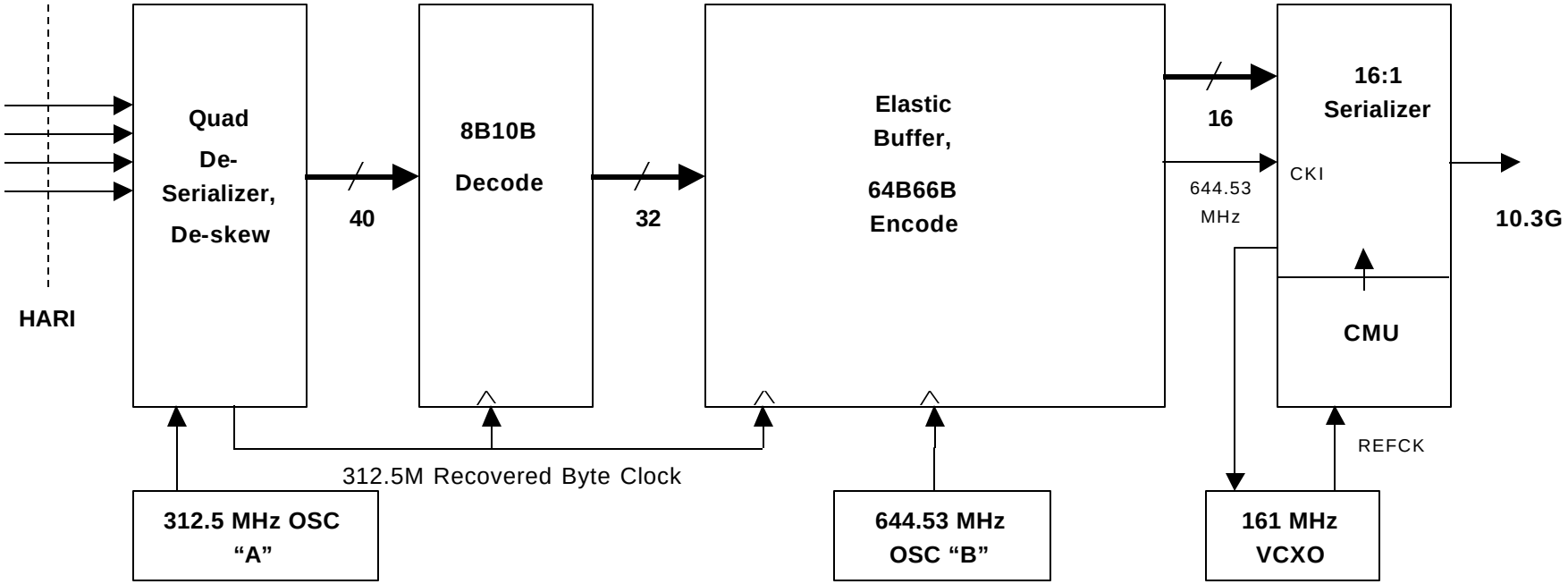
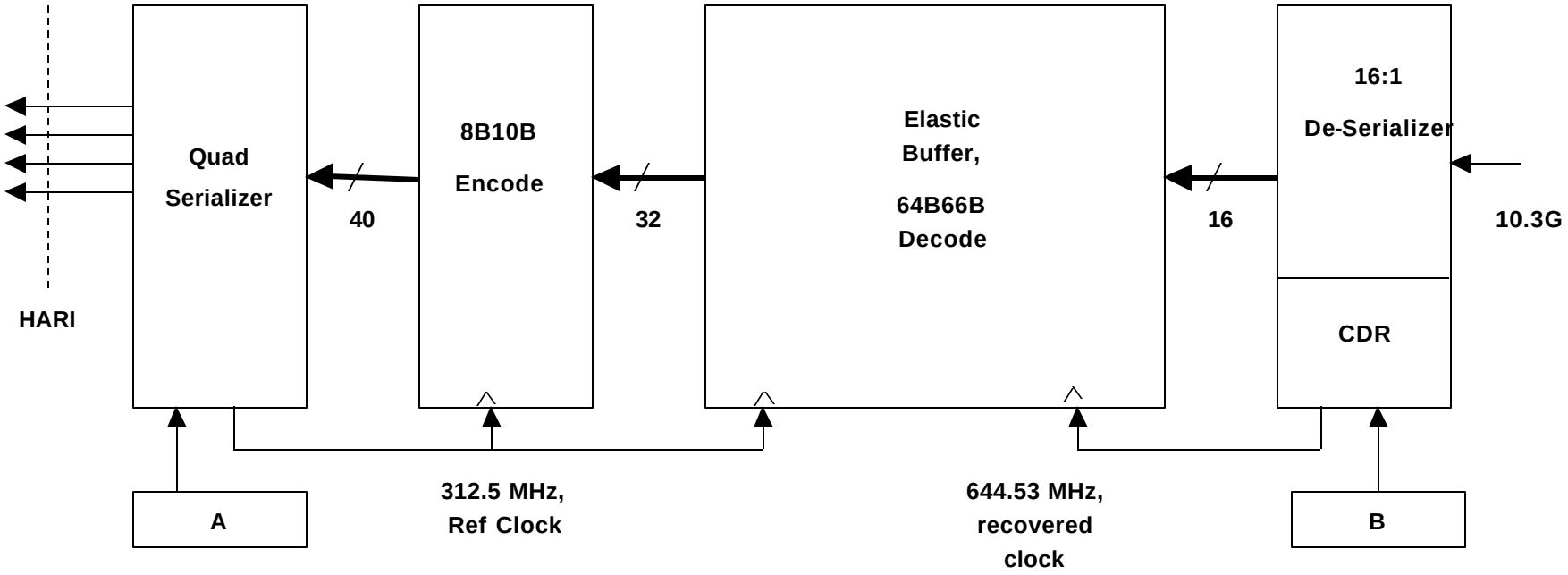
HARI Interface Chip for Serial PMD
A comparison of two clocking schemes

HARI chip, 2 clock domains, Tx path



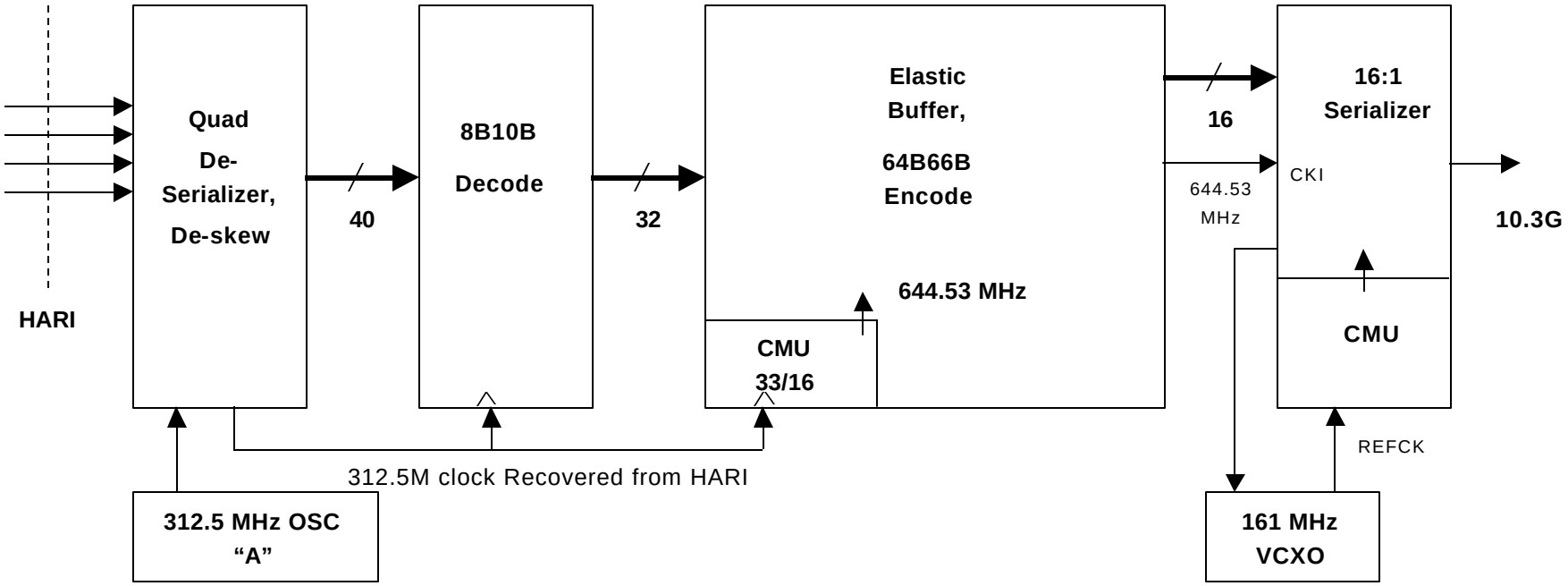
There are two clock/jitter domains in the transmit path - the HARI clock and the link clock. The 312.5 MHz oscillator is provided as a reference to which CDR inside the Quad de-serializer can lock to, in the absence of HARI data. The same oscillator also acts as a reference oscillator in the receive path to generate a new clock domain. The link clock domain is established by a reference 644.53 MHz oscillator. The serializer, in conjunction with VCXO, provides two features. (1) It builds a clean source of clock for serialization. (2) It nulls the phase difference between CKI and REFCK. This VCXO cannot substitute for 644.53M OSC because only a fixed reference can avoid circular clocking. To reduce cost, we should explore if we can eliminate VCXO and feed 644.53 OSC output into REFCK, via a delay line. This may work if the 644.53M OSC output is clean enough, and phase nulling can be approximated by a fixed delay.

HARI chip, 2 clock domains, Rx path



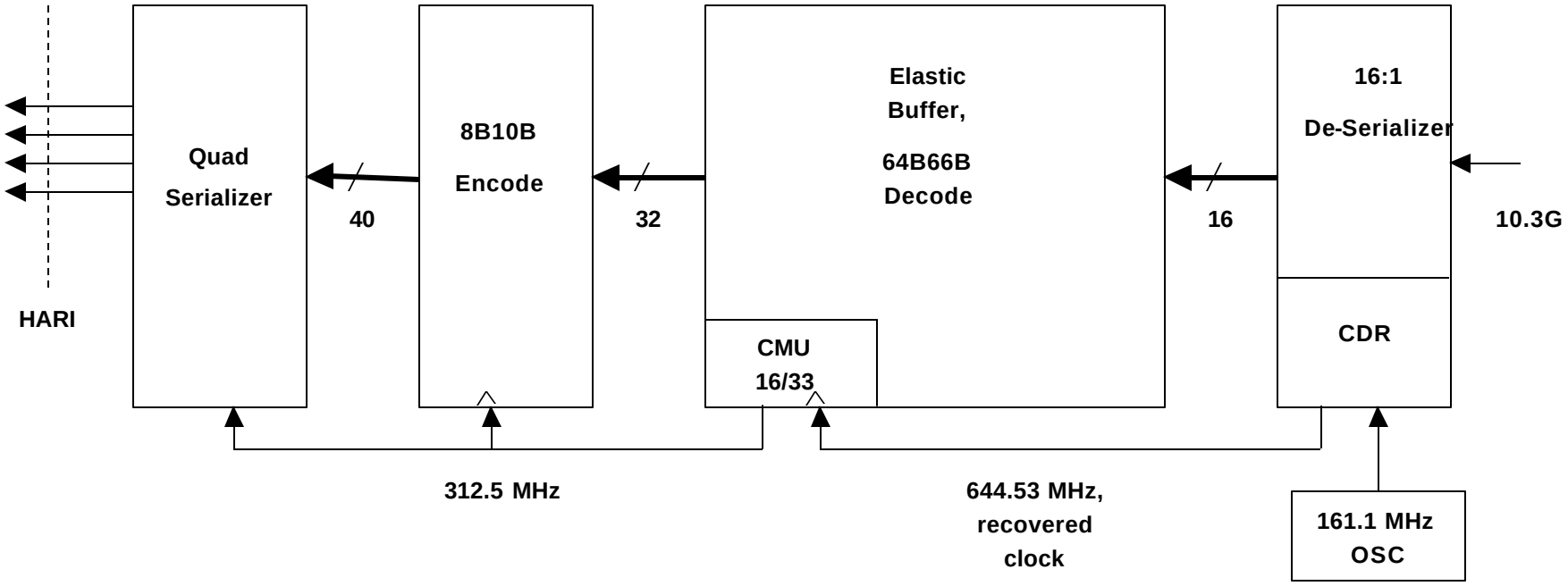
There are two clock/jitter domains in the receive path – link clock domain and HARI clock domain. Link clock is recovered from received serial data. Here B, the 644M OSC, is used as a REFCK to Clock and Data Recovery circuit inside the de-serializer. And A, the 312.5 MHz OSC, is used as a reference clock for the HARI clock domain.

HARI chip, 1 clock domain, Tx path



There is one clock/jitter domain in the transmit path - the HARI clock. The 312.5 MHz oscillator is provided as a reference to which CDR inside the Quad de-serializer can lock to, in the absence of HARI data. The 644.53M clock for link operation is obtained by multiplying the HARI-derived clock with 33/16. The serializer, in conjunction with VCXO, provides two features. (1) It builds a clean source of clock for serialization. (2) It nulls the phase difference between CKI and REFCK. It is not possible to eliminate VCXO because phase nulling in this scheme cannot be approximated by a delay line.

HARI chip, 1 clock domain, Rx path



There is one clock/jitter domain in the receive path – the link clock, recovered from received serial data. The 161M OSC is used as a REFCK to Clock and Data Recovery circuit inside the de-serializer. The clock required for 8B10B encode and Quad-Serializer is derived by multiplying the link clock with 16/33.

Comments

We have outlined two schemes, one in which link clock and HARI clock are in two separate domains, and another in which they are in the same domain. We should compare the two schemes in terms of cost, complexity and performance.

It appears that the cost difference between the two schemes will be small. Both schemes need three external clock components – one 312.5 MHz reference oscillator, one 161 MHz VCXO, and one more reference oscillator, which may be 161 MHz in case of one-domain solution, and 644 MHz in case of two-domain solution. The two-domain solution may be able to save cost by eliminating VCXO provided the the OSC clock is clean enough and phase nulling can be achieved with a fixed delay line.

The complexity difference between the two solutions is a matter of designer preference. One-domain solution requires two Clock Multiplier Units, one 33/16 and another 16/33. The two-domain solution requires two elastic buffers, one in transmit path and one in receive path.

Performance comparison would hinge on our estimate of jitter in the CMOS CMU outputs vs. jitter in the output of reference oscillators after it has entered the CMOS chip.