Update on Serial PMD Activities

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Goal of This Presentation

- To share information with HSSG about major design issues with implementing a Serial PMD, and observations on technology feasibility.
- To identify obstacles and make recommendations if appropriate.
- To provide an implementation perspective on Serial PMD.

The Big Picture

- We are very optimistic about the performance and cost-effectiveness of serial PMD implementations.
- There are no show-stopper obstacles, but there are several design issues and decision points.

Some Design Issues

- Link modeling
- SerDes width
- Coding for transmission
- HARI interface

Link Modeling

With 802.3z as a starting point, we should explore refinements in the link model and parameter inputs:

- Laser Relative Intensity Noise
- Jitter, VCO and 1/f Noise
- Method of estimating ISI Penalty
- Mode Partition Factor

Link Modeling – RIN, Reflections

- RIN: need lower values, for example, less than –130 dB/Hz for DFB.
- Improved laser optical isolation may be required to achieve lower RIN if receiver return loss remains at 12 dB as in 802.3z.
- Must determine the lowest cost trade-off between improved laser isolation and increased receiver return loss.
- Laser RIN test condition must represent worst-case link return loss.

Jitter, VCO and 1/f Noise

- VCO phase noise causes jitter and affects sensitivity.
- VCO design may be code-dependent.
- A Serial PMD will include a deserializer. The 1/f noise of VCO can translate to jitter. Cost-performance tradeoff.

Link Modeling Methods

- Accurate estimate of ISI Penalty is crucial
- One alternative to the 802.3z link model method is to combine simulations and analytic computations
  - Should be based on signal waveform as it may improve ISI Penalty estimate
  - Can take into account laser and receiver non-linearities
  - Can take advantage of better receiver description, i.e. Receiver filter order

Link Modeling – MPN

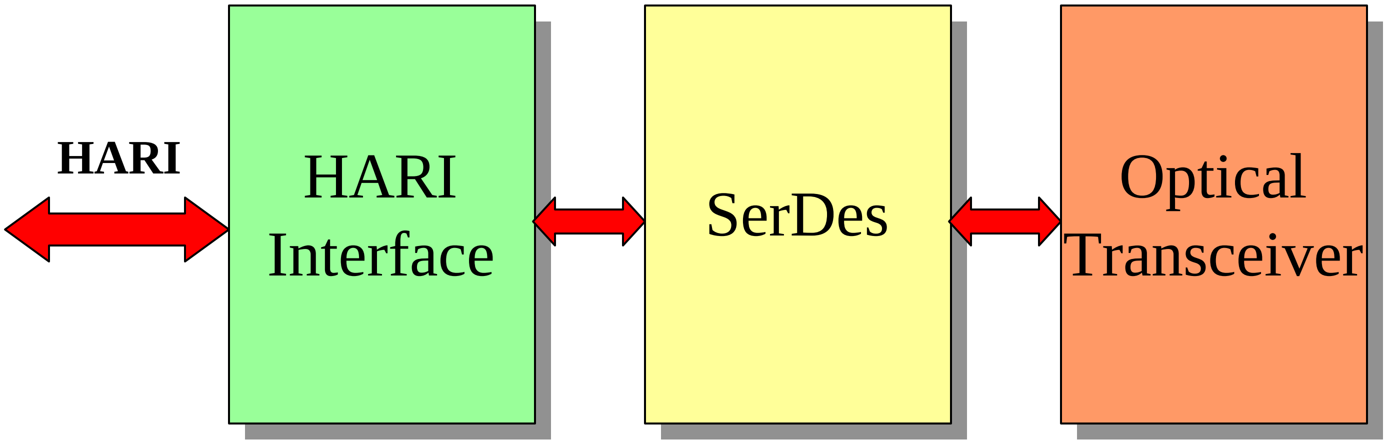
- To accurately predict Mode Partition Noise Penalty, k factor should be determined accurately.
- This factor for 850 nm VCSELs has been adopted from data on 1310 nm FP lasers.
- Need to establish a more accurate value of k using experimental data and analysis for both FP and VCSEL lasers.
- Need to examine alternate MPN model by S. J. Wang.

SerDes Width

For GaAs or SiGe implementations, a width of 4, 8 or 16 has clear benefits.

- At high speeds, power consumption is strongly influenced by architecture.
- Three basic architectures for SerDes are – shift register, phased clock and binary tree.
- Binary tree has advantages at 10G, but requires SerDes width to be 2^N: 4, 8 or 16.
- Width of 10 can be achieved with a two-block design, with 8:10 or 16:10 converter feasible in CMOS. [3]

Serial PMD Functional Blocks



Coding for Transmission

- Codes with 8B10B, scrambled encoding and 64B66B - all have distinct advantages. Therefore, at this stage, it is necessary to keep options open.
- Some codes need large divisors in clock multiplier units. The PLL implementation complexity has been discussed on the 64B66B reflector. No major obstacles are foreseen. (Zero overhead codes do not have this problem).

HARI Interface

- It is necessary to build early prototypes of HARI interface chips and learn about technology feasibility. Lack of consensus on striping is inconsistent with establishing a sense of direction.

Further work

- Prove concepts with experiments.
- Specify reduced RIN.
- Quantify jitter and any 1/f noise effects.
- Define power spectral density and baseline wander data for proposed coding schemes.
- Determine correct k for FP lasers and VCSELs.
- Explore if more accurate methods of estimating ISI penalty are needed.
- Achieve consensus on striping.

References

1. Chapter 38, IEEE 802.3z
2. Hakki et al., “Dispersion and Noise of 1.3-um Multimode Lasers in Microwave Digital Systems”, Journal of Lightwave Technology, Vol.7, No.5, May ’89, pg. 804
3. M. Fukaishi et al., “A 4.25-Gb/s CMOS Fiber Channel Transceiver with Asynchronous Tree-type Demultiplexer and Frequency Conversion Architecture”, IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, Dec. 98