Architecture and Objectives For a HARI PHY

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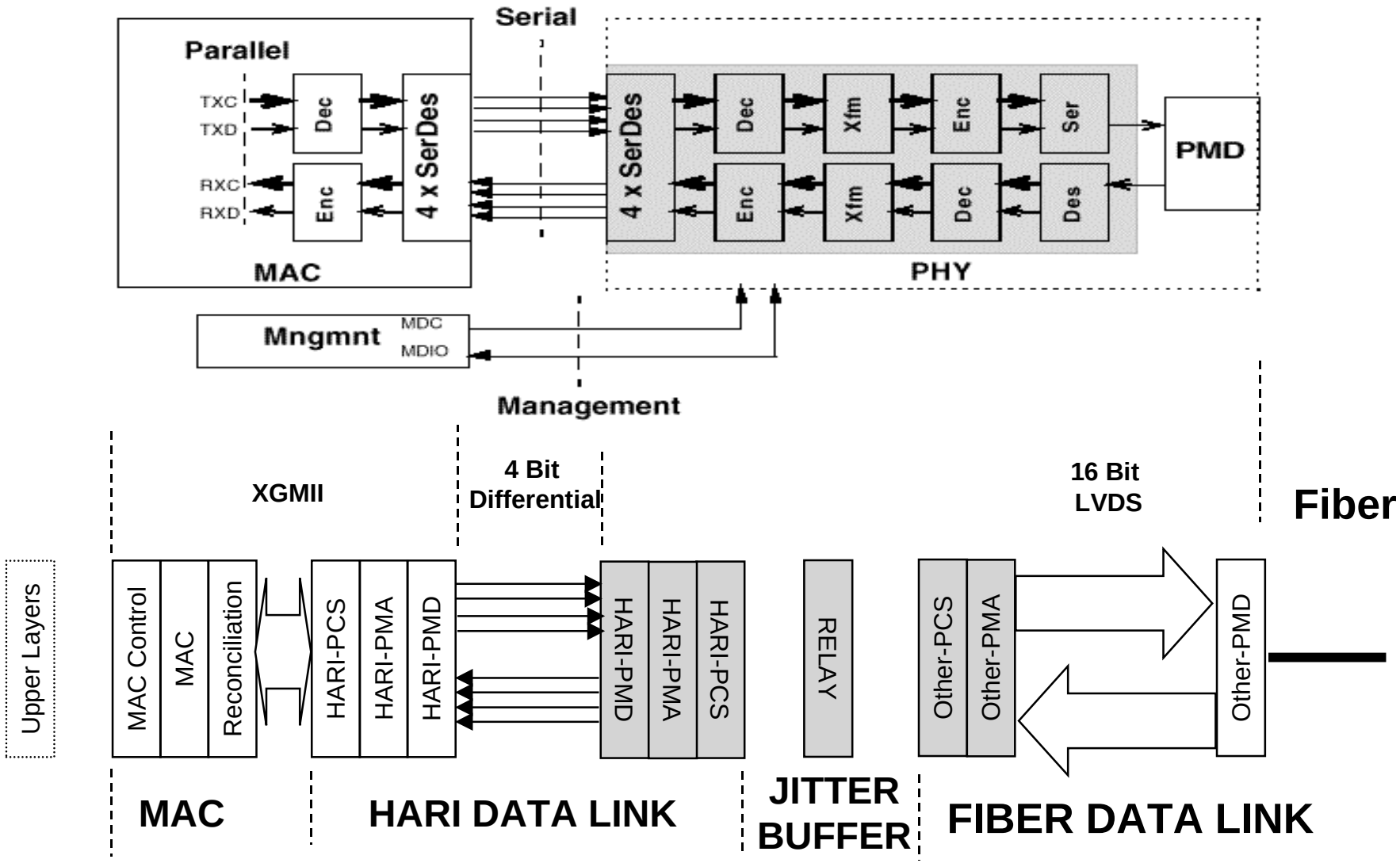
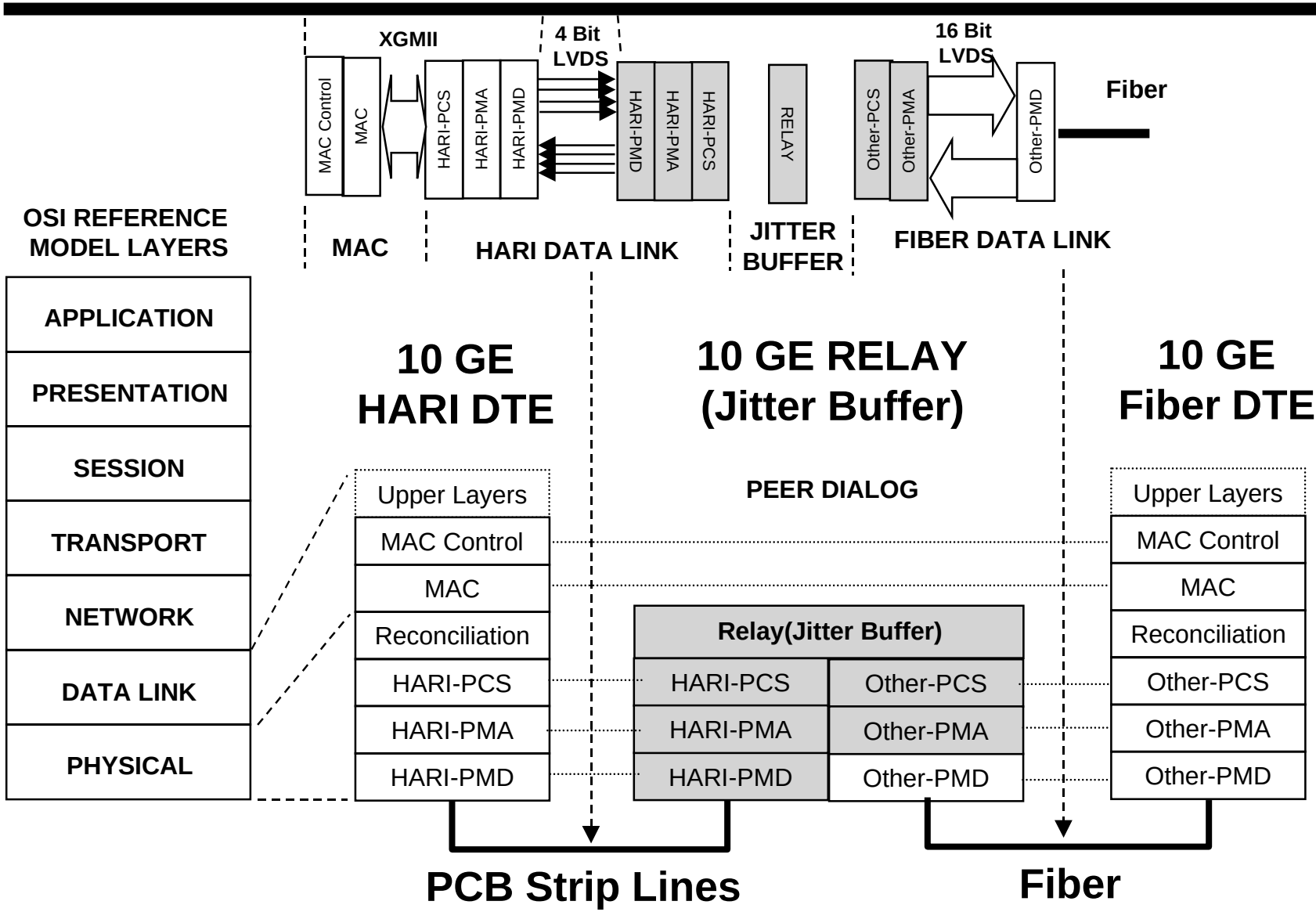
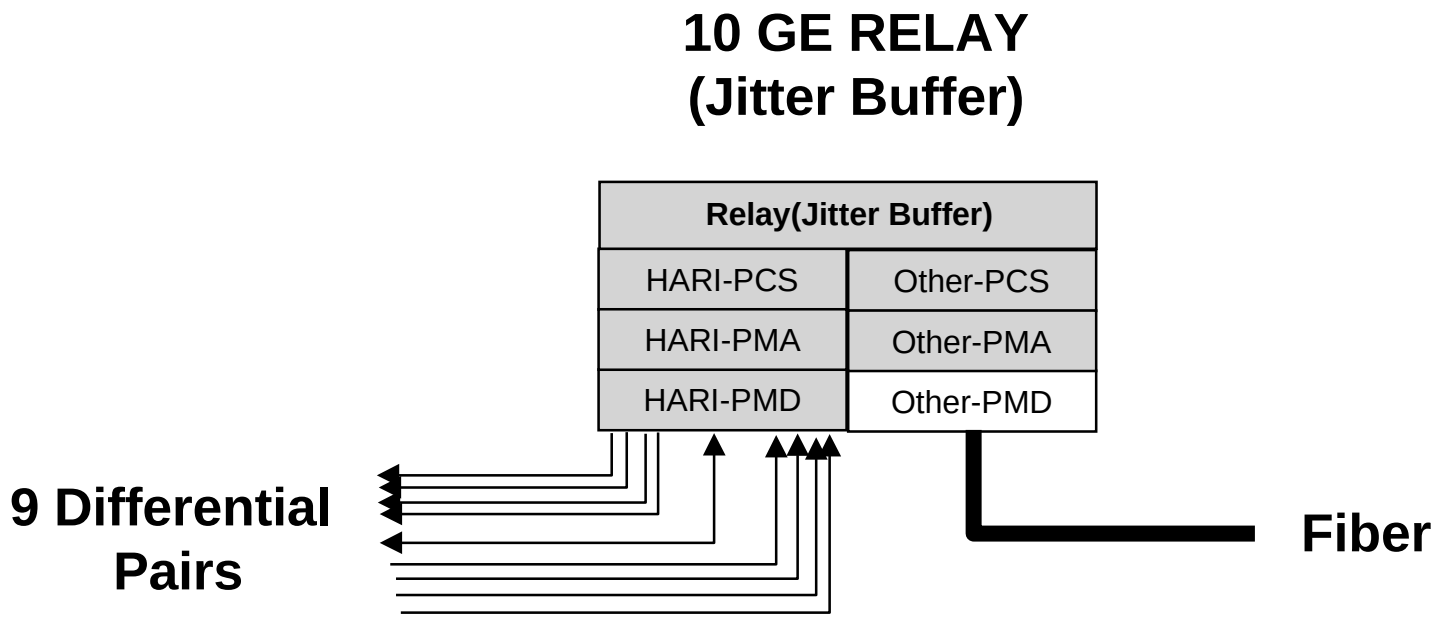
HARI Application to Architecture



HARI Architecture Model



A Relay Connects HARI-PHY to others



- **HARI interface uses a Level 1 relay (usually called a Jitter Buffer) for access to the PMD**
- **The stack in the relay provides the encode/decode for both the HARI protocol and for the Fiber protocol**
- **The Jitter Buffer performs the relay between the two PHY protocols**

HARI is a PHY

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- **The architecture of HARI is naturally explained by modeling HARI as a PHY**
- **PCB traces carrying HARI must be handled as analog transmission lines not digital logic**
- **HARI is not considered error free like digital logic**
- **HARI has all the design considerations of a data link including PMD, PLL, encoding, clock correction, etc.**
- **HARI is best standardized as a short distance copper PHY**

HARI Pros and Cons

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PROS

- **Very low pin count**
- **Long PCB trace distances**

CONS

- **High frequency (3G) signals**
- **High complexity including 8 PLLs**
- **PCB trances are transmission lines requiring special PCB and layout considerations**
- **Requires encoding over each signal**
- **Requires byte synchronization of each signal**
- **Requires phase alignment protocol**
- **Requires jitter elimination before coupling to PMD interface**
- **Very aggressive CMOS process**

Applications For a HARI Data Link

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- Onboard chip to chip connections
- Backplane connections
- Intra-box connections

HARI-PHY Objective

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- 1 meter over PCB traces would cover both chip-to-chip and backplane apps
- A relay from HARI-PHY to the LAN-PHY and from HARI-PHY to the WAN-PHY is required
- A method of slowing the data rate on HARI-PHY for the WAN-PHY is required

Recommendations

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- **Decompose HARI into a HARI-PHY and two L1 relays**
  - HARI-PHY to LAN-PHY relay
  - HARI-PHY to WAN-PHY relay
- **HARI is a useful option for extending the XGMII by adding a short distance HARI-PHY and a L1 relay between the XGMII and the LAN or WAN PHY**