New Sources of Lane to Lane Skew, and a Proposal for Alignment

HARI Skew budget (c.f. Taborek_1_1199

	# per link	Skew	Total Skew
PCB	2	<1 U.I.	<2 U.I.
SerDes	2	<1 U.I.	<2 U.I.
Medium	1	<14 U.I.	<14 U.I.
TOTAL			< 20 U.I.

E.g. 6.4 ns at 3.125 Gbaud

.: 20 UI deskew pattern needs to be 40-bits

Other Important Sources of Skew: Byte Alignment

Byte Alignment Approach 1: Stretch recovered clock

- Requires comma detect at baud rate, but uses few gates. Good approach for high power technologies

Approach 2: Rotate parallel data

- Comma detect at only at character rate, but uses more gates. Good approach for CMOS
- Introduces 0-9 U.I. of delay, since it quantizes comma position to a byte clock with arbitrary phase.

We should not preclude Approach 2

Other Important Sources of Skew: Clock Domain Crossing

FIFO's move data from recovered to local clock domain

- By its nature, effective FIFO latency is quantized to one period of "read clock"
- Therefore, it can add up to 10 U.I. of skew

Deskew circuits must be in a common clock domain, so operate on the data after this additional skew is inserted

Conclusion

Deserialization and clock boundary transition can generate up to 19 U.I. of skew.

A deskew mechanism capable of only +/- 10 U.I. continuously, and +/- 20 U.I. at initialization, is not sufficient.

Revised HARI Skew budget

	# per link	Skew	Total Skew
SerDes (TX)	1	<1 U.I.	<1 U.I.
PCB	2	<1 U.I.	<2 U.I.
Medium	1	<14 U.I.	<14 U.I.
SerDes (RX)	1	<20 U.I.	<20 U.I.
TOTAL			<37 U.I.

.: 40 UI deskew pattern needs to be 80-bits or more.

Proposal

Define a disparity-neutral character /A/, logically equivalent to /R/, except

- Not deletable,
- One column of /A/'s transmitted infrequently (e.g. no more than once per 64 bytes/16 columns, or once per IPG)

Receiver can align on columns of /A/ characters, even when there is no data.

New (Old) Proposal – Stuff Column

Lane 0	K	R	S	d_p	d	d	…	d	d	d	d_f	K	R	K	R
Lane 1	K	R	d_p	d_p	d	d	…	d	d	d_f	T	K	R	K	R
Lane 2	K	R	d_p	d_p	d	d	…	d	d	d_f	R	K	R	K	R
Lane 3	K	R	d_p	d_p	d	d	…	d	d	d_f	R	K	R	K	R

Change /R/ Column to /A/ infrequently

Lane 0	K	R	S	d_p	d	d	…	d	d	d	d_f	K	A	K	R
Lane 1	K	R	d_p	d_p	d	d	…	d	d	d_f	T	K	A	K	R
Lane 2	K	R	d_p	d_p	d	d	…	d	d	d_f	R	K	A	K	R
Lane 3	K	R	d_p	d_p	d	d	…	d	d	d_f	R	K	A	K	R

Summary

Overall skew budget requirement is larger than we thought.

Using deletable IDLE's for deskew results in too short a repeat interval

We need one distinguishable symbol to be used only for alignment.