



10GE WAN PHY & EoS

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Terminology

10GE WAN-Compatible PHY \neq WAN PHY
 \neq SONET/SDH
 \neq SONET “Lite”
 \neq T1X1.5 EoS

T1X1.5 EoS = MAC frames over SONET/SDH

T1X1.5 EoS & 10GE WAN-Compatible PHY

The key difference is **SONET compliance & therefore cost:**

T1X1.5 EoS*

- **fully SONET compliant**
- **broad application range**
 - 10M/100M/1G/10G
 - LO/HO, -nc/-nv
 - linear & rings

10GE WAN-C PHY

- **minimal OH usage**
- **wider clock tolerance**
- **higher jitter tolerance**
- **low cost optics**

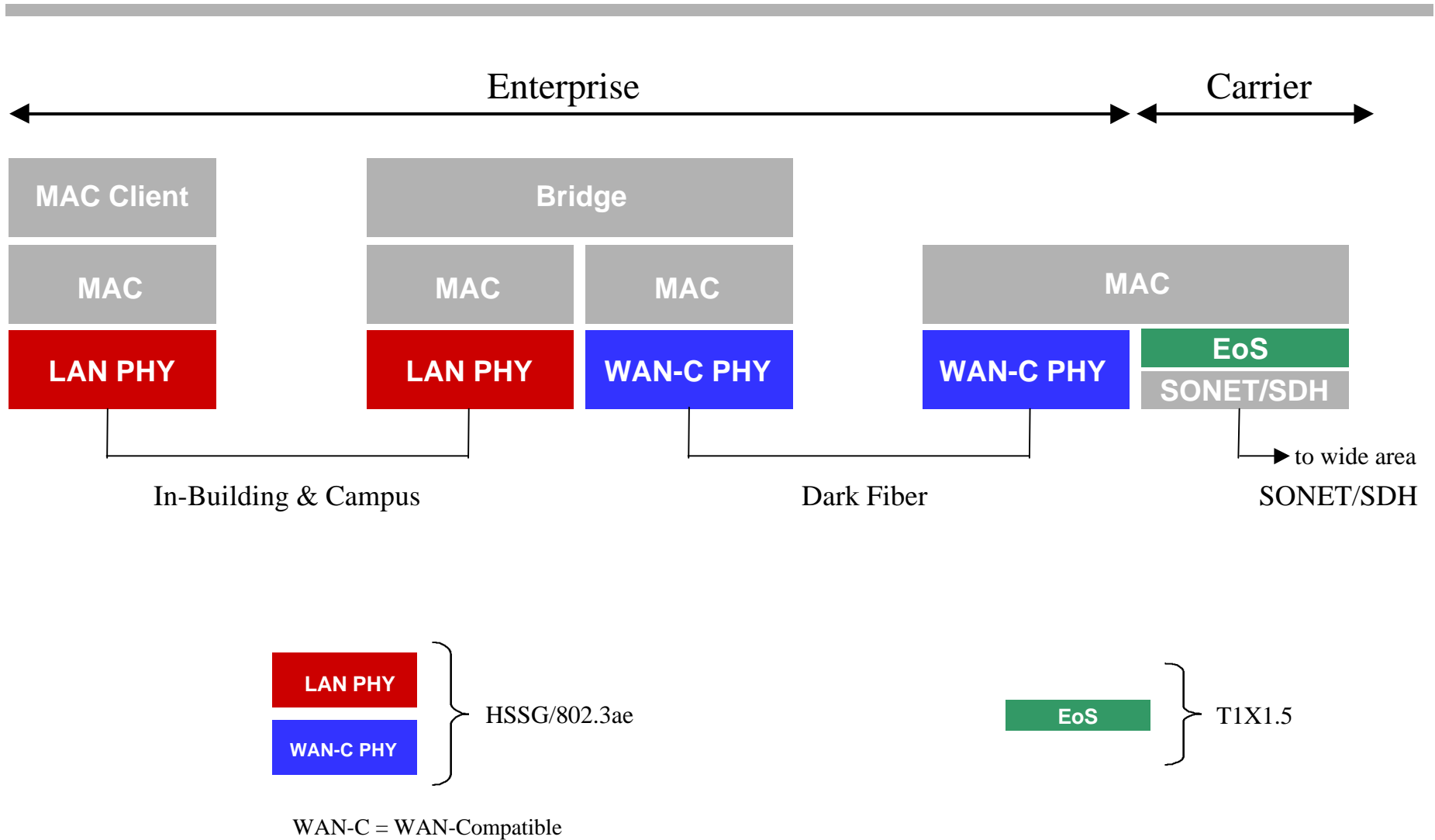
* T1X1.5/99-268r1 proposal

LO=Lower Order (<STM-1, <155Mb/s)
HO=Higher Order (>=155Mb/s)

nc=contiguous concatenation
nv=virtual concatenation

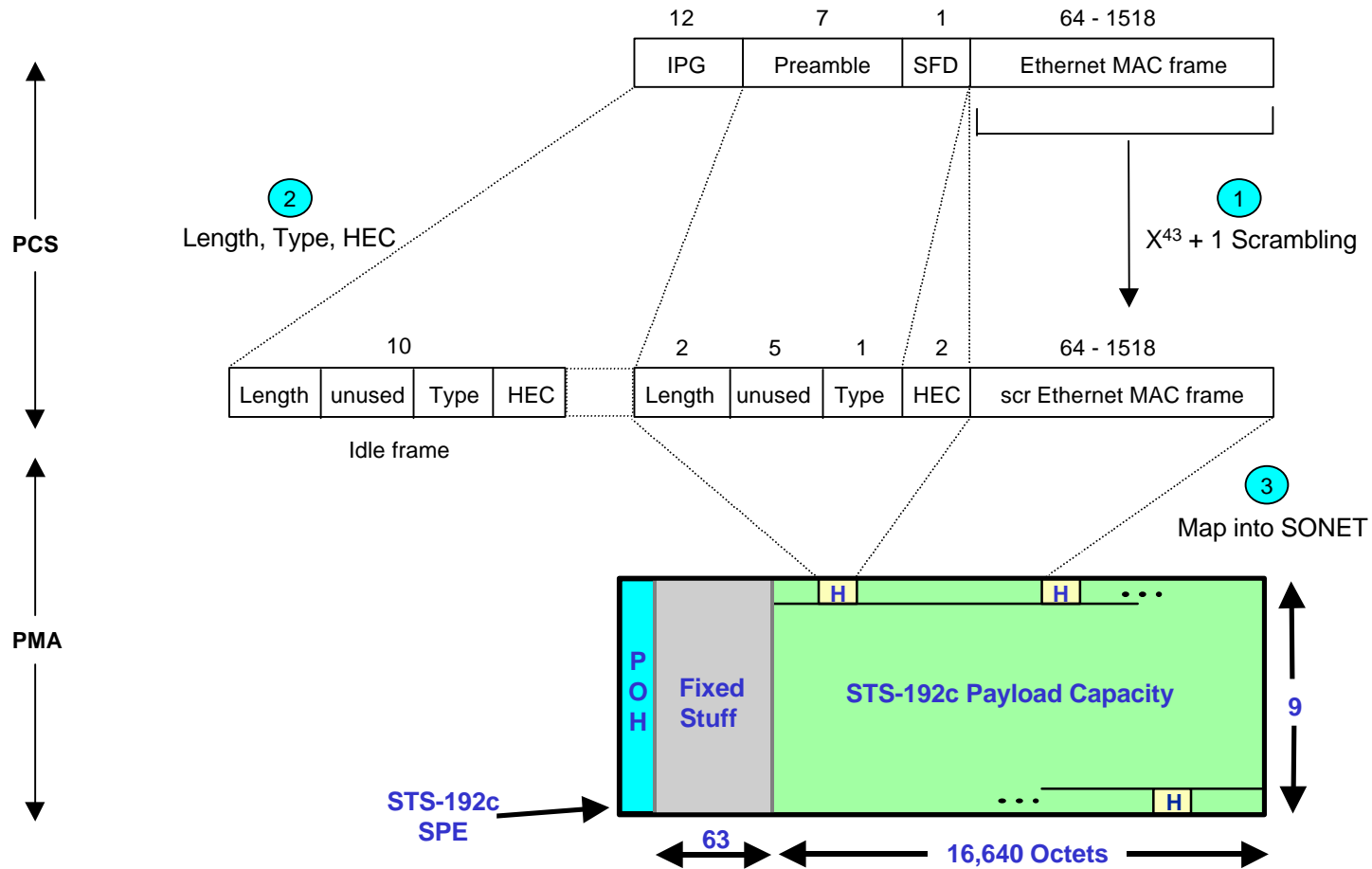
WAN-C = WAN-Compatible

Reference Model

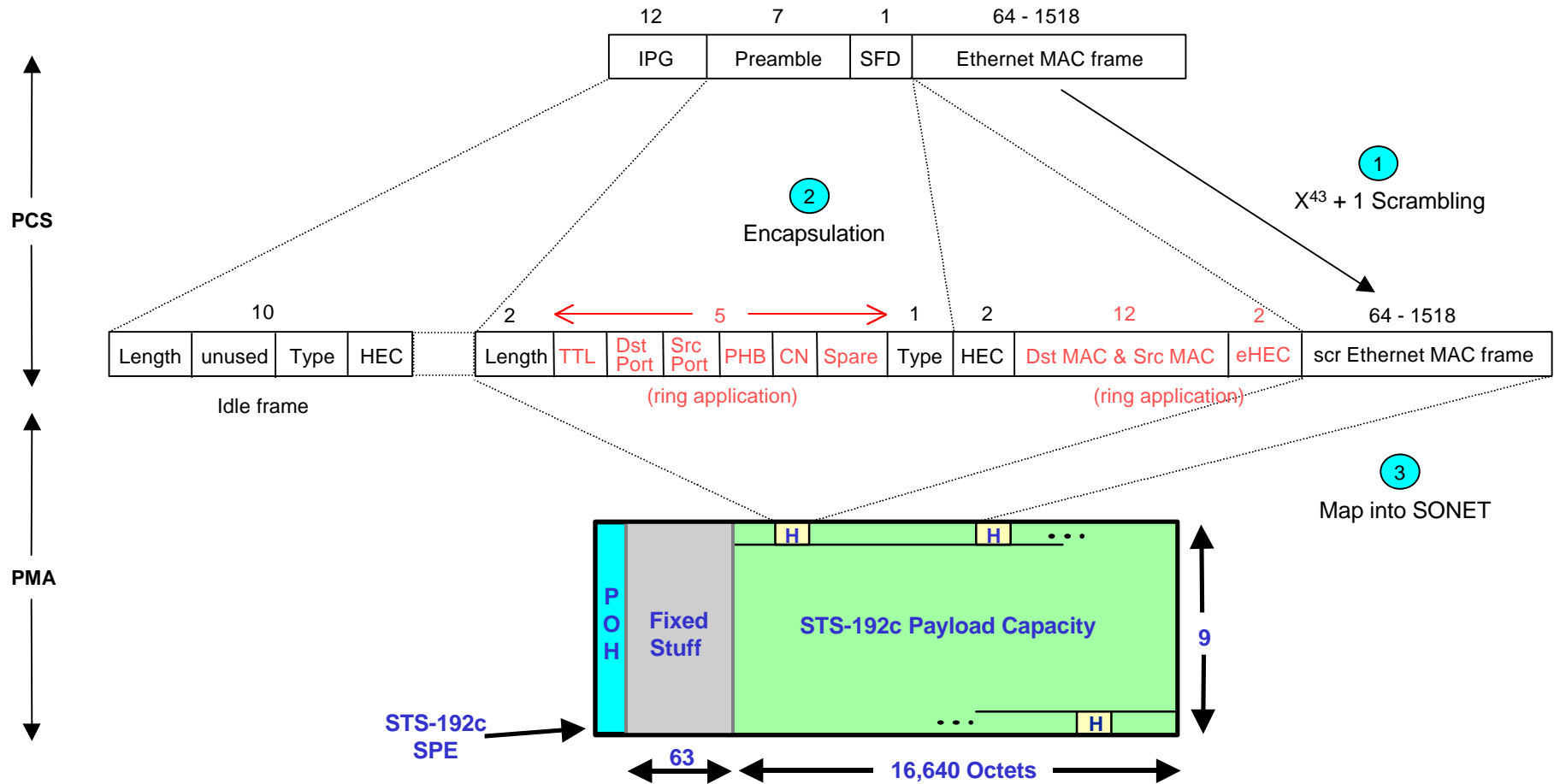


Backup

10GE WAN-Compatible PHY

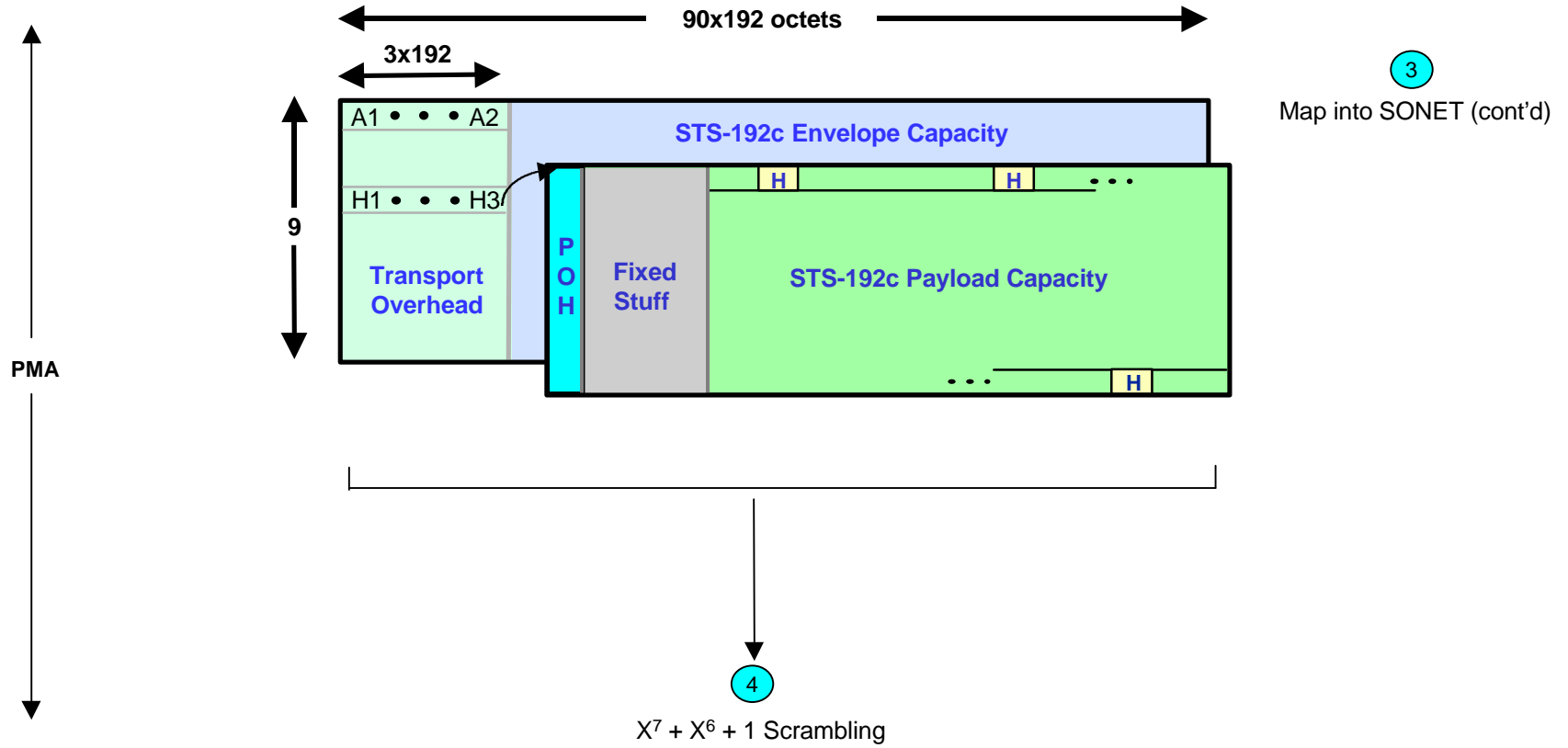


T1X1.5 EoS*

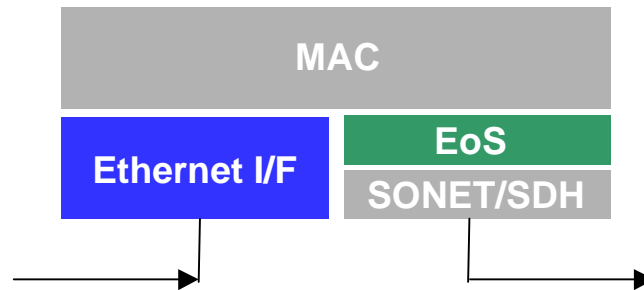


* T1X1.5/99-268r1 proposal

Common

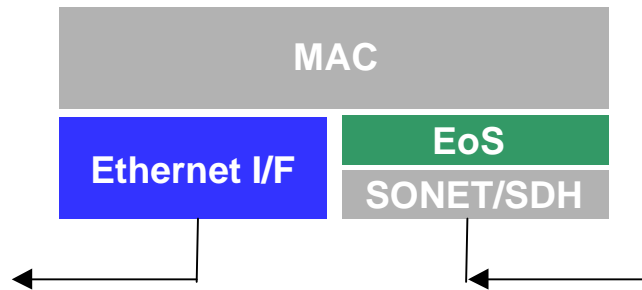


WAN Edge Device Functionality: Ingress



Ingress To Wide Area (Pt-Pt Link)		
Layer	Via 10M/100M/1G Interface	Via 10GE WAN-C Interface
Ethernet I/F	recover clock/data & line decoding	√
	delineate MAC frames	
	buffer (ingress shaping)	
EoS	encapsulate MAC frames	
	map into appropriate SONET SPE	
	add full Path OH	add Path Trace
	map into SONET frame	
	add full Line & Section OH	add remaining Line & Section OH
	scramble	√

WAN Edge Device Functionality: Egress



Egress From Wide Area (Pt-Pt Link)		
Layer	Via 10M/100M/1G Interface	Via 10GE WAN-C Interface
	recover clock/data & frame & descramble	√
	process full Section & Line OH	√
	pointer processing	
	process full Path OH	process Path Trace
	delineate encapsulated MAC frames	
	decap MAC frames	
	buffer (egress shaping)	
	line encoding	√