Technical Seminar

"The Impact of PWB Construction on High-Speed Signals"

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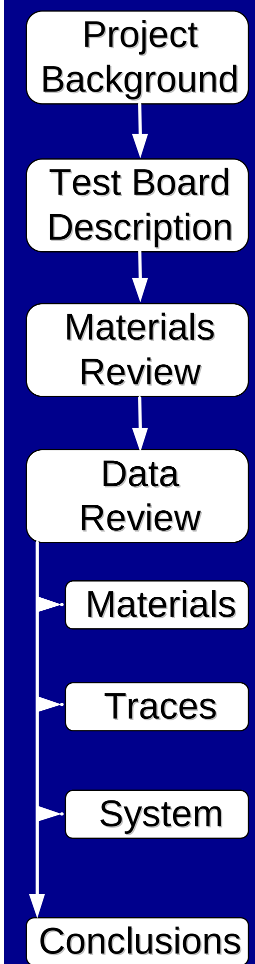
AMP Circuits & Design

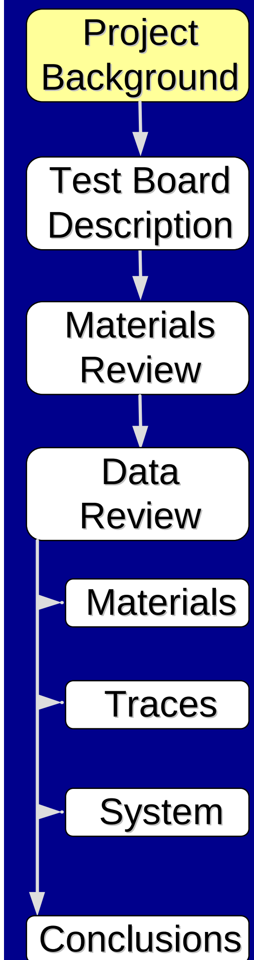
tyco electronics

Session Outline



- Project background
- Test board description
- Materials review
- Data review
  - Material properties
  - Trace properties
  - System properties
- Conclusions

Background and AMP Strategy



- Issues:
  - Increasing system speeds (1-10 Gbps)
  - Copper vs. optics
- Determine maximum copper performance
- Examine limitations
  - Dielectric materials
  - Trace geometries
  - Interconnect structures
- Explore options
  - RF techniques
  - Modulation schemes

Project Background
Test Board Description
Materials Review
Data Review
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Immediate Plan of Action

- Construct four sets of test boards
  - Multiple materials
  - Multiple trace structures
- Obtain both time and frequency data to examine copper limitations
- Use proven RF analysis techniques to characterize signal integrity of PWB structures at very high speeds

Project Background

Test Board Description

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Data Review

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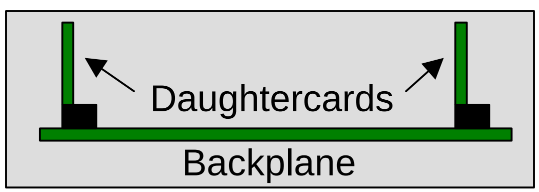
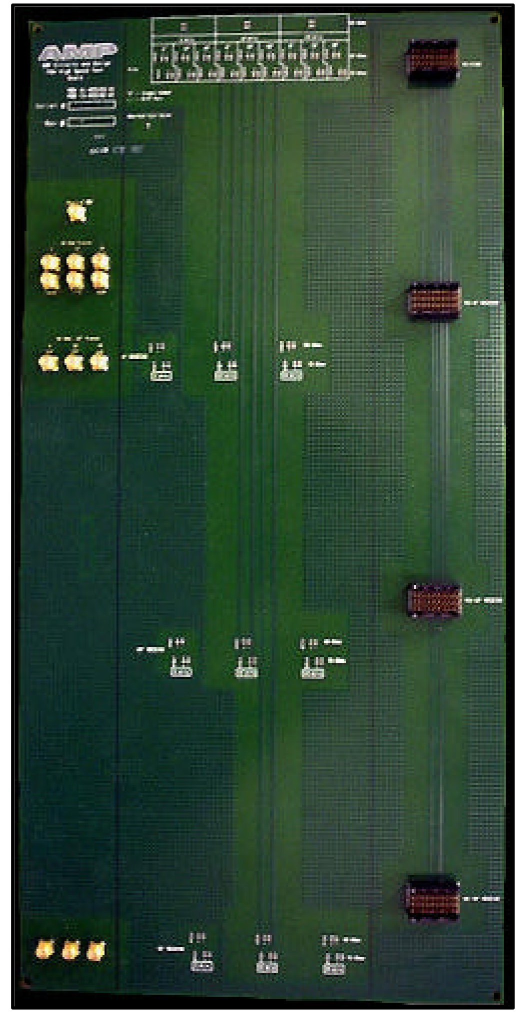
Board Layout Description

- Three sections
  - SMAs
    - Known behavior
    - Repeatable
  - Test points
    - Superior behavior
    - Repeatable
  - HS3 connectors
    - High-density
    - Real-world interconnect





Board Design Details

- Trace structures for each section
  - Trace widths: 5, 12, and 19 mils
  - Trace lengths: 6, 12, and 18 inches
  - Trace impedances: 50 and 75 Ω
  - Single-ended and differential signals
- All four board sets designed to be identical where possible
- Constant impedance maintained by varying layer thicknesses for each material (priority to maintain trace width)

Project Background

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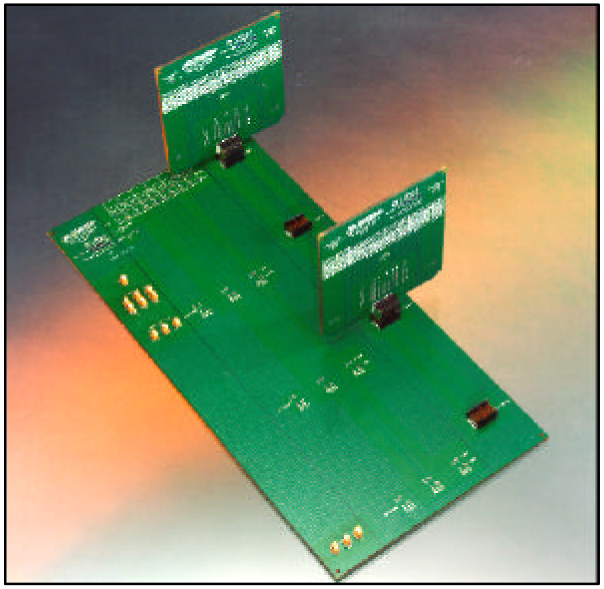
Materials Review

Material	e_r**	tan d**	T_g**	Moisture Absorption(%)**	Relative Cost***
FR4*	4.4	0.018	180°C	0.1	1
GETEK*	3.9	0.012	180°C	0.12	1.1
ROGERS 4350*	3.5	0.004	280°C	0.06	2.1
ARLON CLTE*	2.9	0.0025	288°C	0.04	6.8

*All boards built by TYCO printed circuits group
**Material properties listed are from the manufacturer
***Cost factor derived from 10” by 20”, 12-layer backplane

FR4

- Material properties
  - Woven glass/epoxy resin composition
  - Nelco 4000-6 *(Tg=180ºC)* laminate & prepreg
  - Standard fabrication procedures
  - Many thicknesses available
- Electrical properties
  - ε_r=4.4
  - tanδ=0.018
- Cost factor = 1*
- Insertion factor = 1*



*Relative to FR4

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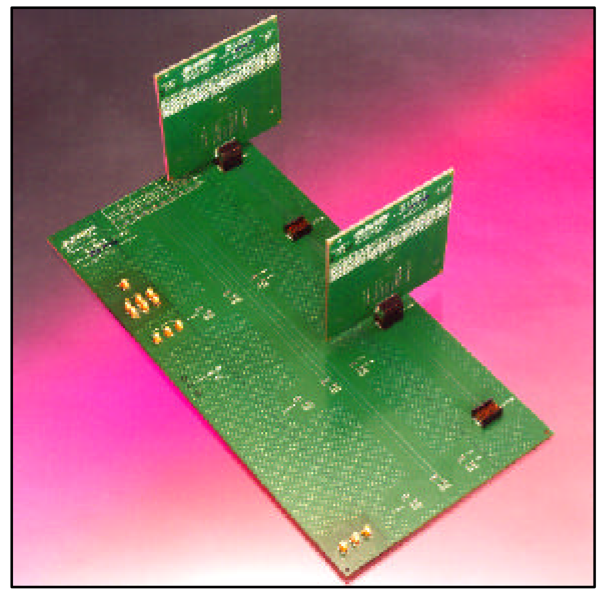
GETEK

- Material properties
  - Polyphenylene oxide/epoxy composition
  - ML200 laminate & prepreg
  - Fabrication requires minor modifications
  - Several thicknesses available
- Electrical properties
  - ε_r=3.9
  - tanδ=0.012
- Cost factor = 1.1*
- Insertion factor = 1.6*



*Relative to FR4

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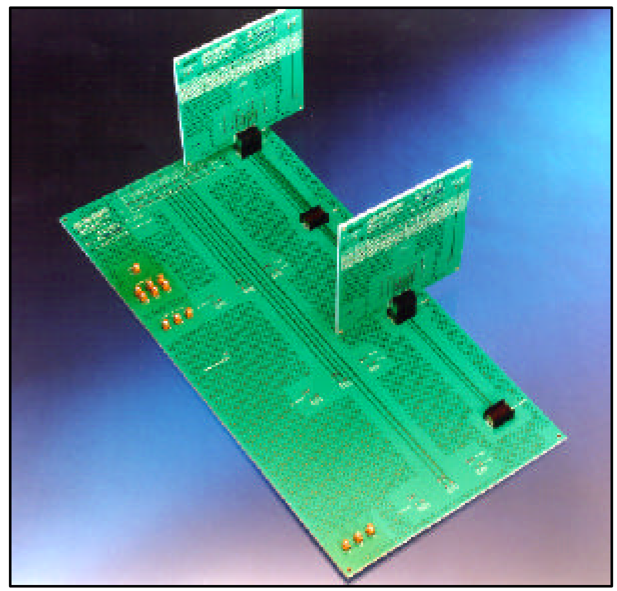
ROGERS 4350

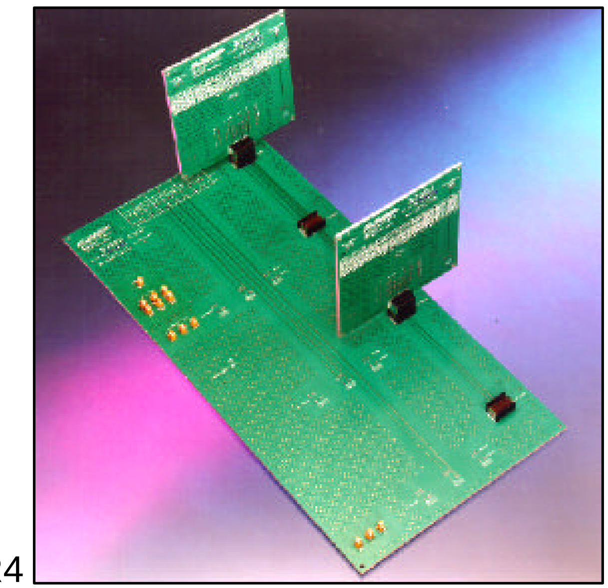
- Material properties
  - Glass-reinforced ceramic thermoset
  - ROGERS 4350 laminate & 4320 prepreg
  - Fabrication requires minor modifications
  - Several thicknesses available
- Electrical properties
  - ε_r=3.5
  - tanδ=0.004
- Cost factor = 2.1*
- Insertion factor = 1.9*



*Relative to FR4

ARLON CLTE

- Material properties
  - Glass-reinforced ceramic/PTFE composite
  - ARLON CLTE laminate & prepreg
  - Fabrication requires special processes
  - Limited thicknesses available
- Electrical properties
  - ε_r=2.9
  - tanδ=0.0025
- Cost factor = 6.8*
- Insertion factor = 2.2*



*Relative to FR4

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Time-domain Testing

- Typical for signal integrity analysis
- Tests performed
  - Bit sequence eye patterns to 3 Gbps
  - Clock bit patterns to 3 GHz
- Equipment
  - HP 8133A bit generator
  - Tektronix 11801C digitizing oscilloscope
- Conclusions
  - Material information not easily extractable
  - Test equipment speed limitations

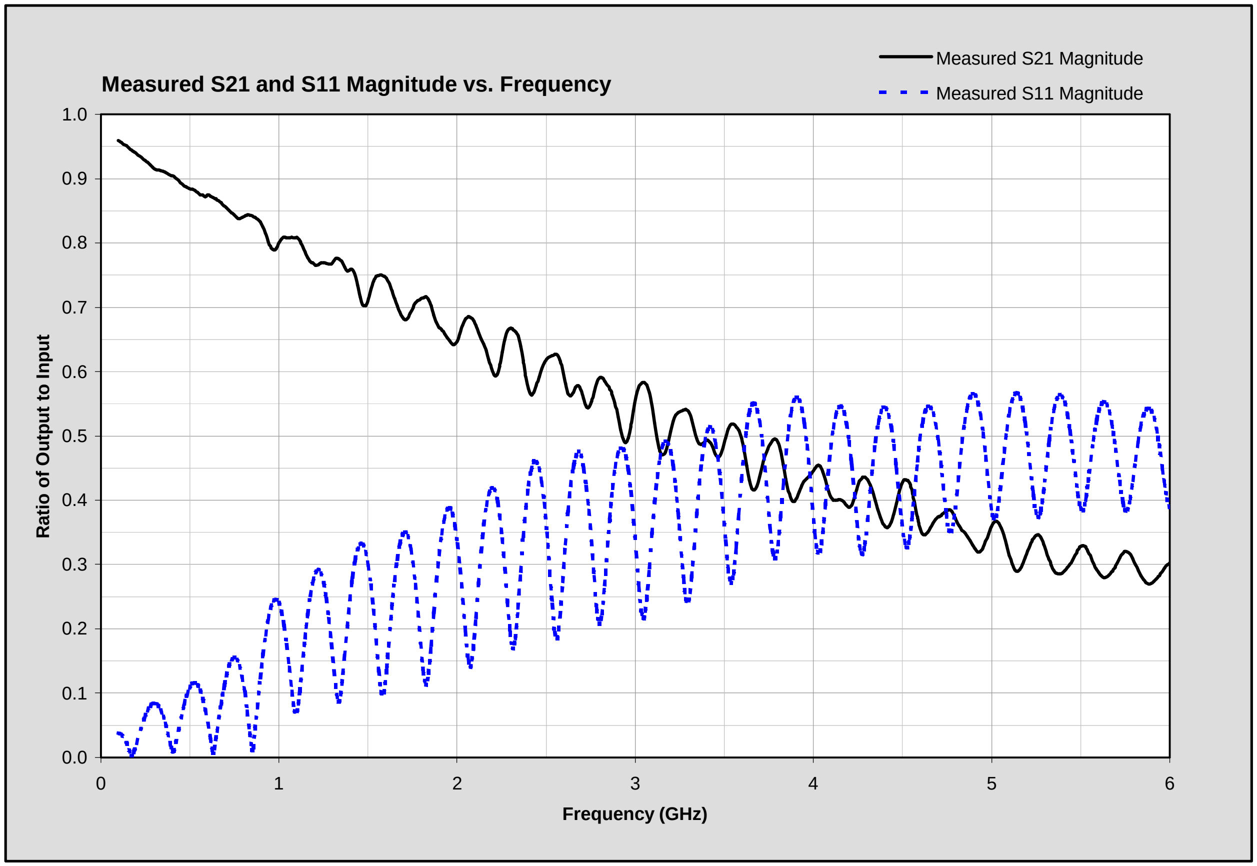
Frequency-domain Testing

- Information more fundamental
  - Proven techniques to extract material information
  - Building block to extract trace and system information
  - Less bandwidth limitations
- Two port S-parameters to 6 GHz
- Equipment
  - HP 8753D network analyzer
  - HP 85033D calibration kit

Measured Frequency Data

- Project Background
- Test Board Description
- Materials Review
- Data Review
  - Materials
  - Traces
  - System
- Conclusions

- S_{21} & S_{11} for 12" trace with test points



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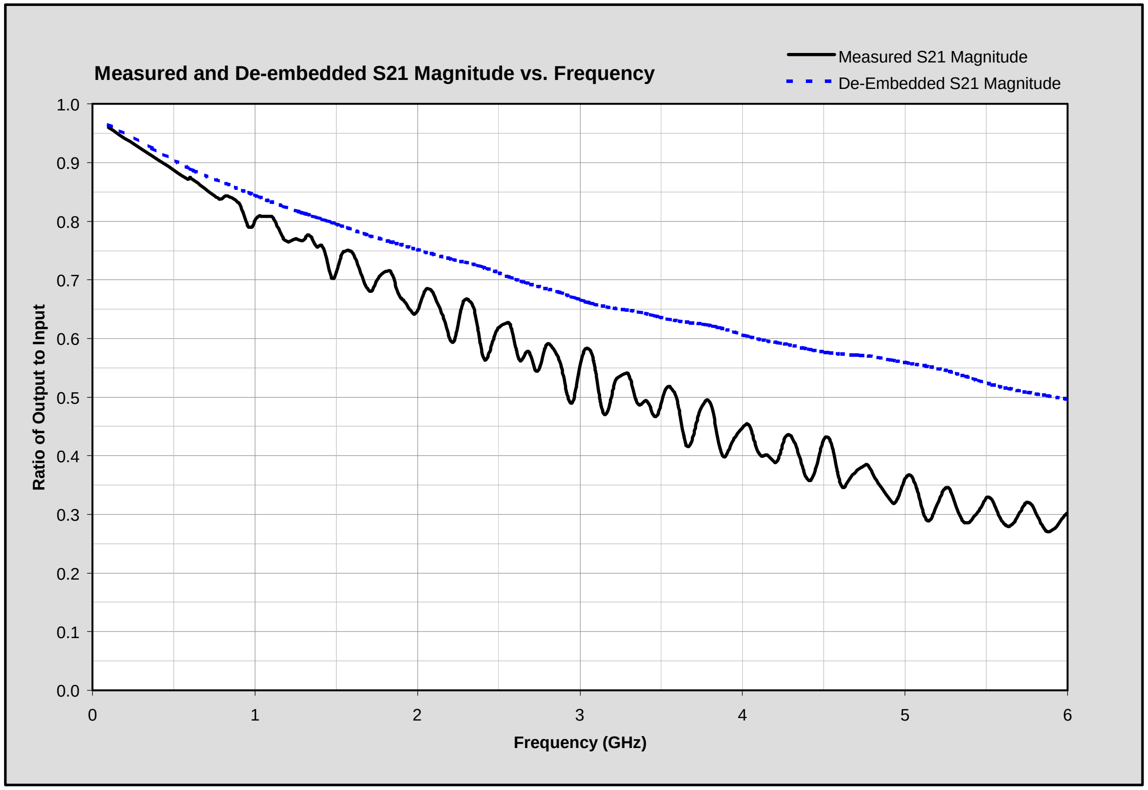
De-embedding Techniques

- Removes effects introduced by test fixtures
- AMP used the Through-Reflect-Line (TRL) method
- Trace data can be used to derive material properties
  - Effective dielectric constant (ε_r)
  - Loss tangent ($\tan\delta$)
  - Conductor loss factor (α_c)
  - Impedance(Z_o) and propagation velocity

De-embedded Frequency Data

- S_{21} for 12" trace with test point effects removed (S_{11} becomes negligible)



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Materials Comparison

- Project Background
- Test Board Description
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  - Materials
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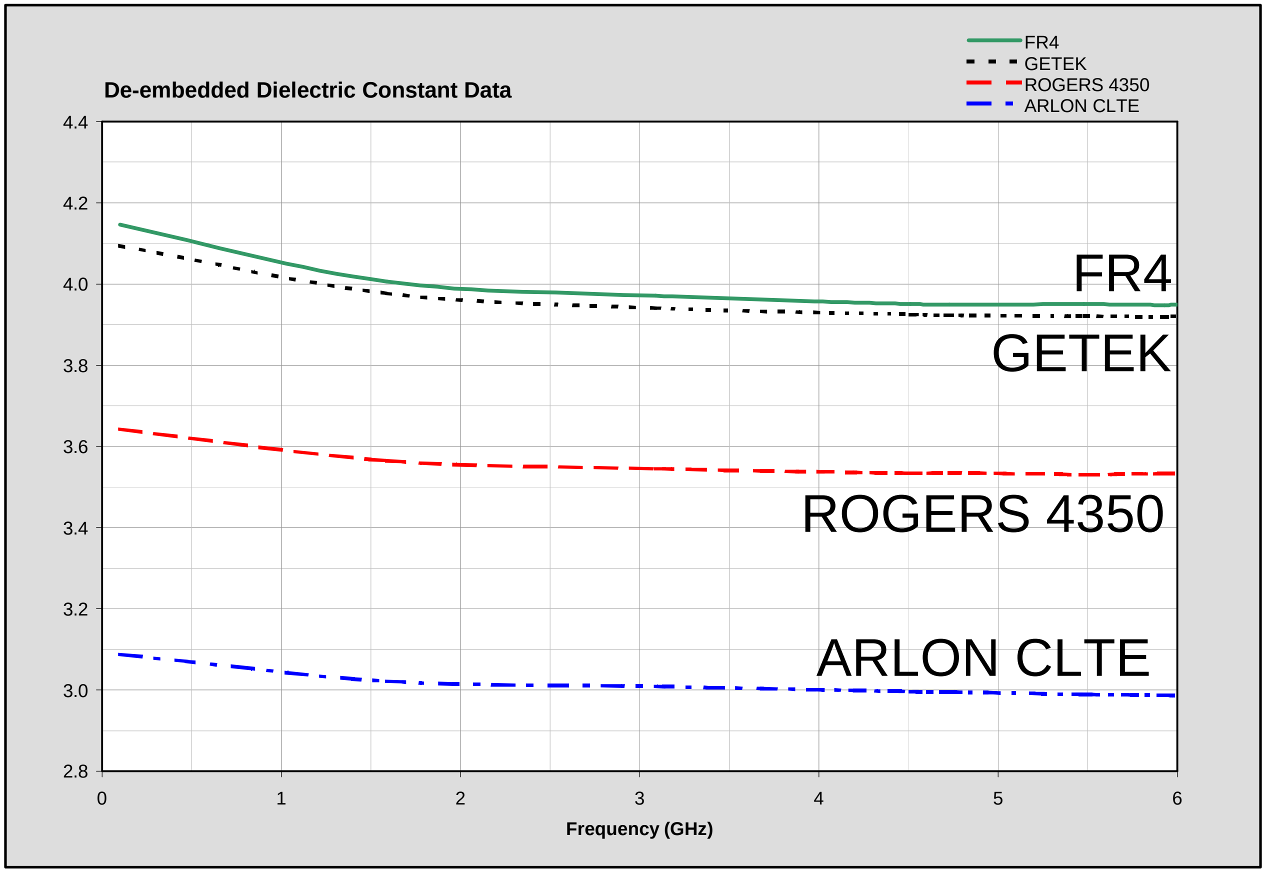
- Dielectric constant (ε_r) vs. frequency



Project Background

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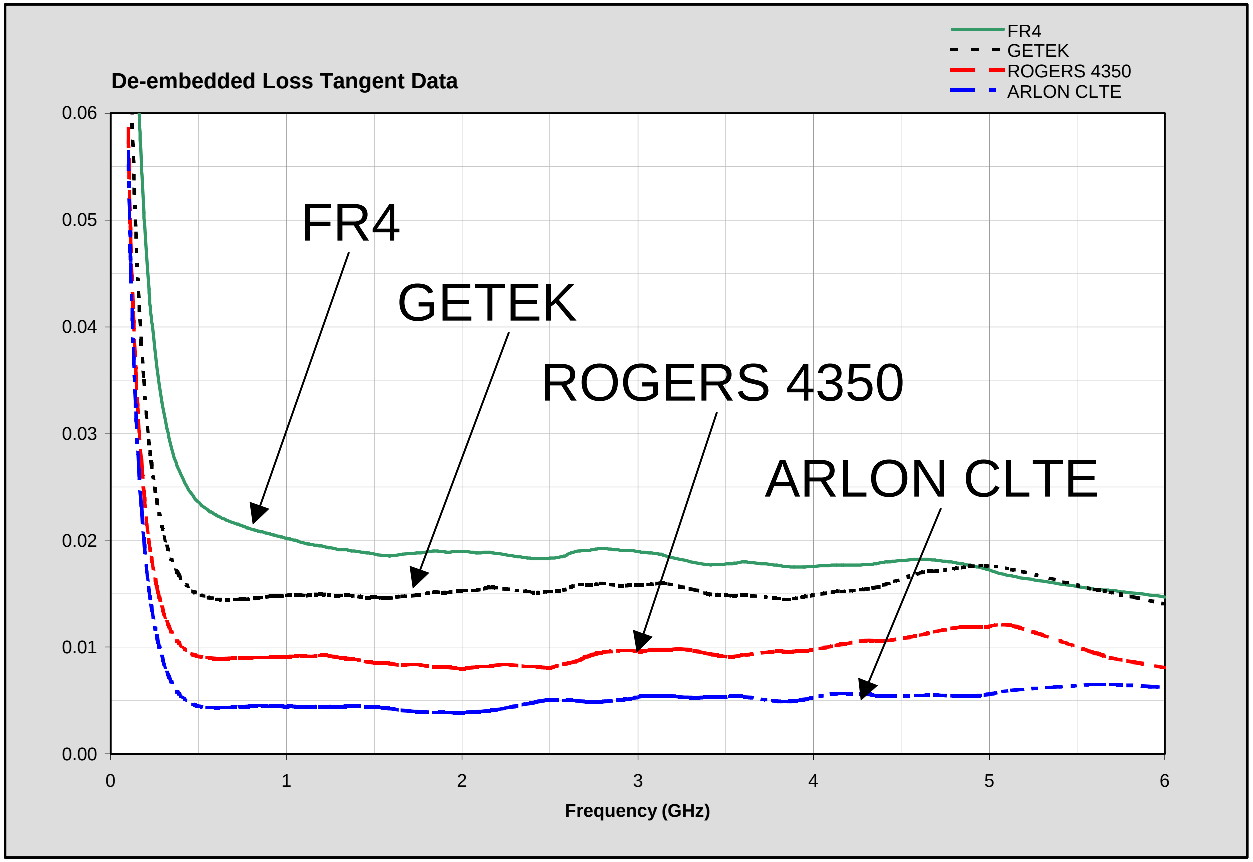
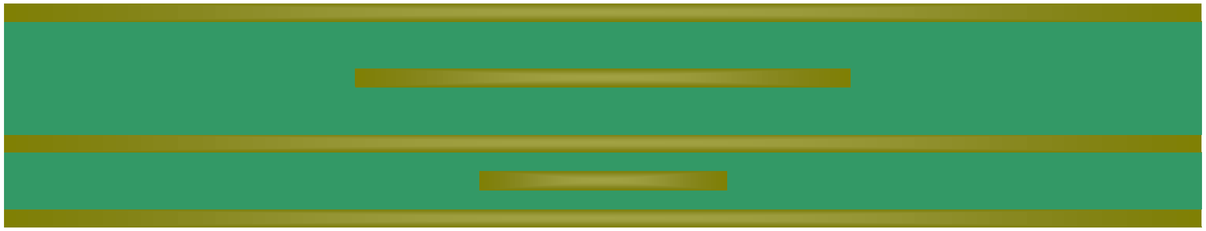
Materials Comparison

- Loss tangent (tanδ) vs. frequency



PWB Stripline Performance

- From measured data
  - Frequency domain
  - Test points de-embedded
- Multiple trace widths
- Multiple trace lengths

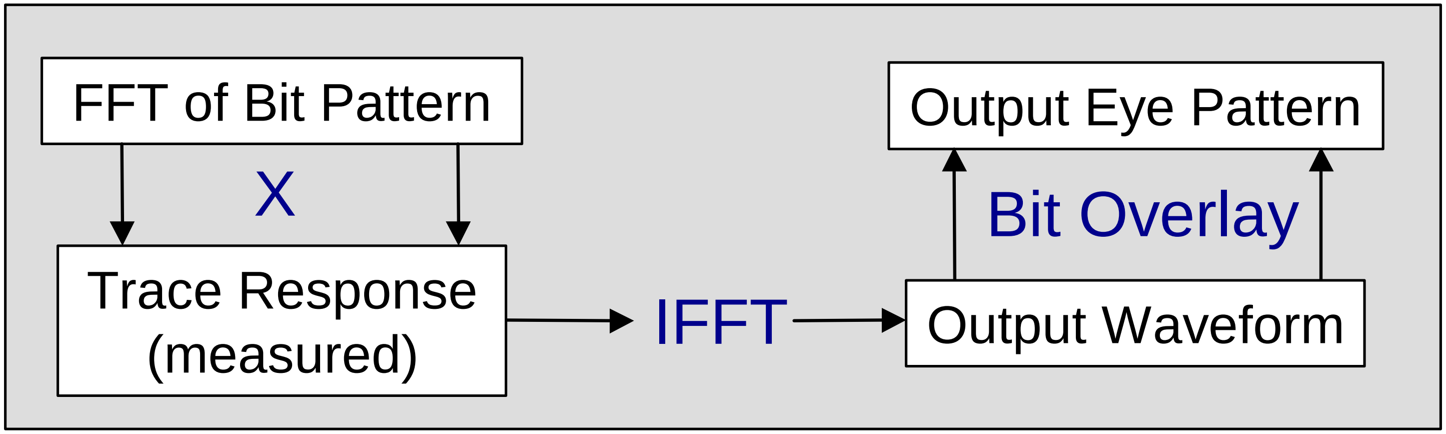


Design Gains Due to Materials

- Trace width
  - 5 mil ROGERS 4350 trace performance equates to that of 12 mil FR4 trace
  - Higher system trace densities can be achieved using alternate materials
- Trace length
  - 24” ARLON CLTE trace performance equates to that of 12” FR4 trace
  - Increased system lengths improve design flexibility

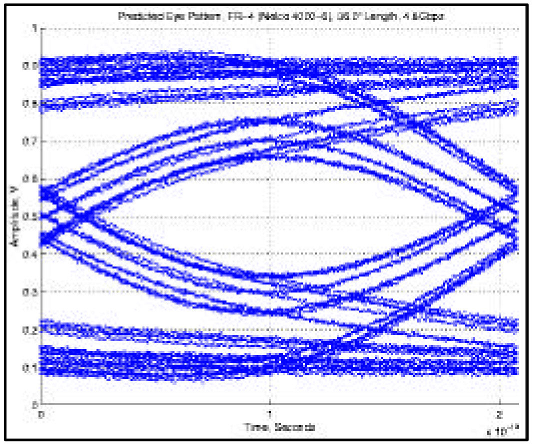
Generating Trace Eye Patterns

- Frequency data used to generate time-domain response without test points
- Higher frequency S-parameters enable higher speed time-domain results

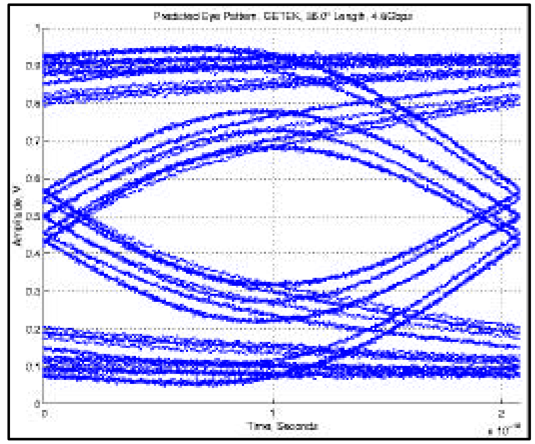


Trace Eye Patterns (4.8 Gbps, 36”)

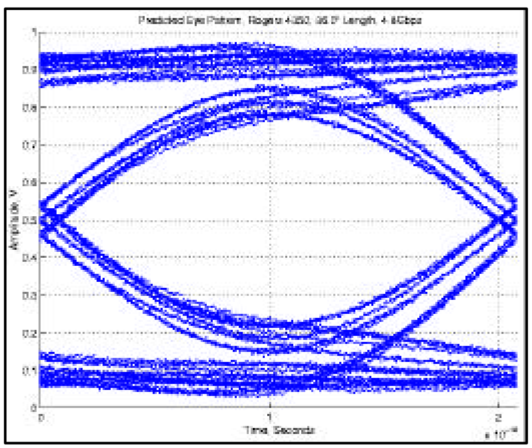
FR4



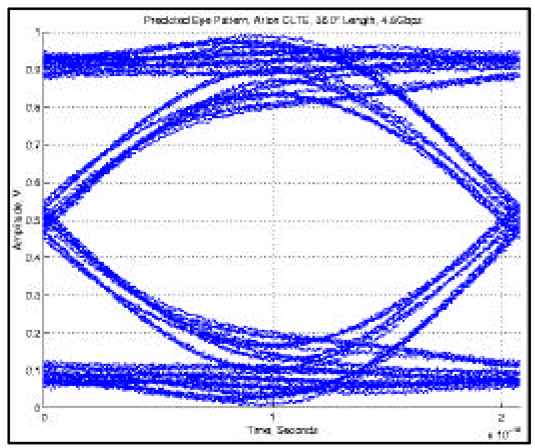
GETEK



ROGERS 4350



ARLON CLTE



<u>FR4:</u>
Jitter = 0.23 UI
Opening = 289 mV

<u>GETEK:</u>
Jitter = 0.21 UI
Opening = 336 mV

<u>ROGERS 4350:</u>
Jitter = 0.11 UI
Opening = 532 mV

<u>ARLON CLTE:</u>
Jitter = 0.10 UI
Opening = 614 mV

-The output waveforms shown result from a 1-volt, 32-bit inverting K28.5 input bit pattern (4.8 Gbps, 60ps edges) that is applied to a 12 mil, 50 Ohm stripline trace that is 36” long.

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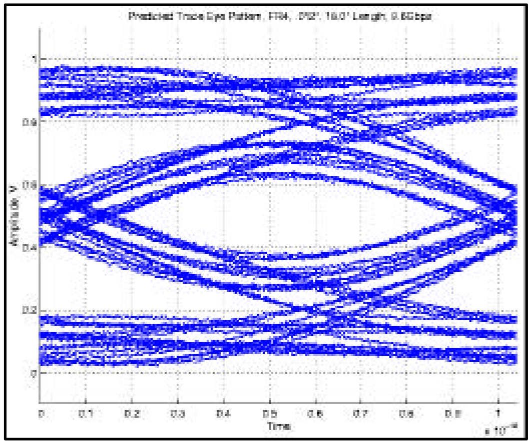
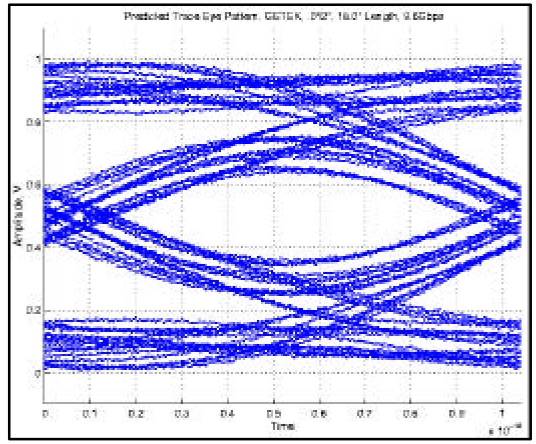
Trace Eye Patterns (9.6 Gbps, 18”)

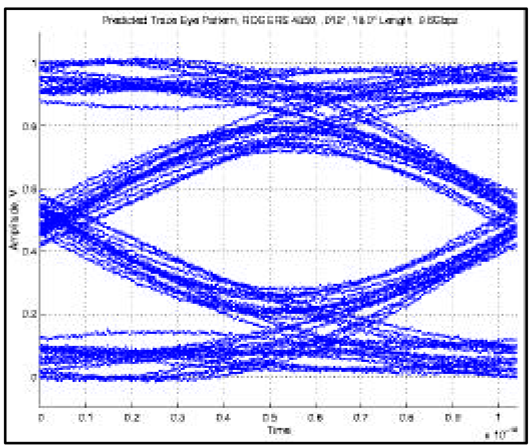
FR4



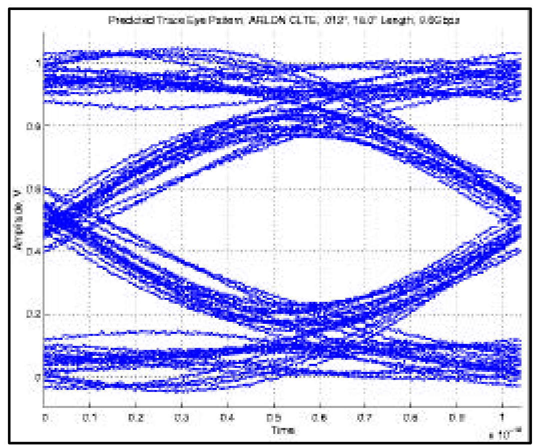
GETEK



ROGERS 4350



ARLON CLTE



FR4:
Jitter = 0.30 UI
Opening = 238 mV

GETEK:
Jitter = 0.28 UI
Opening = 268 mV

ROGERS 4350:
Jitter = 0.20 UI
Opening = 426 mV

ARLON CLTE:
Jitter = 0.19 UI
Opening = 520 mV

-The output waveforms shown result from a 1-volt, 32-bit inverting K28.5 input bit pattern (9.6 Gbps, 60ps edges) that is applied to a 12 mil, 50 Ohm stripline trace that is 18” long.

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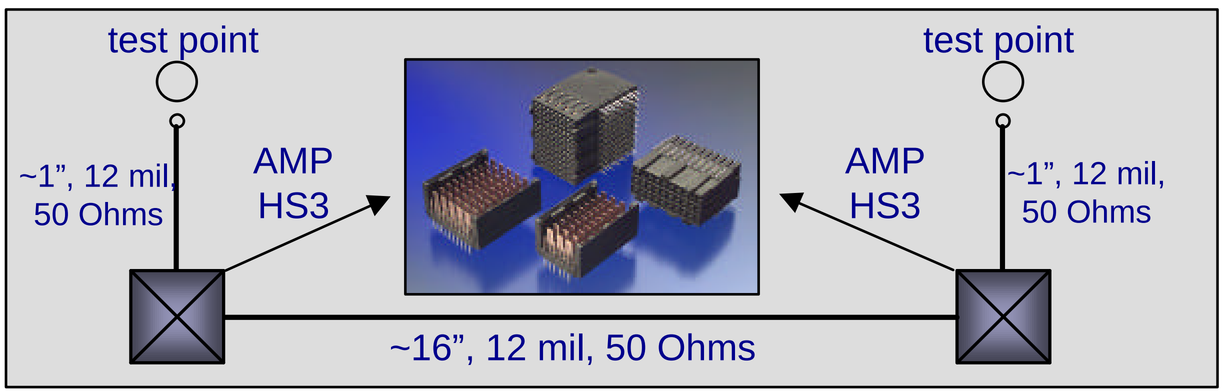
The Interconnect Path

- System analysis must consider the entire interconnect
- Connector and through-hole impact
  - Impedance mismatches (ringing)
  - Resonance due to structure lengths
  - Mode coupling and crosstalk



Measured System Eye Pattern

- Project Background
- Test Board Description
- Materials Review
- Data Review
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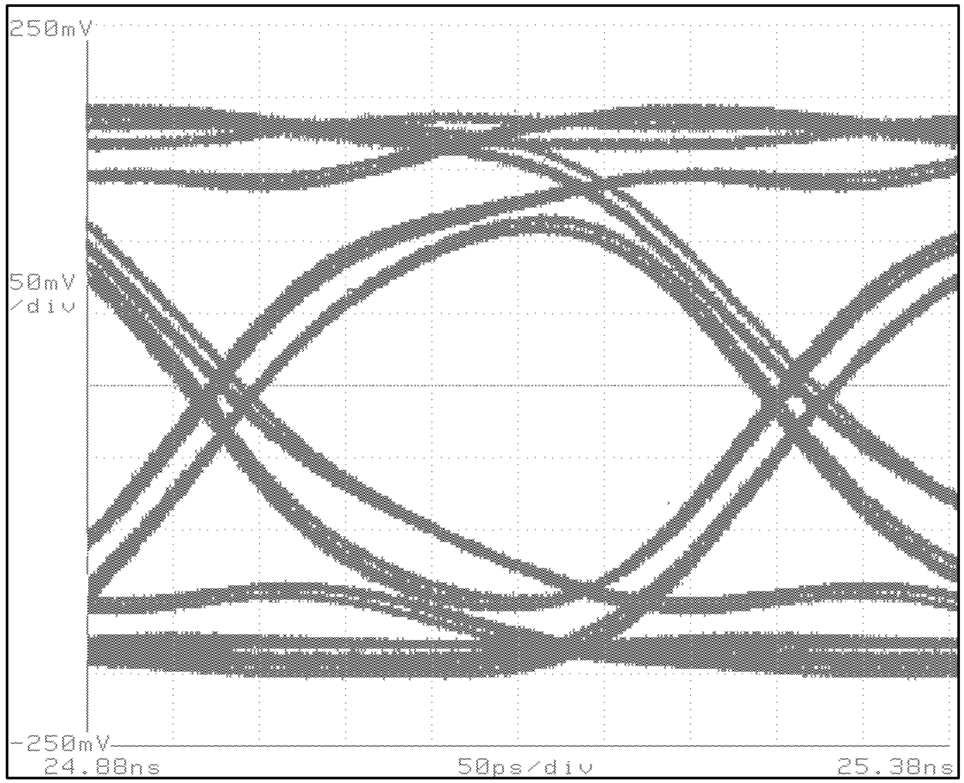
  - System
- Conclusions

- FR4 System: 12 mil, 18” trace at 3 Gbps



-The output waveform shown results from a +/- 200 mV, 32-bit inverting K28.5 input bit pattern (3 Gbps, 60ps edges) that is applied to a system with two through-holes, two AMP HS3 connectors, and a 12 mil, 50 Ohm stripline trace in FR4 that is ~18” long (shown on slide 28).

Simulated System Eye Pattern

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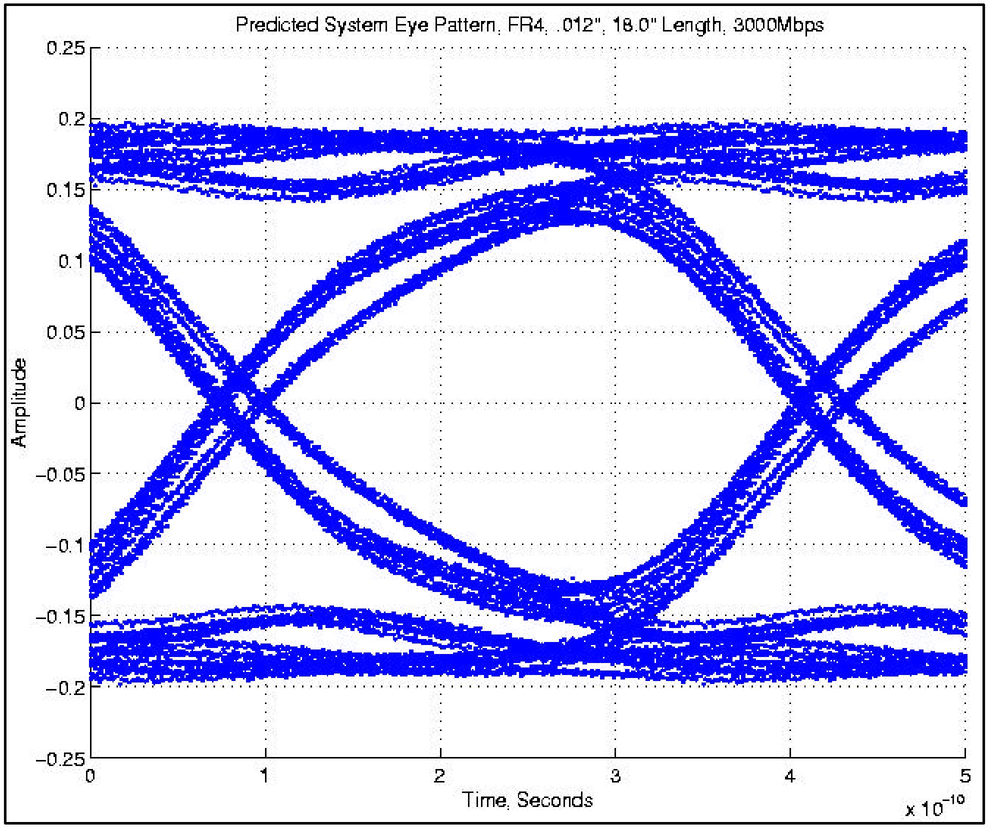
- FR4 System: 12 mil, 18” trace at 3 Gbps



-The output waveform shown results from a +/- 200 mV, 32-bit inverting K28.5 input bit pattern (3 Gbps, 60ps edges) that is applied to a system with two through-holes, two AMP HS3 connectors, and a 12 mil, 50 Ohm stripline trace in FR4 that is ~18” long (shown on slide 28).

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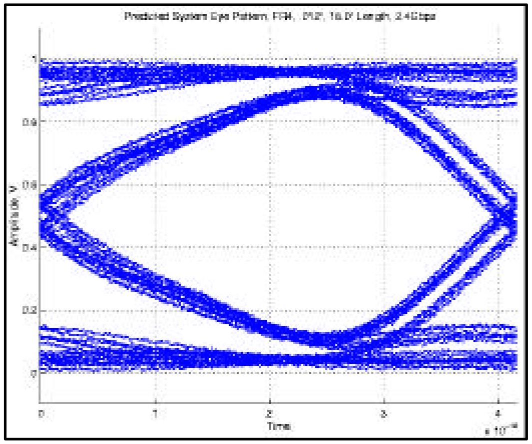
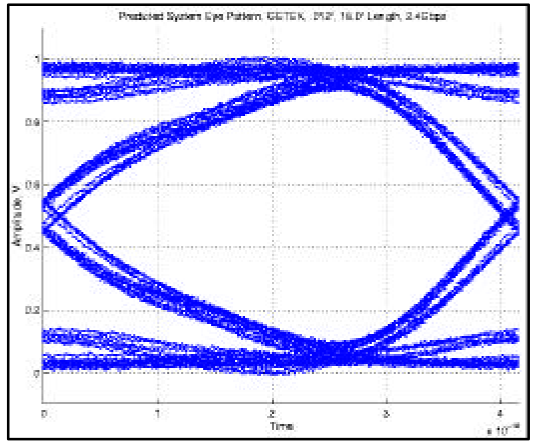
System Eye Patterns (2.4 Gbps, 18”)

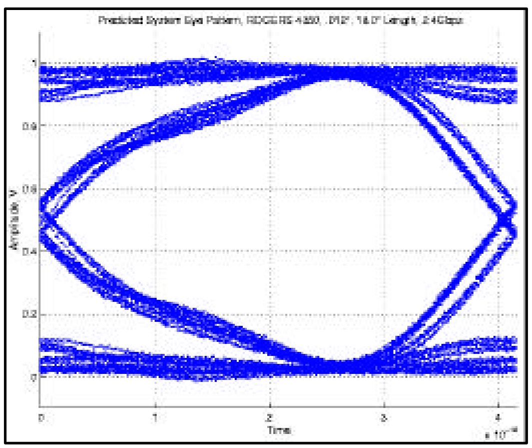
FR4



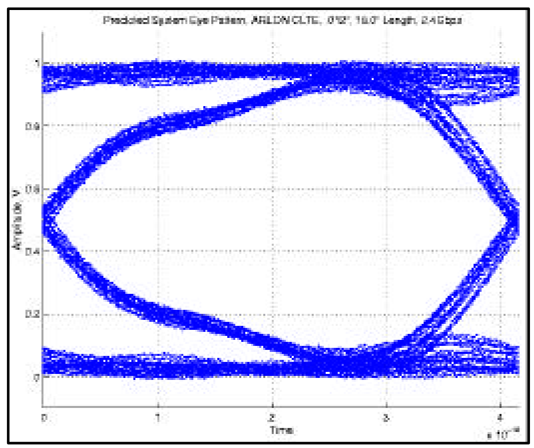
GETEK



ROGERS 4350



ARLON CLTE



FR4:
Jitter = 0.11 UI
Opening = 733 mV

GETEK:
Jitter = 0.09 UI
Opening = 790 mV

ROGERS 4350:
Jitter = 0.07 UI
Opening = 896 mV

ARLON CLTE:
Jitter = 0.05 UI
Opening = 820 mV

-The output waveforms shown result from a 1-volt, 32-bit inverting K28.5 input bit pattern (2.4 Gbps, 60ps edges) that is applied to a system with two through-holes, two AMP HS3 connectors, and a 12 mil, 50 Ohm stripline trace that is ~18” long.

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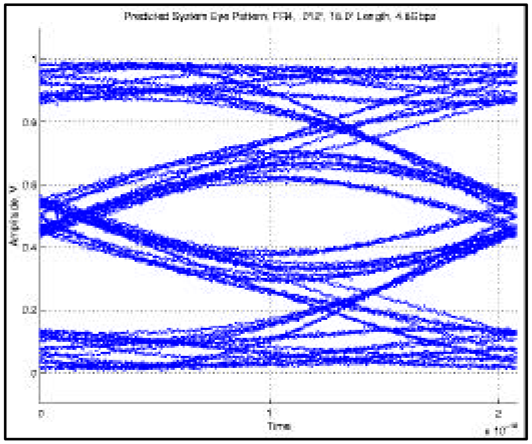
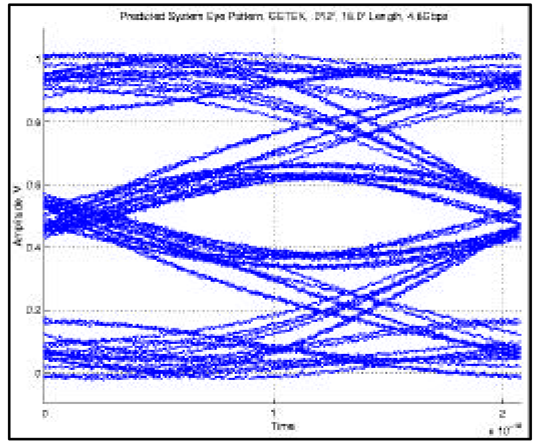
System Eye Patterns (4.8 Gbps, 18”)

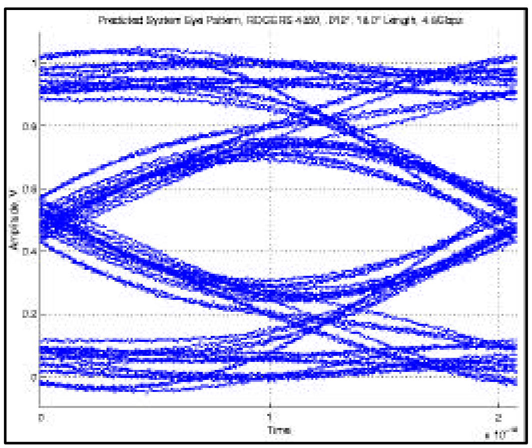
FR4



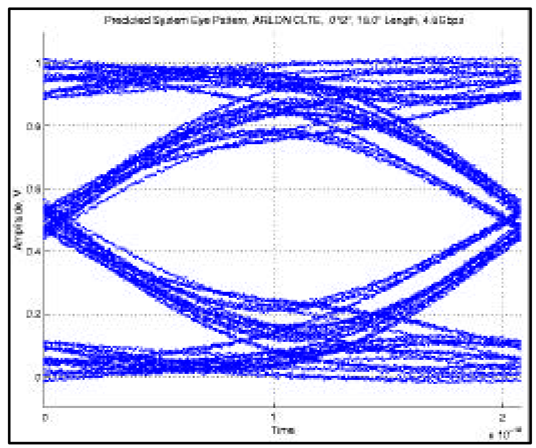
GETEK



ROGERS 4350



ARLON CLTE



FR4:
Jitter = 0.25 UI
Opening = 218 mV

GETEK:
Jitter = 0.24 UI
Opening = 227 mV

ROGERS 4350:
Jitter = 0.19 UI
Opening = 378 mV

ARLON CLTE:
Jitter = 0.12 UI
Opening = 516 mV

-The output waveforms shown result from a 1-volt, 32-bit inverting K28.5 input bit pattern (4.8 Gbps, 60ps edges) that is applied to a system with two through-holes, two AMP HS3 connectors, and a 12 mil, 50 Ohm stripline trace that is ~18” long.

System Eye Patterns (9.6 Gbps, 18”)

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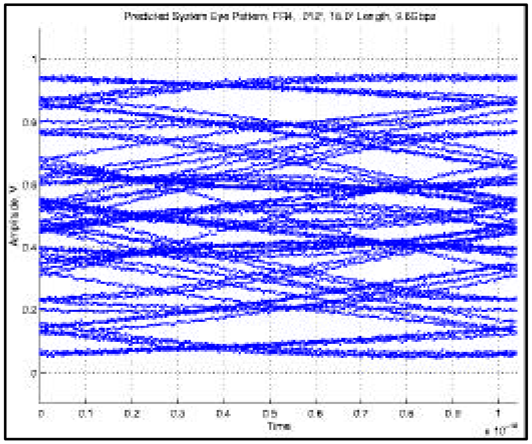
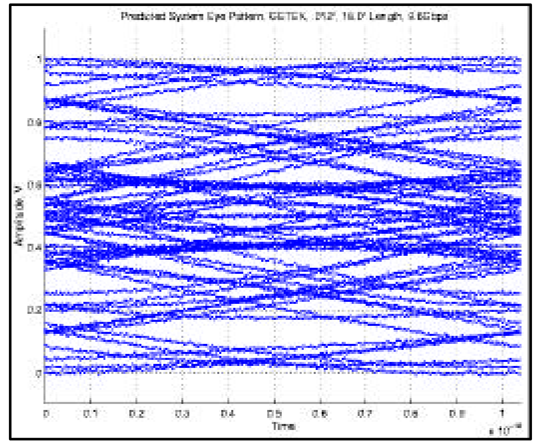
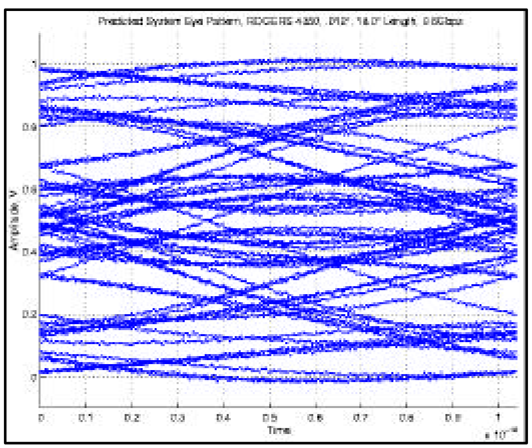
FR4



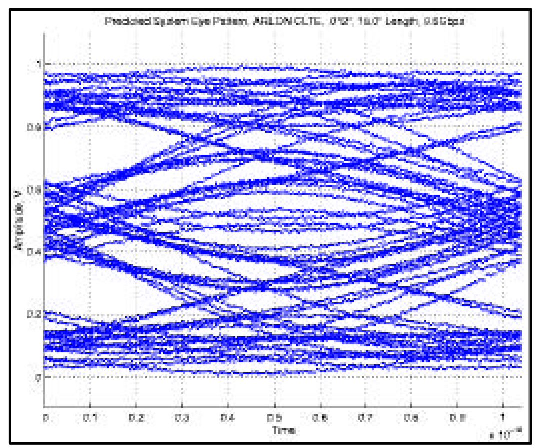
GETEK



ROGERS 4350



ARLON CLTE



All Materials:

Zero Crossover jitter is indistinguishable

The eye is closed (no open amplitude)

-The output waveforms shown result from a 1-volt, 32-bit inverting K28.5 input bit pattern (9.6 Gbps, 60ps edges) that is applied to a system with two through-holes, two AMP HS3 connectors, and a 12 mil, 50 Ohm stripline trace that is ~18” long.

Trace Eye Patterns (9.6 Gbps, 18”)

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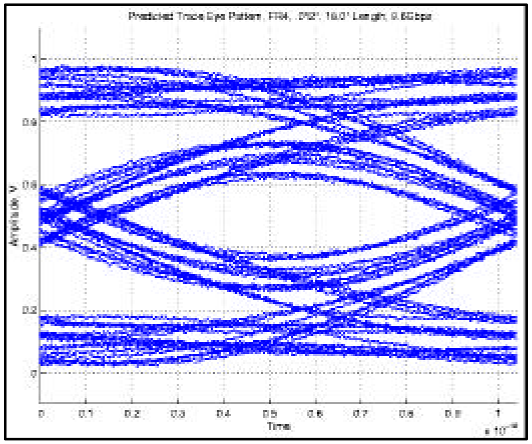
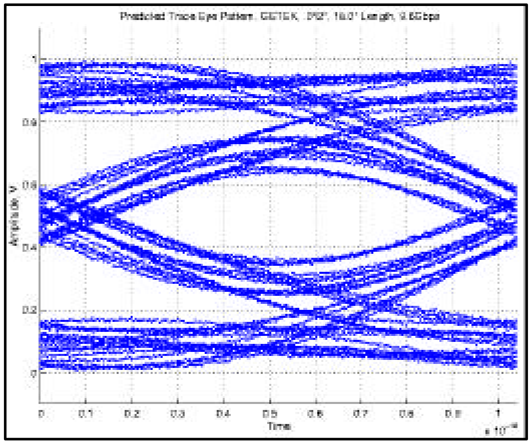
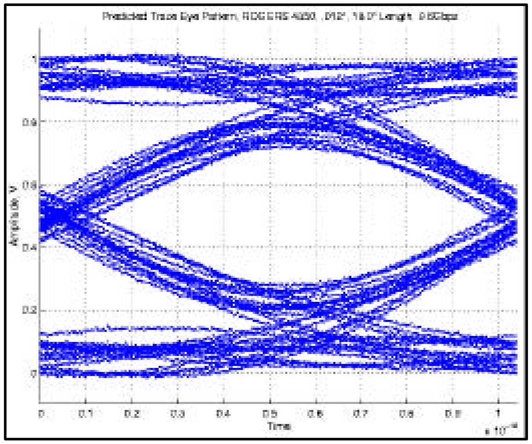
FR4



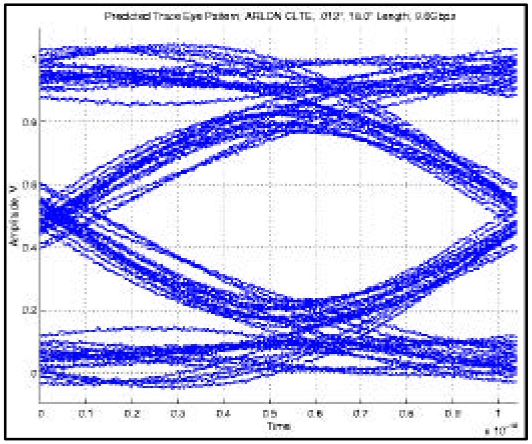
GETEK



ROGERS 4350



ARLON CLTE



FR4:
Jitter = 0.30 UI
Opening = 238 mV

GETEK:
Jitter = 0.28 UI
Opening = 268 mV

ROGERS 4350:
Jitter = 0.20 UI
Opening = 426 mV

ARLON CLTE:
Jitter = 0.19 UI
Opening = 520 mV

-The output waveforms shown result from a 1-volt, 32-bit inverting K28.5 input bit pattern (9.6 Gbps, 60ps edges) that is applied to a 12 mil, 50 Ohm stripline trace that is 18” long.

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Interconnect System Summary

- Interconnection assumptions:
  - 50 Ω stripline trace (12 mils, 18”)
  - 2 HS3 connectors and minimal vias
- Results summary:
  - @ 2.4 Gbps performance in all materials should be acceptable
  - @ 4.8 Gbps
    - System analysis required
    - Alternate materials could make the difference
  - @ 9.6 Gbps
    - Alternate interconnect technology required
    - Improved materials required
    - System analysis critical

Conclusions

Project Background → Test Board Description → Materials Review → Data Review (Materials, Traces, System) → **Conclusions**

- Materials

  Alternate dielectric materials exist that are manufacturable, cost-effective, and superior in electrical performance.

- PWB structures (traces)

  PWB structures can support substantial future bandwidth requirements using improved dielectric materials.

- Interconnection systems

  Future bandwidth trends require improved interconnection technology and in depth system analysis.

Future Investigations

- Measurements
  - Time-domain testing to 12 Gbps
  - Frequency-domain testing to 50 GHz
  - Further compliant pin force testing
- Technology research
  - Via studies
  - Next generation connector development
  - Advanced modeling techniques

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Conclusions

Recommended Resources

- AMP Circuits & Design

System Analysis → System Design → Prototype Production

- For further information, contact:
  - AMP simulation services - simulation@amp.com
  - AMP modeling services - modeling@amp.com

- Presentation information and additional paper copies can be obtained from:

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