Limits of FR-4 in High-Speed Designs

Dr. Edward Sayre, Mr. Michael Baxter, Dr. Jinhua Chen
NESA
Tel: 978 897-8787 ❖ Fax: 978 897-5359
www.nesa.com ❖ info@nesa.com

The FR-4 Problem in Gigabit Design

- FR-4 is the most common PCB Fabrication material and the most cost effective.
- Fabricators know how to laminate and etch a wide variety of conductor patterns and conditions
- A well known material with UL and other approvals
- Question of the Hour!!!!

How far can Gigabit signals be run on 100 Ω impedance differential etch and at what speeds?

Total RF Transmission Line Loss

$$\frac{Attenuation}{Per\ Unit\ Length}(dB) = 4.35\left[G_d * f * Z_0 + \frac{R_{dc} + R_s\sqrt{f}}{Z_0}\right]$$

Where: G_d = shunt dielectric conductance $[\Omega\ \mathrm{Hz}]^{-1}$
R_s = skin effect series loss $[\Omega(\mathrm{Hz})^{-1/2}]$

Frequency Where Skin Effect Losses Equal Dielectric Losses

$$f_e \equiv \left[\frac{R_s}{G_d} \bullet \frac{1}{Z_0^2} \right]^2$$

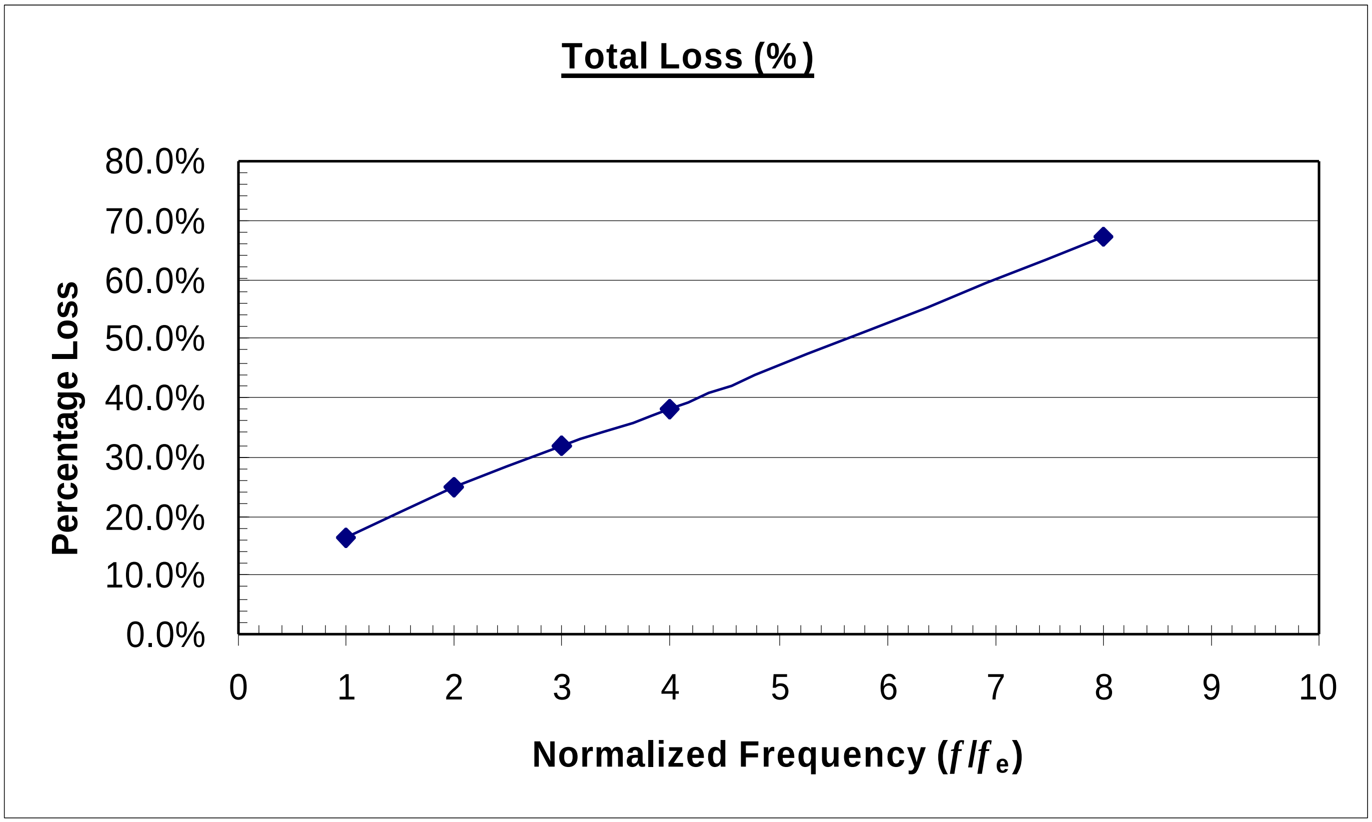
Where: R_s = Skin Effect Resistance [Ω(Hz)$^{-1/2}$]
G_d = Dielectric Shunt Conductance [Ω Hz]$^{-1}$
Z_o = Transmission Line Impedance [Ω]

Typical Values for FR-4 & Common Line Parameters

- Line Width - 8 mil
- Line thickness - 1 oz Cu (1.4 mils)
- Differential Impedance Z_o = 100 Ω
- FR-4 Dielectric Constant = 4.5
- FR-4 Loss Tangent = 0.021 (assumed constant)

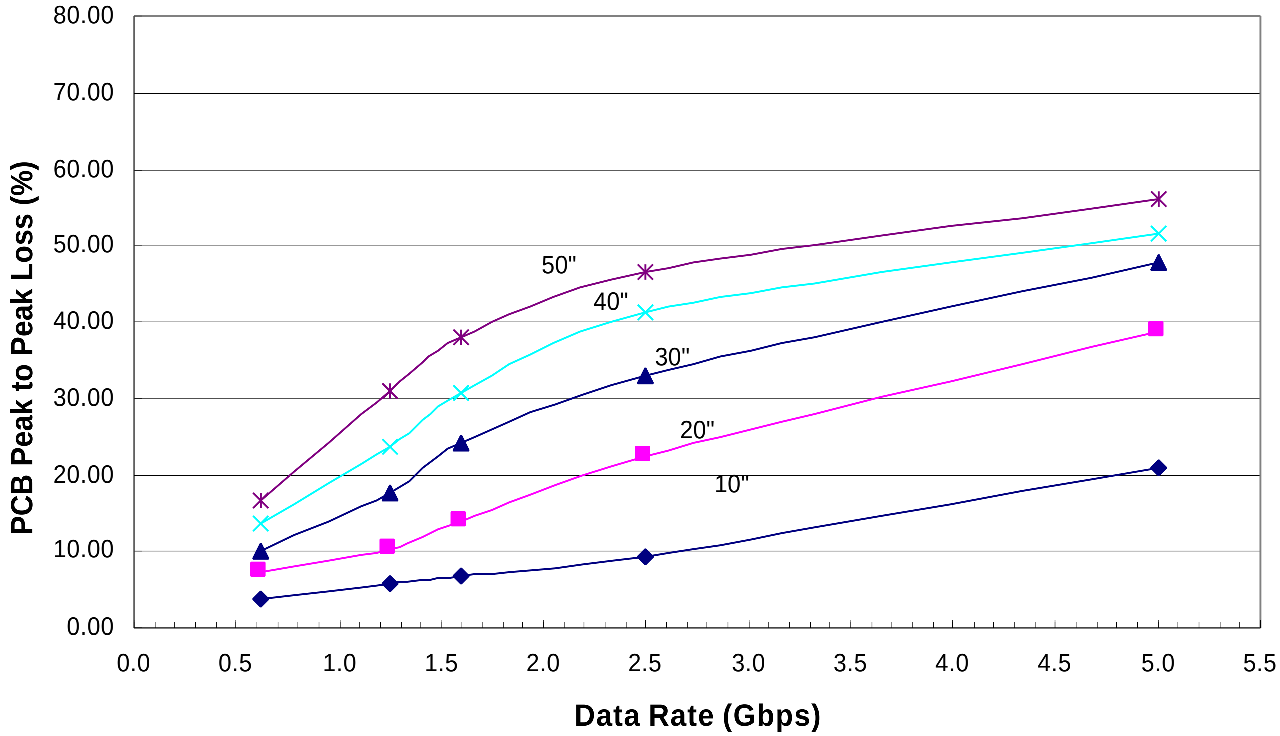
- Skin Loss = Dielectric Loss at f_e = 205 MHz

RF Total Loss vs. Normalized Frequency



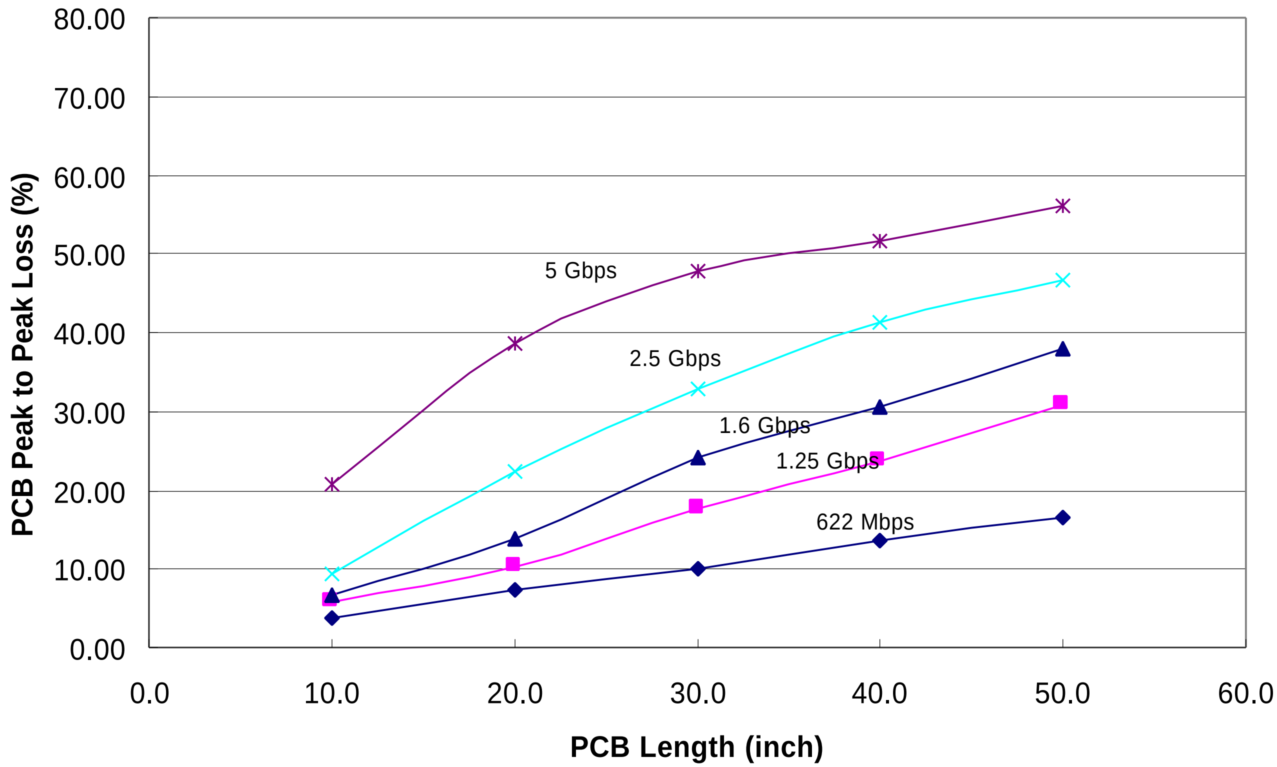
100 W Differential PCB

percentage peak to peak loss as the function of
data rate, PCB lengths from 10” to 50” with 8 mil line width



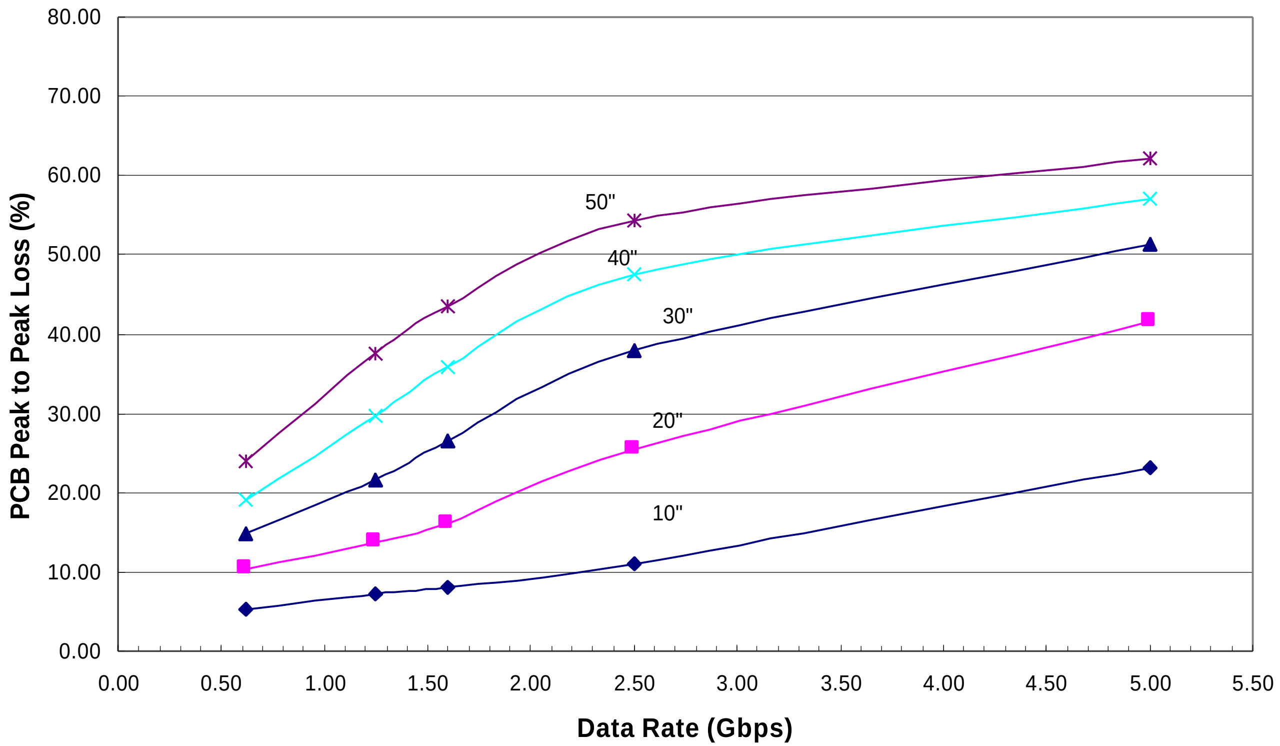
100 W Differential PCB

percentage peak to peak loss as the function of
PCB length with 8 mil line width



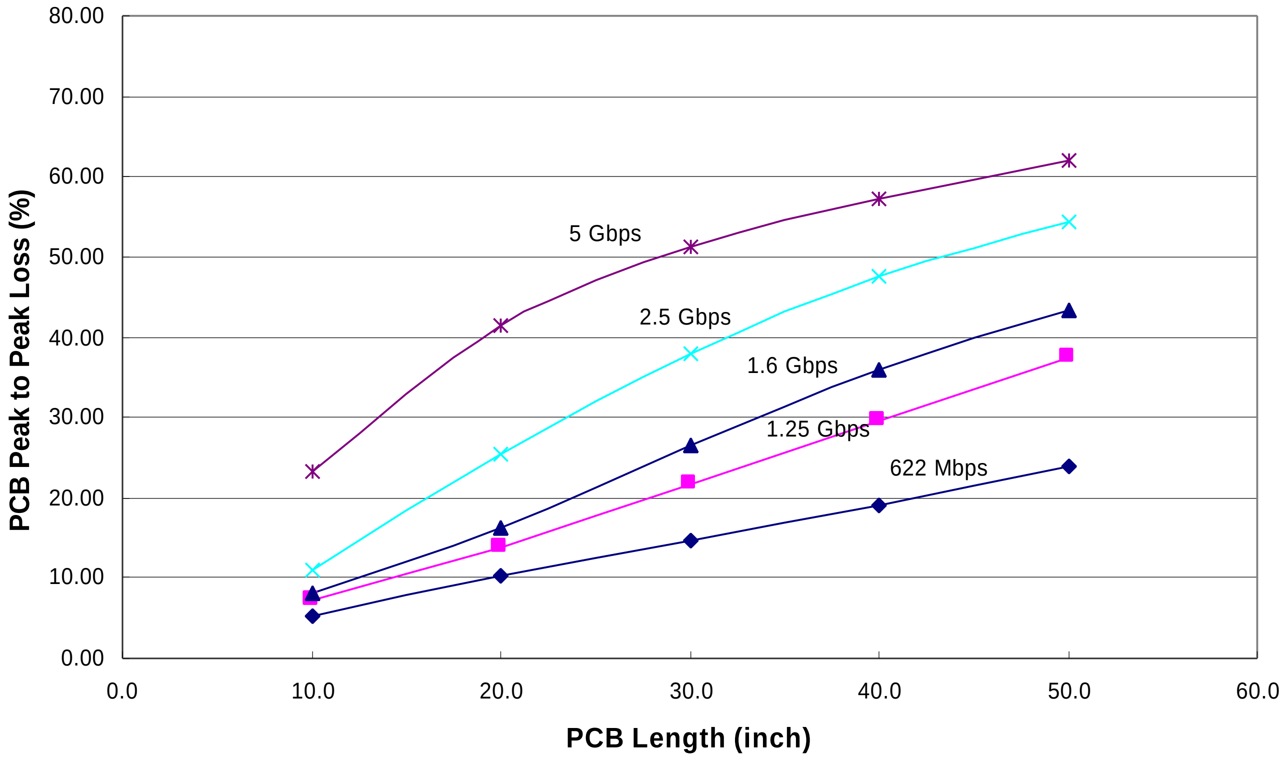
100 W Differential PCB

percentage peak to peak loss as the function of
data rate, PCB lengths from 10” to 50” with 6 mil line width



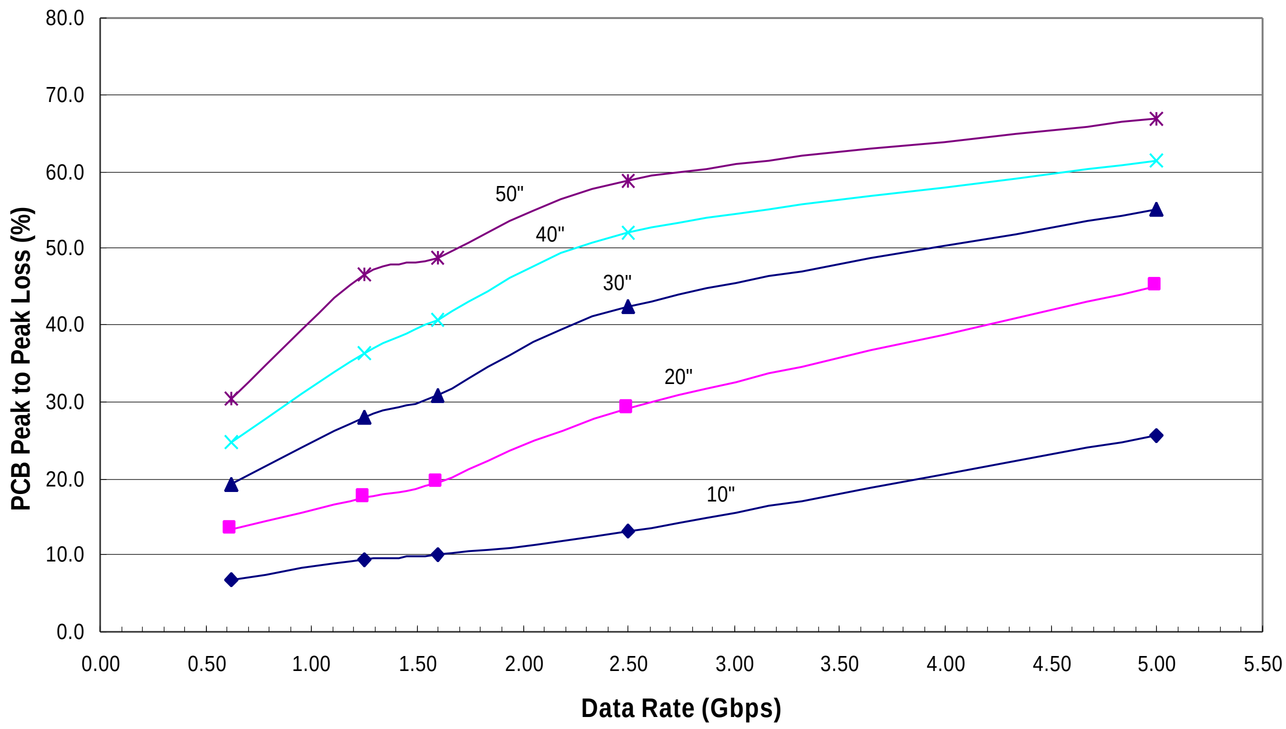
100 W Differential PCB

percentage peak to peak loss as the function of
PCB length with 6 mil line width



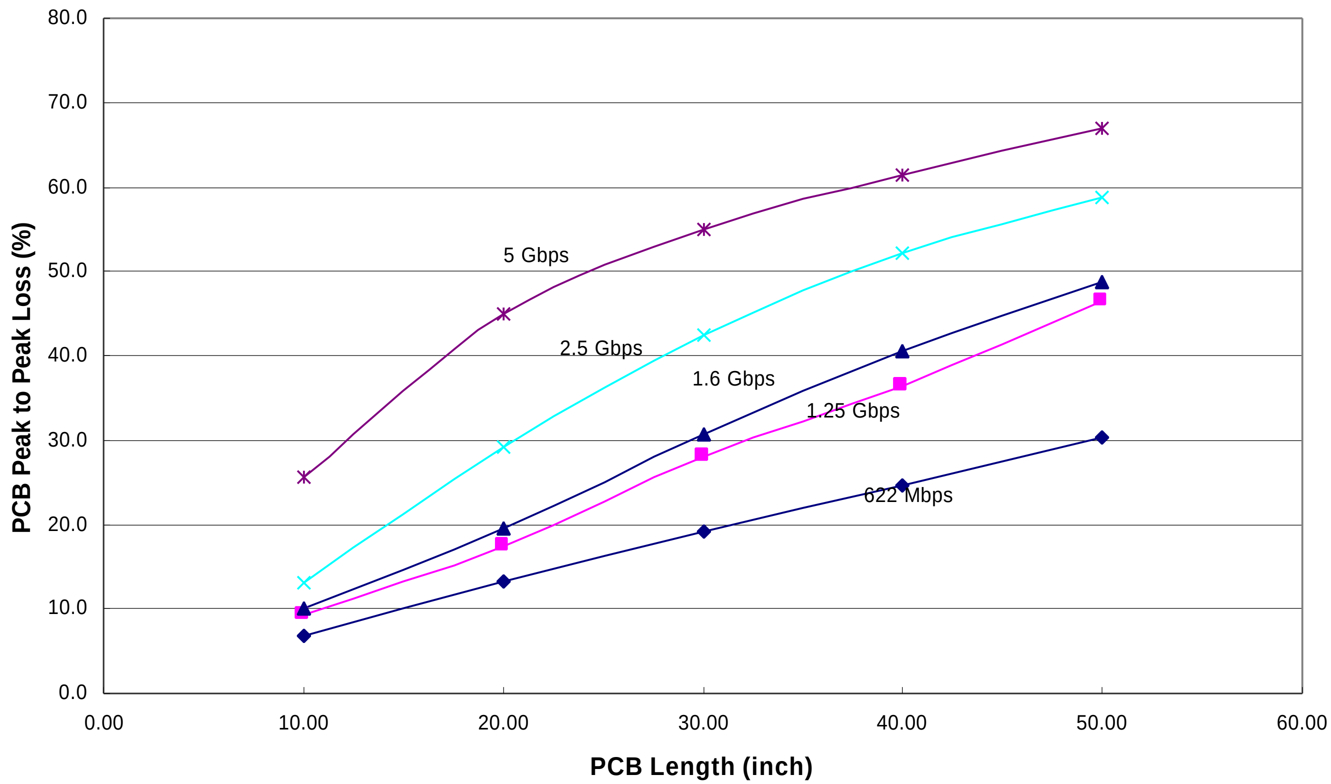
100 W Differential PCB

percentage peak to peak loss as the function of
data rate, PCB lengths from 10” to 50” with 4 mil line width



100 W Differential PCB

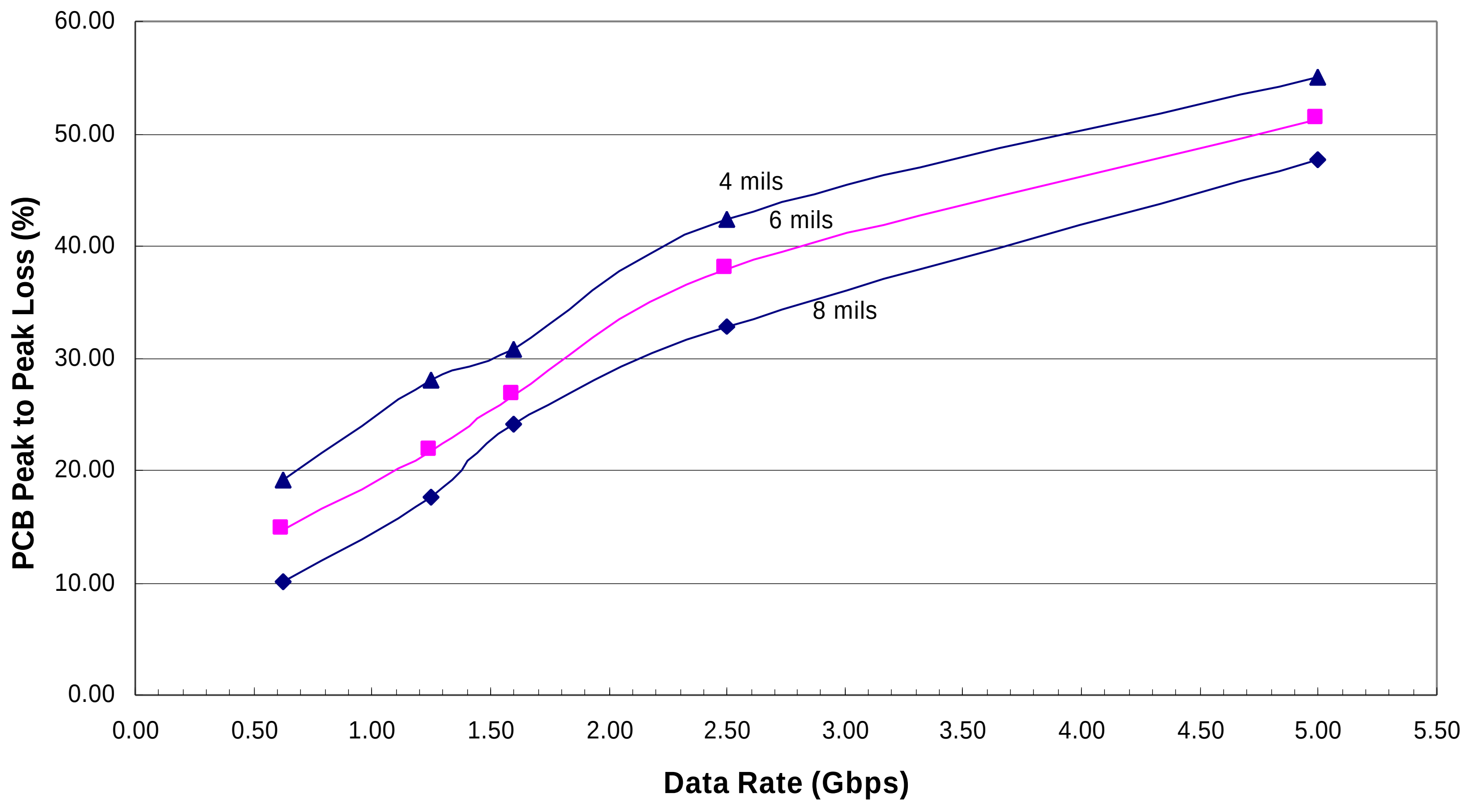
percentage peak to peak loss as the function of
PCB length with 4 mil line width



Successful Design of OC-48/2.5Gbps Interconnects

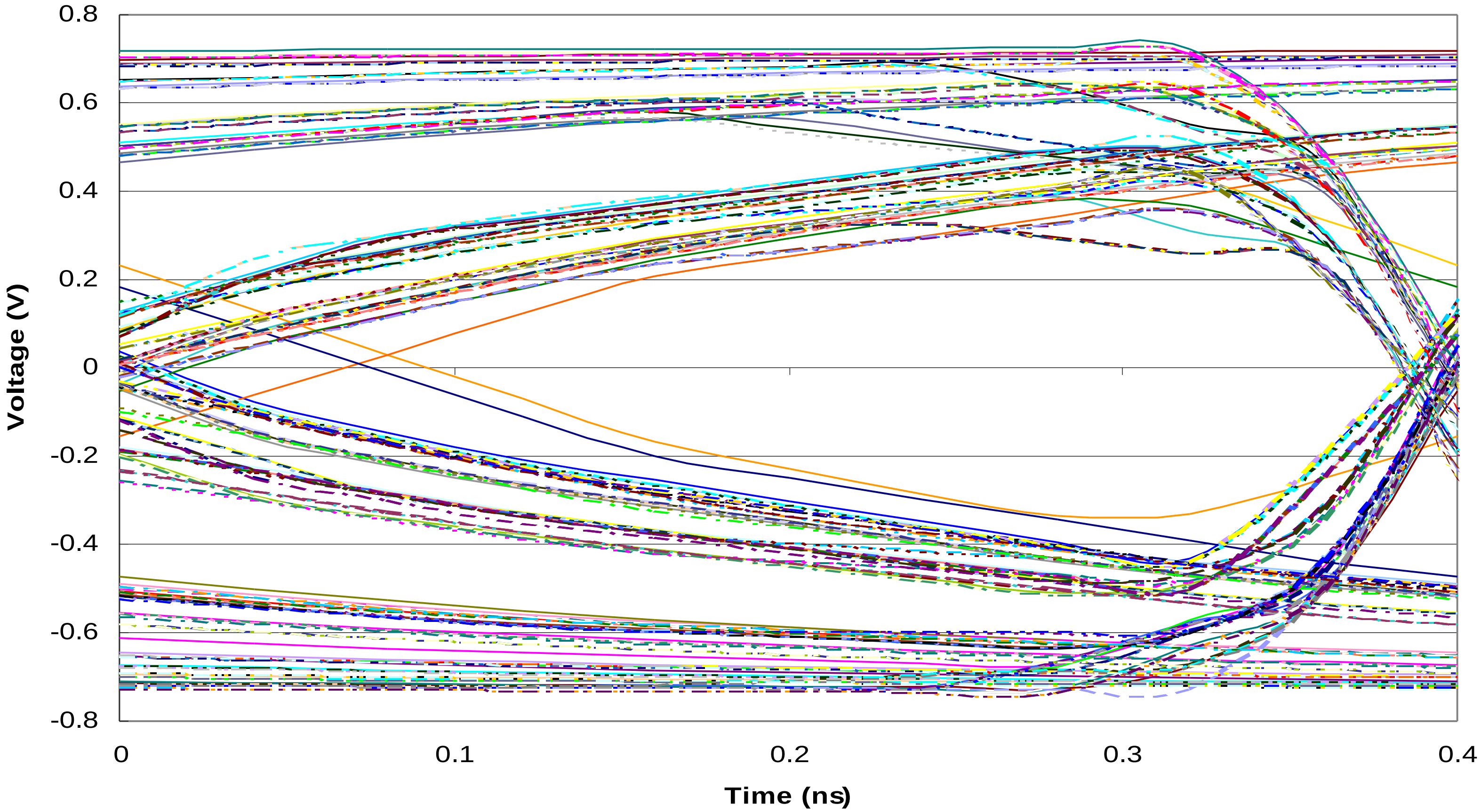
100 W Differential PCB

percentage peak to peak loss as the function of data rate
30" traces with 4, 6 and 8 mil line width



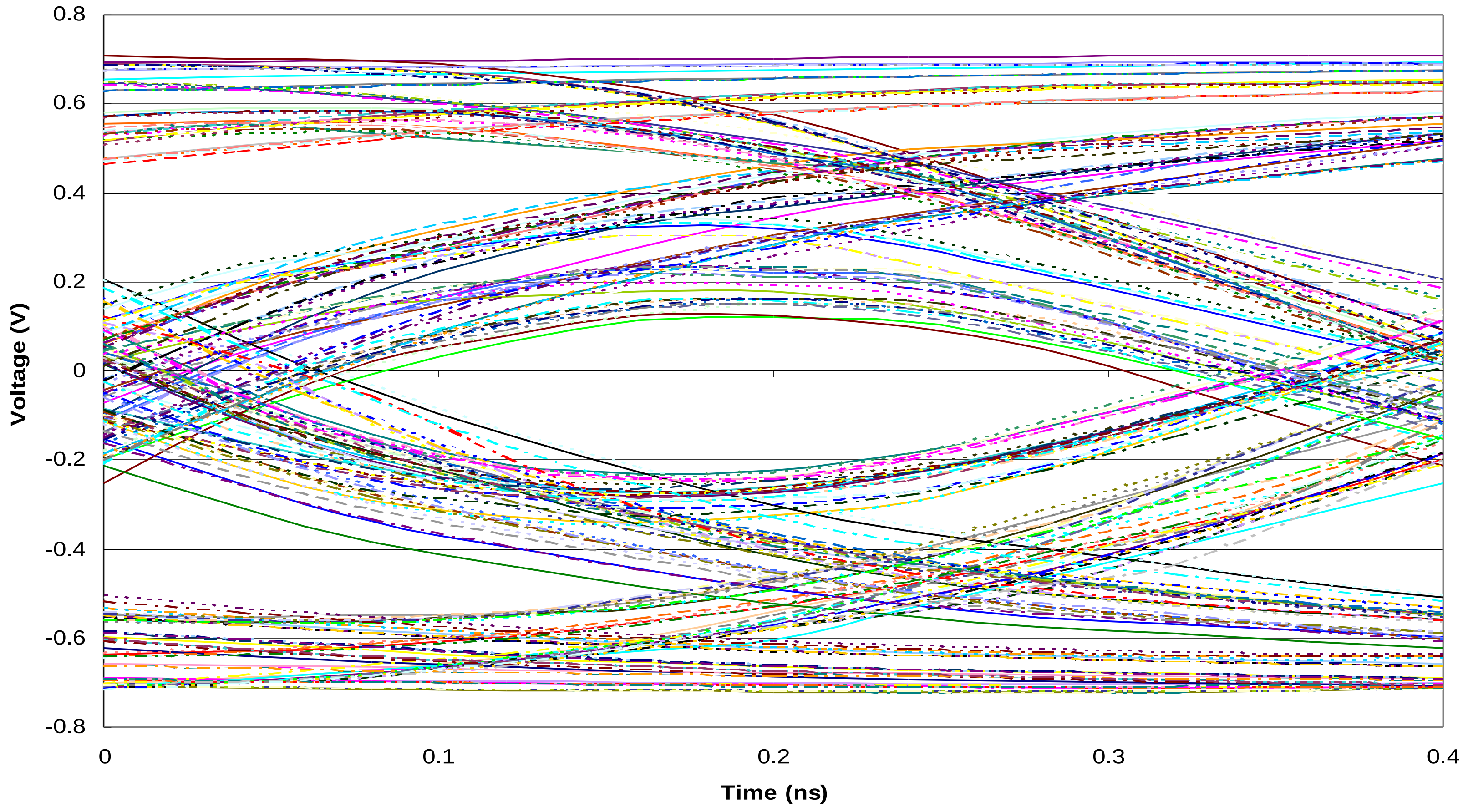
Simulated 2.5 Gbps Eye Pattern

skin effect + dielectric loss (FR-4 loss tangent 0.021) for 40” trace



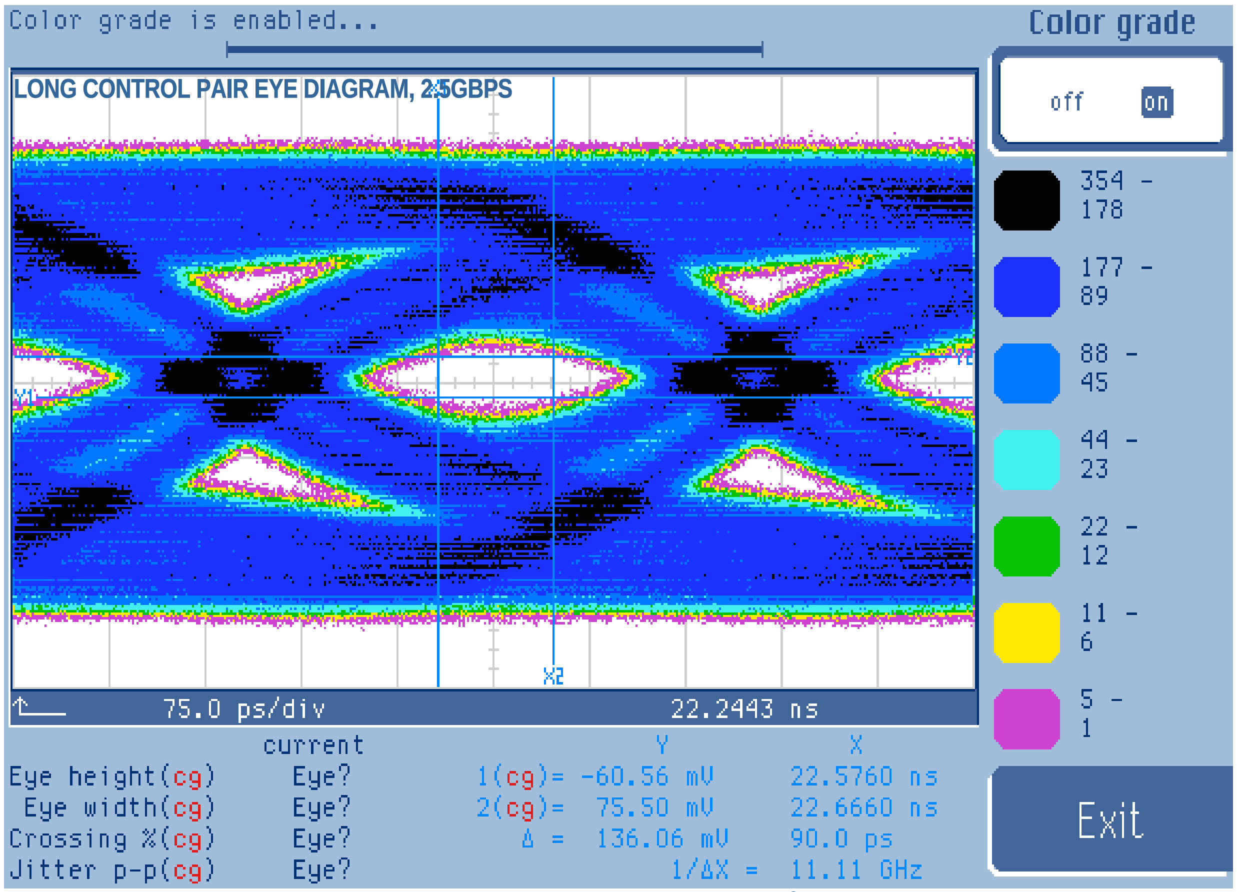
Simulated 2.5 Gbps Eye Pattern

skin effect + dielectric loss for 40” trace with two backplane connectors



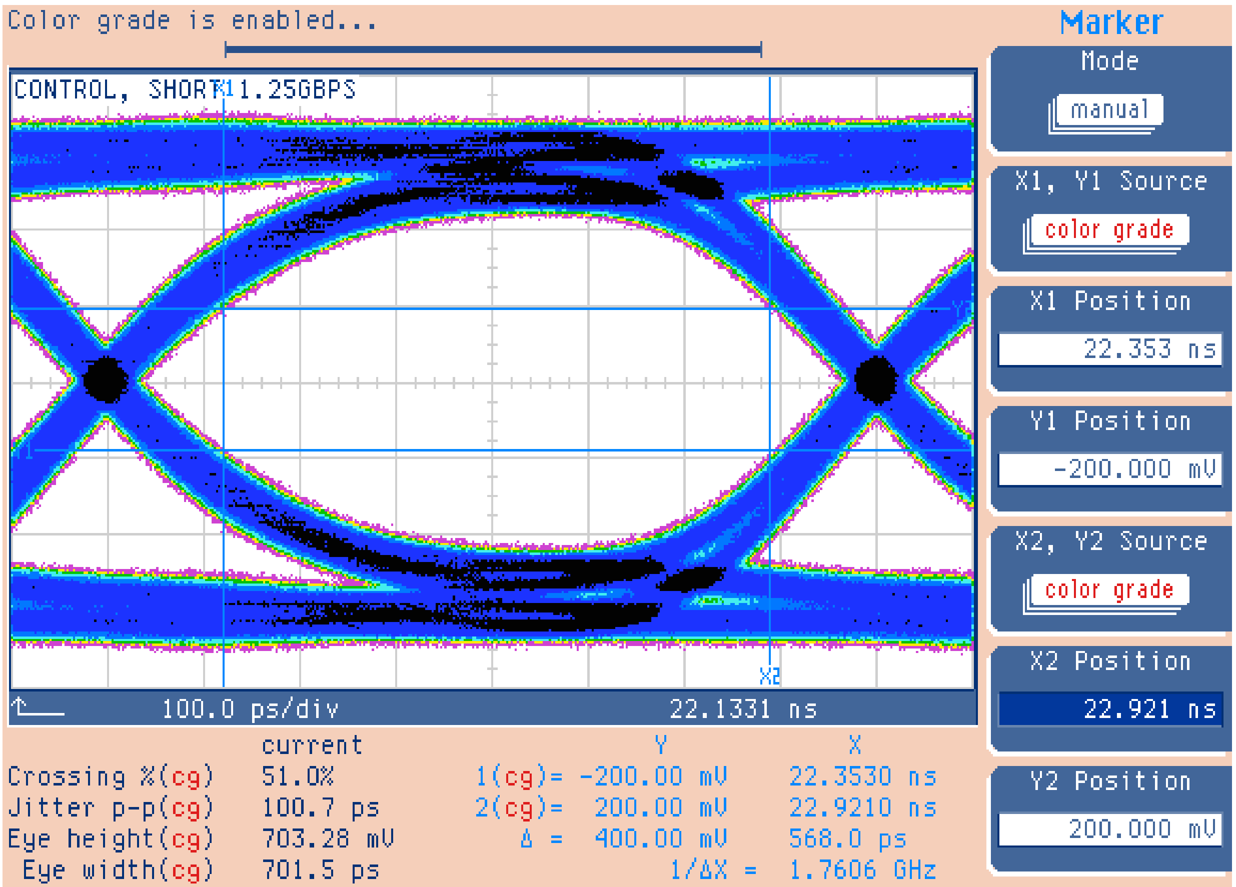
Measured 2.5 Gbps Eye Pattern

skin effect + dielectric loss for 40” trace with two backplane connectors



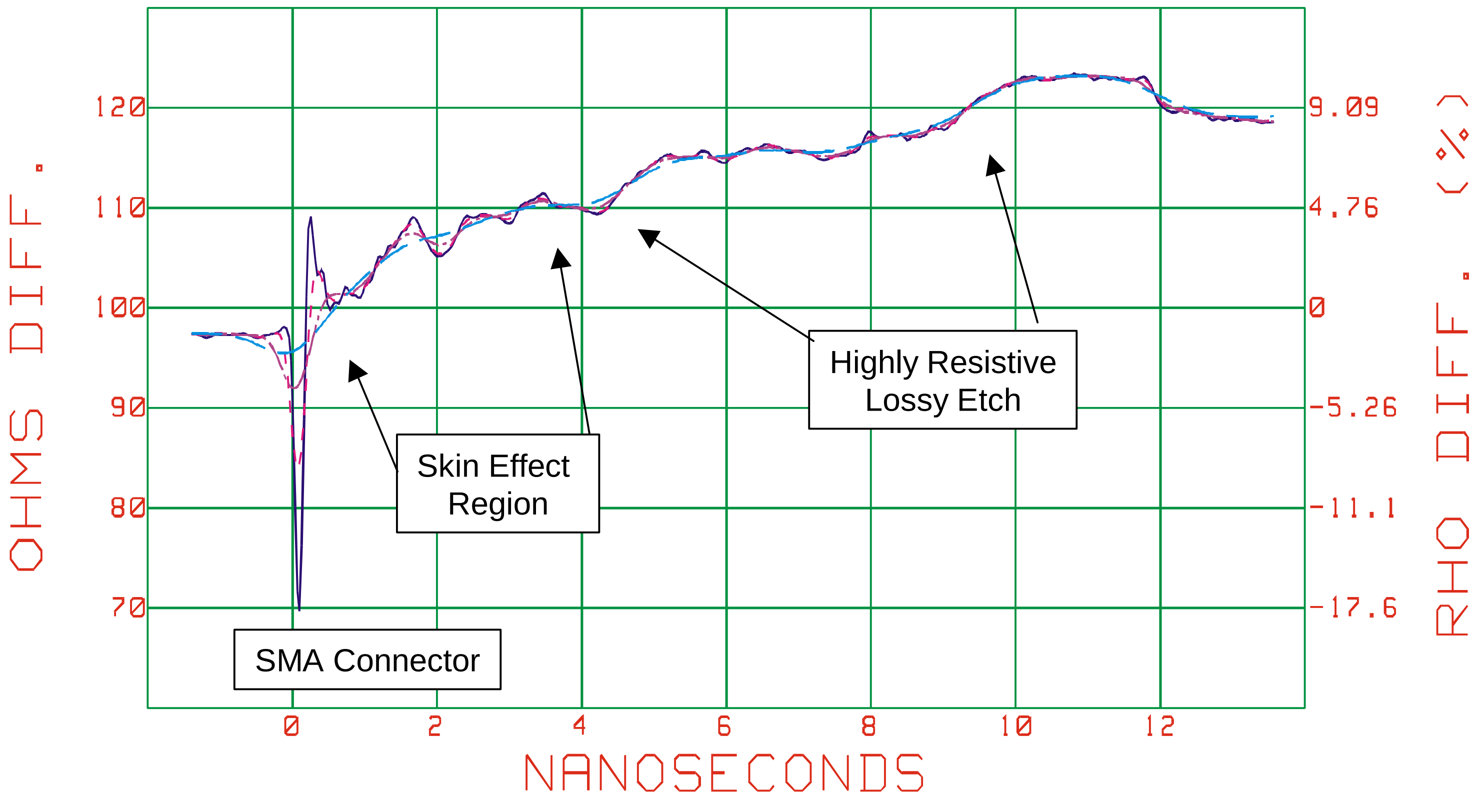
Differential 1.25 Gbps Eye Pattern

23” trace including two backplane connectors



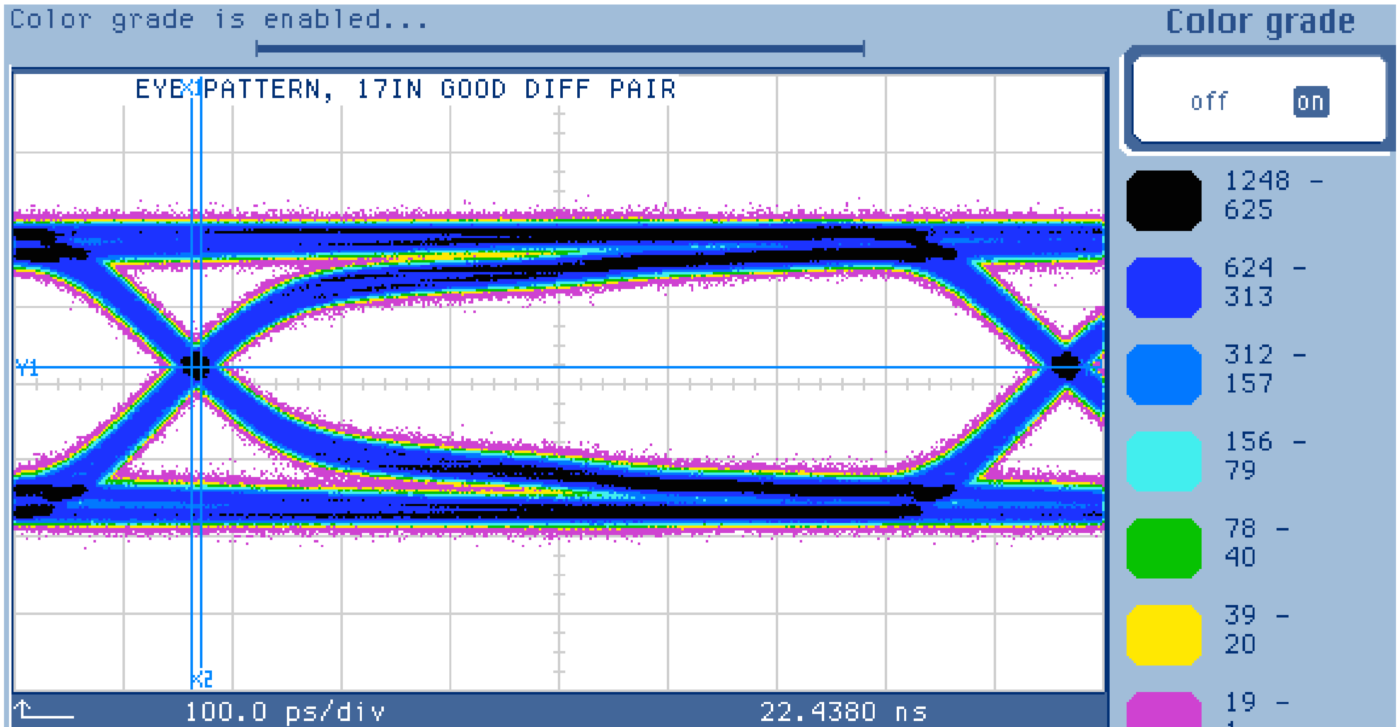
Poor Fabrication Results

Differential TDR vs. Risetime



1.25 Gbps Eye Pattern

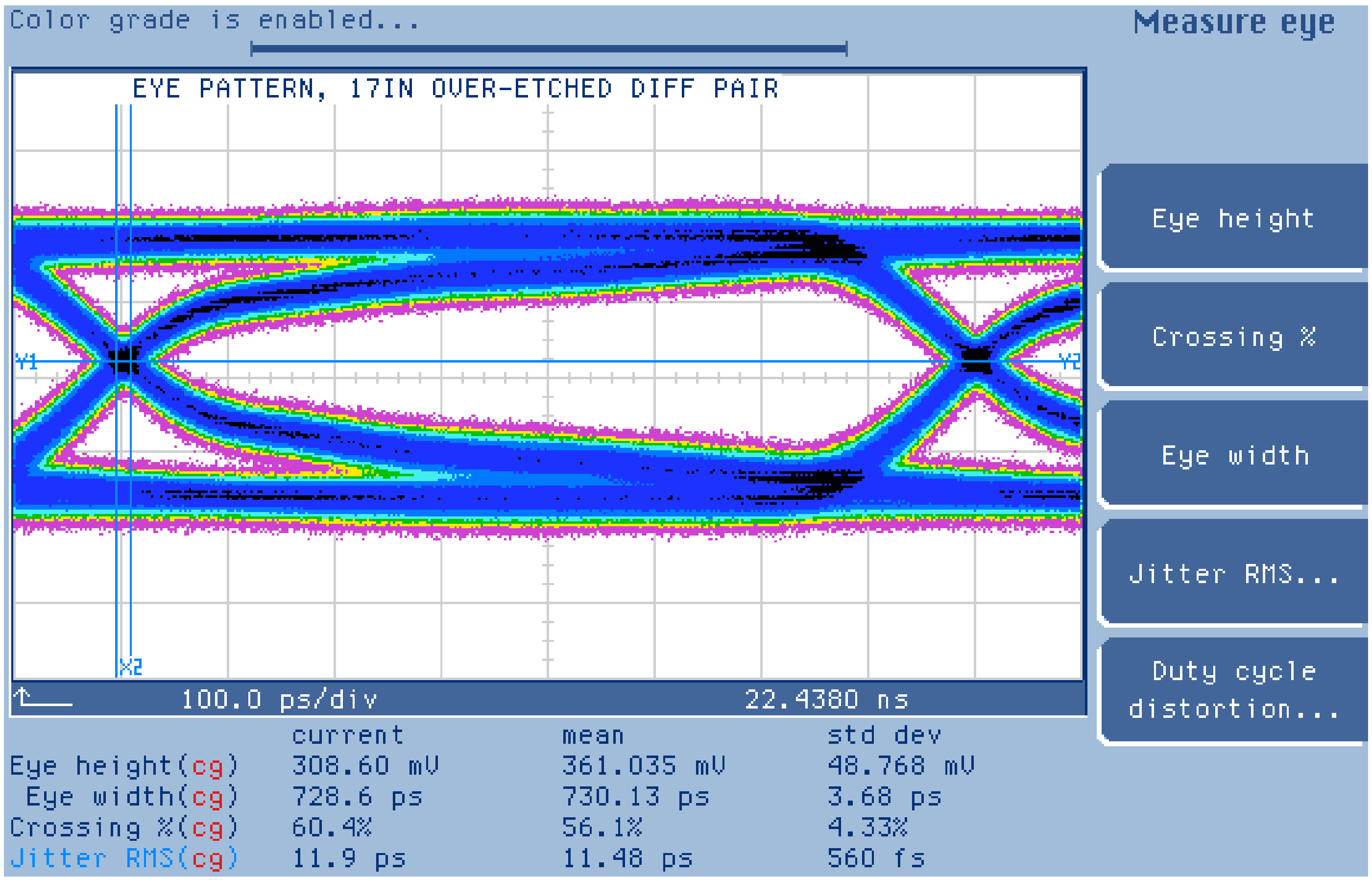
properly etched differential pair



	current	mean	std dev
Eye height(cg)	409.94 mV	458.023 mV	44.061 mV
Eye width(cg)	733.4 ps	737.69 ps	3.56 ps
Crossing %(cg)	52.2%	52.5%	1.35%
Jitter RMS(cg)	10.7 ps	10.27 ps	530 fs

1.25 Gbps Eye Pattern

over-etched differential pair



FR-4 PCB Limits - Summary

- Eye Diagram Response
  - Deterministic Jitter and Risetime Losses are well known and due to dielectric and conductor skin effect losses.
  - Eye diagram mask violations in amplitude or bit time jitter lead to unacceptable Bit Error Rates
- Fabrication Quality of PCB traces strongly affects eye response.
  - 100 Ω impedance line losses not strongly affected by line size.
- Semiconductor pulse fidelity and receiver determining factors
  - Receiver threshold region < (15 - 20%) of swing OK
  - Risetimes <(15 - 20)% of bit width reduces mask violations
- FR-4 max. line length depends on devices, bit rate, reflections and losses
  - As a practical matter, jitter more forcefully impacted by bandwidth limits due to losses
  - Connector reflections shorten maximum length.
- Maximum usable clock rate F_{clk} ~ (7 - 10) * f_e at reasonable PCB lengths of 0.5 meter to 1.25 meter.