IEEE 802.3
Higher Speed Study Group

Proposal for a 10 Gbps MII

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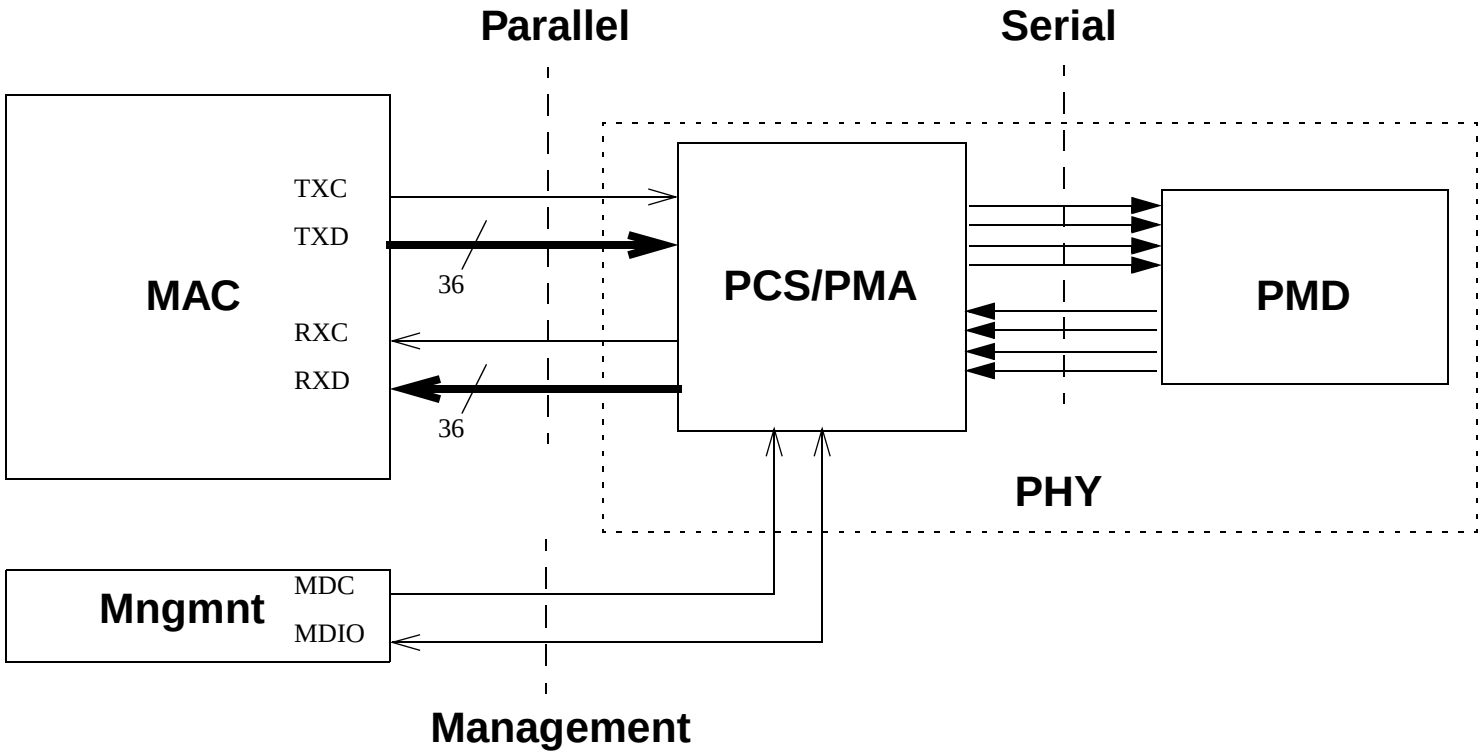
Outline

- Wish List
- Interface Locations
- Parallel Interface
- Serial Interface
- Management Interface
- Scaling
- Summary

Wish List

- Specify interfaces that allow for multiple PHY and PMD variations
- Provide a convenient partition for implementers
- Provide a standard *inter-layer* interface between MAC and PHY
- Provide a standard *intra-layer* interface between PHY and PMD
- Interfaces should be scalable in speed and width
  - Keep up with technology development
  - Allow implementation flexibility

Interface Locations



Parallel Interface

- 32 data bits, 4 control bits (one per byte), one clock, for transmit
- 32 data bits, 4 control bits (one per byte), one clock, for receive
- Dual Data Rate (DDR) signaling, with data and control driven and sampled on both rising edge and falling edge of clock
- Control bit per byte allows use of embedded delimiters, rather than discrete signals
- Control bit per byte allows interface to be scaled in speed and width

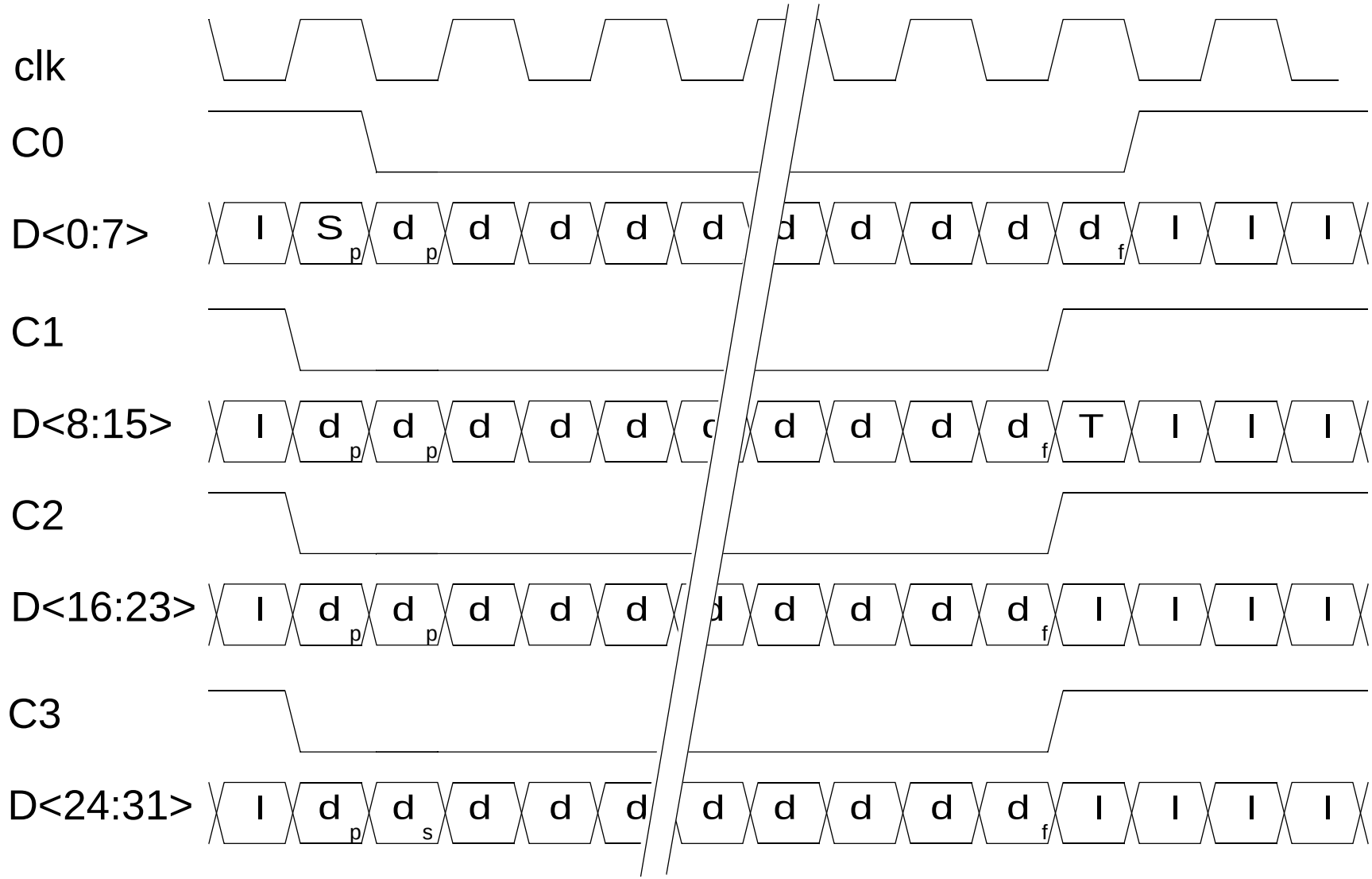
Parallel Interface (cont)

- Control bit (C) is “1” for delimiter and special characters
- Control bit (C) is “0” for normal data characters
- Delimiter and special character set includes:
  - IDLE
  - SOP
  - EOP
  - ERROR
- Delimiters and special characters are distinguished by the value of the 8 bit data bundle when the corresponding control bit is “1”

Parallel Interface (cont)

- IDLE (I) is signaled
  - during the inter-packet gap
  - when there is no data to send
- SOP (S) is signaled
  - for one byte duration
  - at the beginning of each packet
- EOP (T) is signaled
  - for one byte duration
  - at the end of each packet
- ERROR (E) is signaled
  - when an error is detected in the received signal
  - when an error needs to be forced into the transmit signal

Parallel Interface (Example)



Serial Interface

- 4 x 2.5 Gbps
- Transmit and Receive data signals
- Clock references?
- Data signals are:
  - Differential
  - PECL
- Control signals (RX_LOSS, TX_DISABLE) are single-ended

Management Interface

- Reuse management interface protocol from 802.3u clause 22
- Serial 2 wire (MDIO/MDC)
- 32 bit management frame, conveys 16 bits of data
- 16 registers defined by IEEE
- 16 registers available for vendor specific information
- Define new bits and registers as needed for 10 Gbps operation
  - Need to be careful about bit and register consumption
  - May need to use an “escape hatch”

Scaling

- The parallel interface can be scaled in speed and width
  - 32 data bits, 4 C bits
  - 16 data bits, 2 C bits
  - 8 data bits, 1 C bit
- The delimiter and special character definitions remain constant
- Since this is not an exposed interface,
  the speed and width choice is up to the implementer
- No need to “negotiate”, monitor, or control the speed and width

Summary

- The parallel interface supports different coding schemes
- The serial interface supports different signal parameters
- Together, these two interfaces provide lots of flexibility
- Both interfaces can be scaled in speed and width without changing the protocols
- The existing clause 22 management interface can be reused