Error Correction with Fibre Channel Transmission Code

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Purpose and Application

- Reduce rate of retransmission
  - Reduce interruptions for real time applications
  - Reduce processing burden in network nodes
- Link-component trade-off

Basic Principle

Rectangular arrangement of *horizontal* and *vertical parity*

Byte 1	**Horizontal Parity byte 1**
Byte 2	**Horizontal Parity byte 2**
. . .	**. . .**
Byte n–1	**Horizontal Parity byte n–1**
Byte n	**Horizontal Parity byte n**
Vertical Parity for segment (byte 1 to n)	**Horizontal Parity for Vertical Parity byte**

- A violation of a *horizontal parity locates* the error to a specific byte
- Violations in the *vertical parity* are used to *correct* the erroneous byte
- The horizontal parity may be explicit or an equivalent parameter may be built into a transmission code

Transmission Codes with Local Parity

- **16/20B Transmission Code** using only 20B vectors with 10 ones and 10 zeros
  - Complex Implementation compared to codes of smaller blocks
  - Large Error Spread (≤ 2 bytes)
  - Requires two bytes of vertical parity
- **Special 8B/10B Code** with local parity using only 10B vectors with 3, 5, or 7 ones
  - Efficient, overhead of *only one byte* of vertical parity/segment

For both codes, any odd number of errors in a byte generates an invalid character

Properties of special 8B/10B Code with Local Parity

- Maximum run length is 5, no contiguous runs of 5
- Minimum of 3 transitions per byte
- 8-bit Comma: ‘11011111’ or complement
- Running disparity at byte boundaries: ± 2
- DC-balanced, but stronger low frequency spectral components than FC code. Time constants for high pass filters must be increased by 80% compared with Fibre Channel Code
- The encoding and decoding process requires more gates than the FC code

Application of Codes with Local Parity

- Universal use of error correction on all links of an application
- Significantly reduced overhead if EC segments are short
- High error rates which require short segments

Locating Erroneous Byte with Fibre Channel Code

Fundamental Facts

- A frame with any odd number of erroneous bits is recognized as invalid by the FC code
- All coded bytes are either balanced (5 ones) or have a disparity of ± 2 (4 or 6 ones)
- For random data, a bit error generates an ***invalid character in 2 out of 3 cases.***
- The remaining errors generate a disparity error at the *next disparity dependent* code block.
- For random data, ***only 2 out of*** 10^9 ***errors remain undetected after the next 15 bytes of random data.***

Requirements and Assumptions for Success of Error Correction

- There is *only one* erroneous byte in the segment covered by the error correction scheme
- There are no EC segment or byte *alignment* errors
- Any detected error is assumed to have occurred within the 16 byte field ending with the first code violation.

Error Locating Based on Disparity Violations

- Each byte and each quartet of bytes is assigned a *Balance Bit B and Q*, respectively, with a value of 1 for balanced blocks. The B and Q bits are *not transmitted*.
- A *parity bit BPAR0* is derived from all the B-bits assigned to byte 0 of each quartet in the entire EC segment. BPAR1, 2, and 3 is each derived in the same way from byte 1, 2, and 3 of each quartet, respectively.
- The *parity bits QPAR0*, 1, 2, and 3 are derived in an analogous way from the balance bits Q0, Q1, Q2, and Q3 assigned to consecutive quartets, modulo 4.
- The eight PAR bits are encoded and *transmitted* after the end of the EC segment.
- An *error* in transmission will cause a *change in the balance bits B and Q* of the erroneous byte and quartet which in turns causes a parity violation in the respective BPAR and QPAR bits, which point to the exact quartet and byte, assuming that the error is in the byte with the 8B/10B disparity violation or in one of the preceding 15 bytes.

Structure of Error Correction Segment

Raw Data ABCDE FGH K	Coded Bytes DF abcdei fghj DB	Balance Bits B	 Q	Byte #
00111 101 1	– 001111 1010 +	0		0 0000
10101 101 0	+ 101010 1010 +	1		0 0001
11101 100 0	+ 000101 1001 –	0		0 0010
00101 010 0	– 001011 0101 –	1	1	0 0011
01100 101 0	– 011001 1010 –	1		0 0100
10010 100 1	– 100101 1001 –	1		0 0101
10011 101 0	– 100110 1010 –	1		0 0110
01001 011 0	– 010011 0110 –	1	1	0 0111
10110 110 0	– 101100 1100 –	1		0 1000
11010 011 0	– 110100 0110 –	1		0 1001
10010 000 0	– 100101 1011 +	0		0 1010
10101 000 0	+ 101010 0100 –	0	1	0 1011
01110 101 0	– 011100 1010 –	1		0 1100
01110 101 0	– 011100 1010 –	1		0 1101
01110 101 0	– 011100 1010 –	1		0 1110
10010 000 0	– 100101 1011 +	0	0	0 1111
00110 110 0 **Vertical Parity**		0 1 1 1 BPAR	0 0 0 1 QPAR	1 0000

Application Option No. 1

Error Checking Segments and Packet Frames are congruent

- Reliable demarcation of *segment boundaries* in the presence of errors can be difficult, depending on the frame and Idle structures
- Too much *overhead* for short frames if there are no mandatory Idles between frames
- EC segment formatting and error correction could be done in the same layer where the CRC checks are performed, using the existing buffers. Not an option for Ethernet.
- The EC operations can be done in the physical layer which requires dedicated buffers and adds in practice *latency* equivalent to the packet length.
- Requires an architecture which has room for the parity bits.

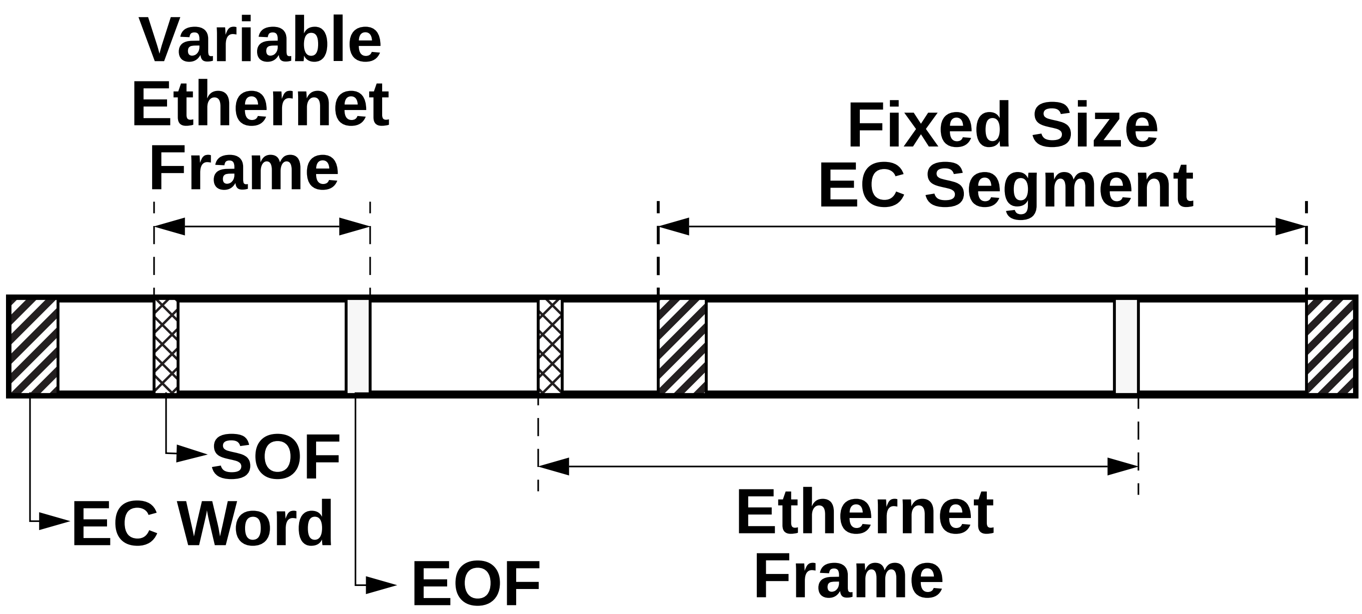
Application Option No. 2

Error Checking Segments and Packet Frames are totally independent

In the physical layer, an **EC parity** is inserted into the bit stream at fixed intervals:

- For example, a 4-byte EC-word starting with a **comma-character** every 768 bytes
  - The EC-word provides byte and word synchronization independent of the pay-load structure. This feature is very useful for striped parallel links.
  - Any comma-characters in the payload must be aligned with the same boundaries.
  - Create the necessary bandwidth for the EC-word by deleting and restoring pre-amble bytes. Equalize rate with the help of a small buffer.
  - For very long frames, an appropriate Inter Frame Gap can be specified.

Option No. 2, continued



- Entry and removal of the EC word at the physical layer is *transparent* to the upper levels of the protocol, if part of the preamble can be made available for this purpose.

Summary

- Fibre Channel 8B/10B Code can support single error correction with a minimum of 17 bits per EC segment of extra overhead.
- Practical implementations use a *4-byte word* to also provide *word synchronization* which is desirable for high speed applications. The Ethernet framing and Idles are then relieved of this task.
- Simple circuits translate between standard Ethernet frames and frames suitable for transmission over a single or multiple parallel links.
- The translation process also sets free enough bandwidth for the requirements of error correction.
- References:

1. IBM Research Report RC 19106, Error Correction Based on Transmission Code Violations and Parity *
2. IBM Research Report RC 18855, The ANSI Fibre Channel Transmission Code *

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