# Feasibility of 3.125 Gb/s in CMOS

Mike Jenkins LSI Logic Corporation

### Feasibility of 3.125 Gb/s in CMOS

#### ----- Transmitter ------Tek $\leftrightarrow$ Cursors Window FFTmaa Def Tra 500mV 100m ∕div ኡ Inot! trig'd **∕** ⊺ -500mV-24.04ns 50ps/div 24.54ns 10mV Mean 24.43ns $\mu \pm 1\sigma$ 69.034% Main Size gol RMS∆ 11.76ps µ±2σ 96.548% 50ps∕div Btm -10mV 24.25ns PkPk 68ps u±3σ 100% Main Pos 1014 Wfms 195 24.55ns Hits 24.035ns Mask Color Grad Standard Remo∨e⁄Clr Persist∕ Histograms Testing Scale Trace 1 Masks Color GradCount Off FC1063E M7-M8 Stopped 1062.5Mb Main

#### ----- Receiver ------

LSI GBG11RD.mdb - GigaBlaze G11 Evaluation System	
<u>F</u> ile <u>E</u> dit ⊻iew <u>S</u> cripts	<u>H</u> elp
🖻 🗿 የ 📢	
E- Core1	Register Addr (Hex) Data (Hex)
	ERRCNT 2000 00000
COREOUT	CYCCNT 2001 46F40
FOI CPZB	CYCCNT 2002 109EE
CYCCNT	CYCCNT 2003 00000
EDDCNT	CR 2004 784
	CPZn 2005 0070C
ERRUR_BUFFER	TGWR 2007 5557C
	TGWR 2008 95A56
E LEXAR	TGMR 2009 FFFFF
E LTXAR	TGMR 200A FFFFF
STATEBITS	TGAR 2008 00000
	LTXAR 200C 00071
	LEXAR 200D 00065
	STATE 200E 00044
	COREO 200F 000C8

LSI LOGIC

#### Zero errors in more than 2<sup>36</sup> cyc x 20 bits/cyc < 10<sup>-12</sup> BER

### Feasibility Of 3.125Gb/s in CMOS: through **20**" of PCB vs. **Emphasis**







## **Technical Details**



- Hardware used for this demo is nominal G11 GigaBlaze evaluation parts. G11 GigaBlaze is not fully characterized nor planned to be offered at this speed.
- Transmitter waveform is after 20" of board trace plus 1meter of cable (100 ohm differential impedance). Differential PCB traces are microstrip (15 mils wide, 35 mil space & 8 mil dielectric). Transmitter emphasis is used. Transmitted pattern is CRPAT.
- Receiver data looped back from transmitter through ~6 inches of board trace plus 1 meter cable plus ~6 inches of board trace. (There wasn't an error after 10<sup>12</sup> bits. I just got tired of waiting.)
- Power dissipation (TX plus RX, nominal) = 404 mW.

![](_page_4_Figure_0.jpeg)

- Hardware that produced these results is compatible with word striping proposal. It is not compatible with byte striping proposal, which requires higher clock rates, more complex logic plus training sequences.
- Both proposals transfer data organized as shown above. Both do add/delete in 4-byte increments.

### Summary

![](_page_5_Picture_1.jpeg)

- Feasibility of 3.125 Gb/s in LSI Logic's CMOS technology has been demonstrated.
- For low-risk implementations, the word striping approach on the PCS/PMA-to-PMD interface is strongly recommended.