Word Striping on Multiple Serial Lanes

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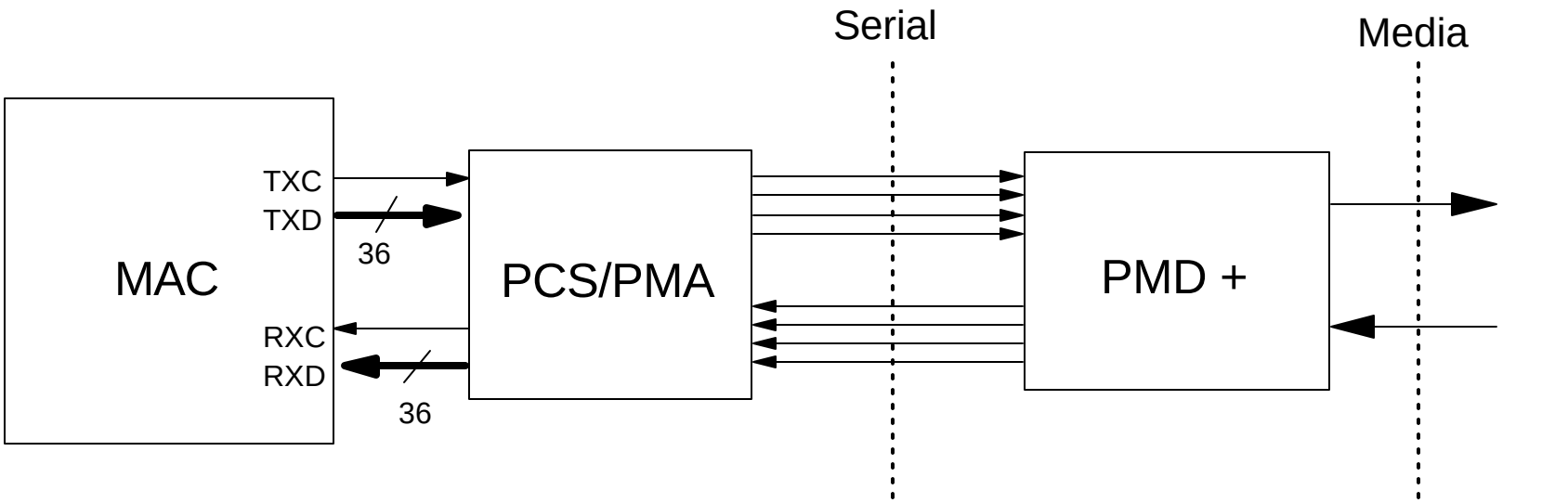
Interfaces Which Benefit from Word Striping



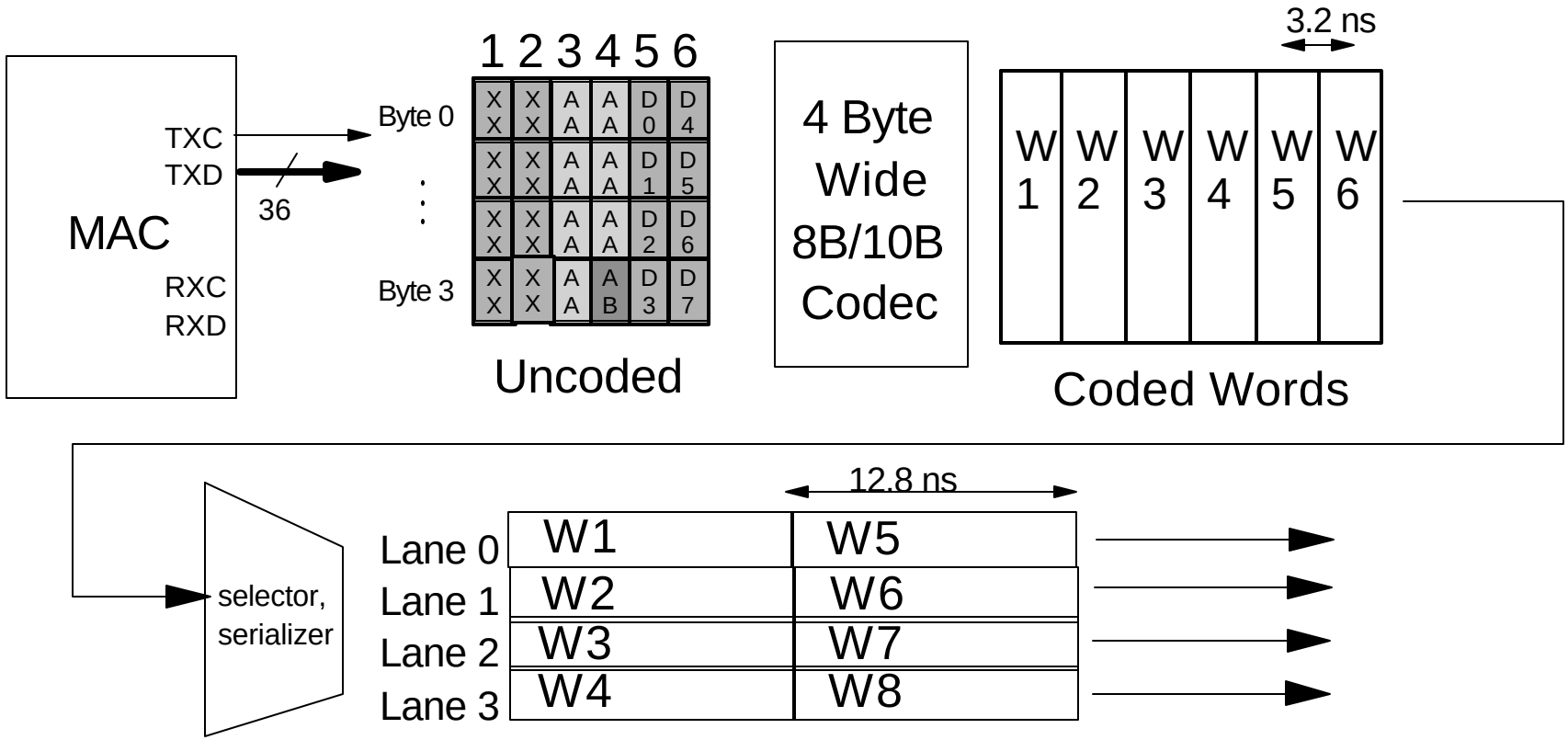
- Word striping simplifies:
  - Deskewing on Serial and Media Interfaces
    - No training sequences needed to deskew
    - Simple circuits, easy implementation
  - Translation from "serial" electrical to Media coding

Requirements and Assumptions

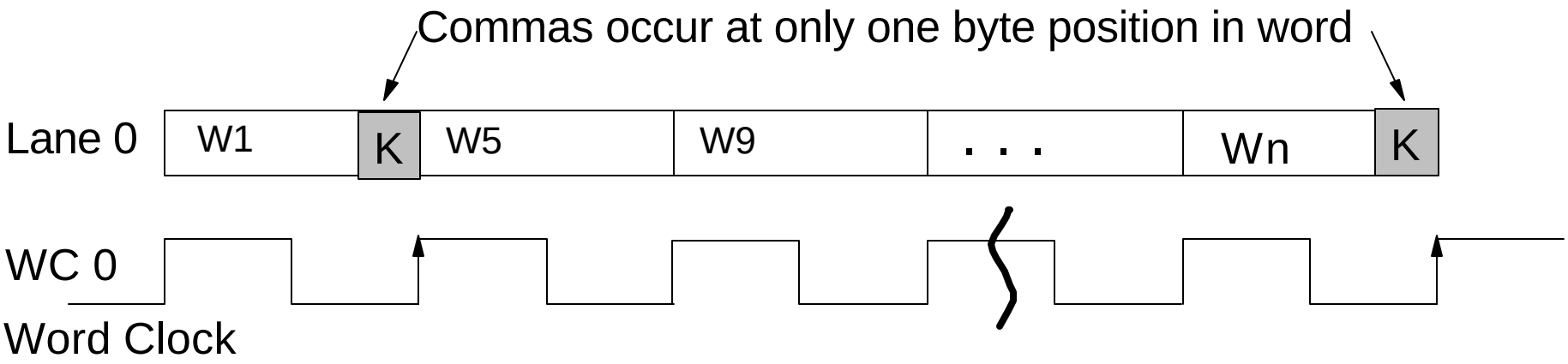
- Skew Tolerance Requirements:
  - 6 ns peak to peak skew
  - simple circuits operating from data derived clocks
  - no special training sequences or protocol needed to deskew
- Multi-Clock Domain Synchronization:
  - Insert / Delete granularity of 1 Word (regardless of number of lanes)
  - Accommodate any number of lanes without change
- Versatility:
  - Accommodate single (12.5 Gbaud) and a variety of multiple lanes with no change in transmission format or insert/delete granularity
  - Should serve both 10 Gb/s Ethernet and Fibre Channel with simple adaptations
  - Accommodate transmission codes other than 8B/10B
  - Provide easy in-band signalling for maintenance, diagnostic, and control functions

What is Word Striping?

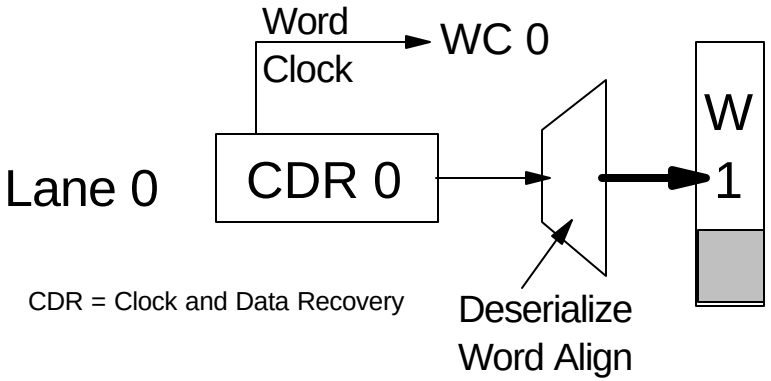
- EXAMPLE: Look at 4 x 3.125 Gbaud "Serial" interface:
  - Uncoded data is presented 4 bytes wide at Parallel interface
  - Data is coded by 4 byte parallel 8B/10B codec
  - Word = 40 bit or 4 byte encoded entity
  - Word is serialized and transmitted on a lane
  - Successive words sent to successive lanes wrapping back to the first
  - Modest added serialization delay; great payback in deskewing and clocking !



Word Synchronization on a Lane



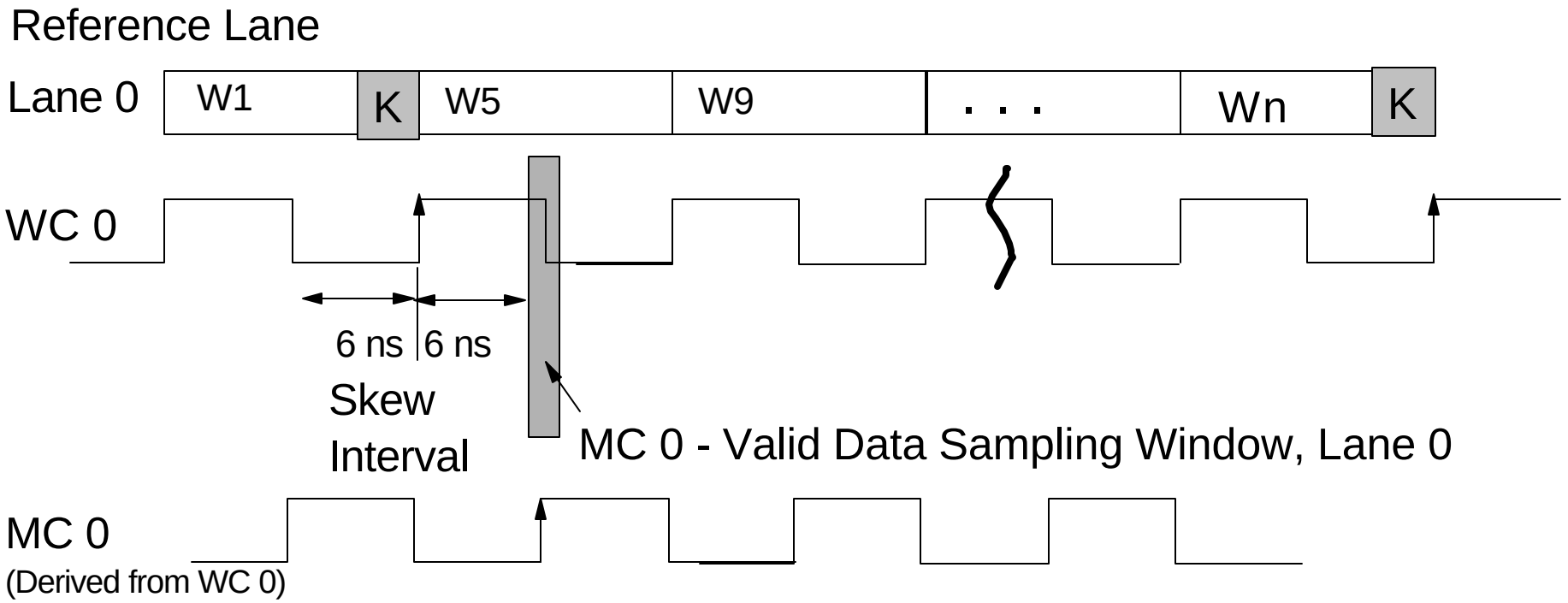
- Commas must appear in designated byte position of word
- Commas then maintain phase alignment with word clock
- At least one comma must be received per lane at link bringup before payload traffic



Then:

- Each lane has a local word clock (e.g. WC 0)
- Data is automatically byte and word aligned

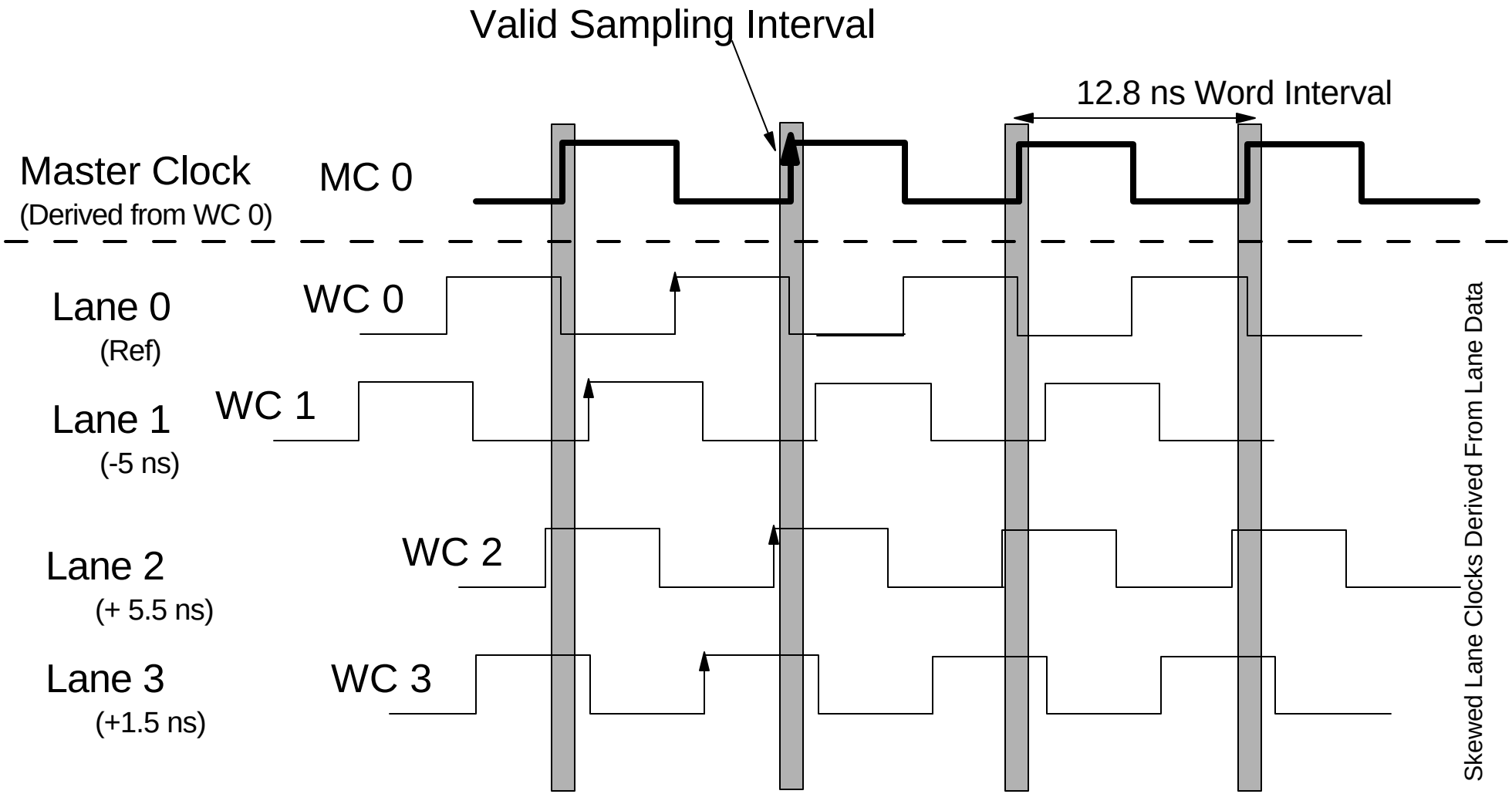
Deskew Using Master Received Reference Clock



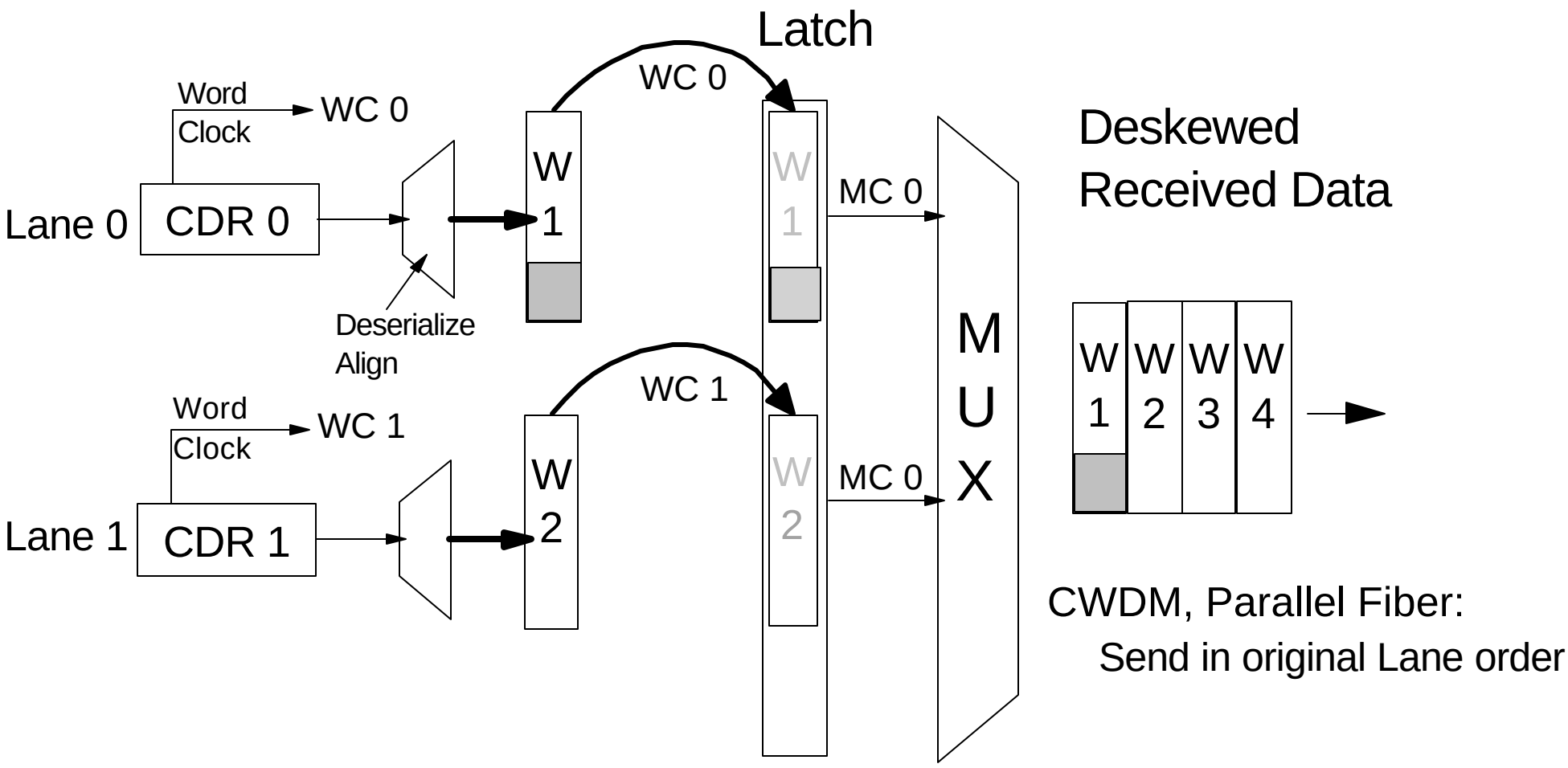
- IF Skew among lanes is 6 ns = (12.8ns - latch setup - margins)/2, THEN
  - Can choose any lane as the reference lane
  - Do not need to know relative delay from Reference Lane to other lanes
  - A set of hardwired clocks can be used to eliminate skew
    - NO ADJUSTMENT OF PHASE, NO STATE MACHINE
    - NO SKEW MONITOR CIRCUITS
    - NO TRAINING SEQUENCES
- For greater skews (to 12 ns), some decisions must be made BUT NO TRAINING SEQUENCES, NO STATE MACHINES

Master Reference Clock Valid for All Lanes

- IF each lane within +/- 6 ns skew of Lane 0, MC 0 is Data Valid Clock for all lanes
- Can choose any lane clock as reference clock (no need to specify)

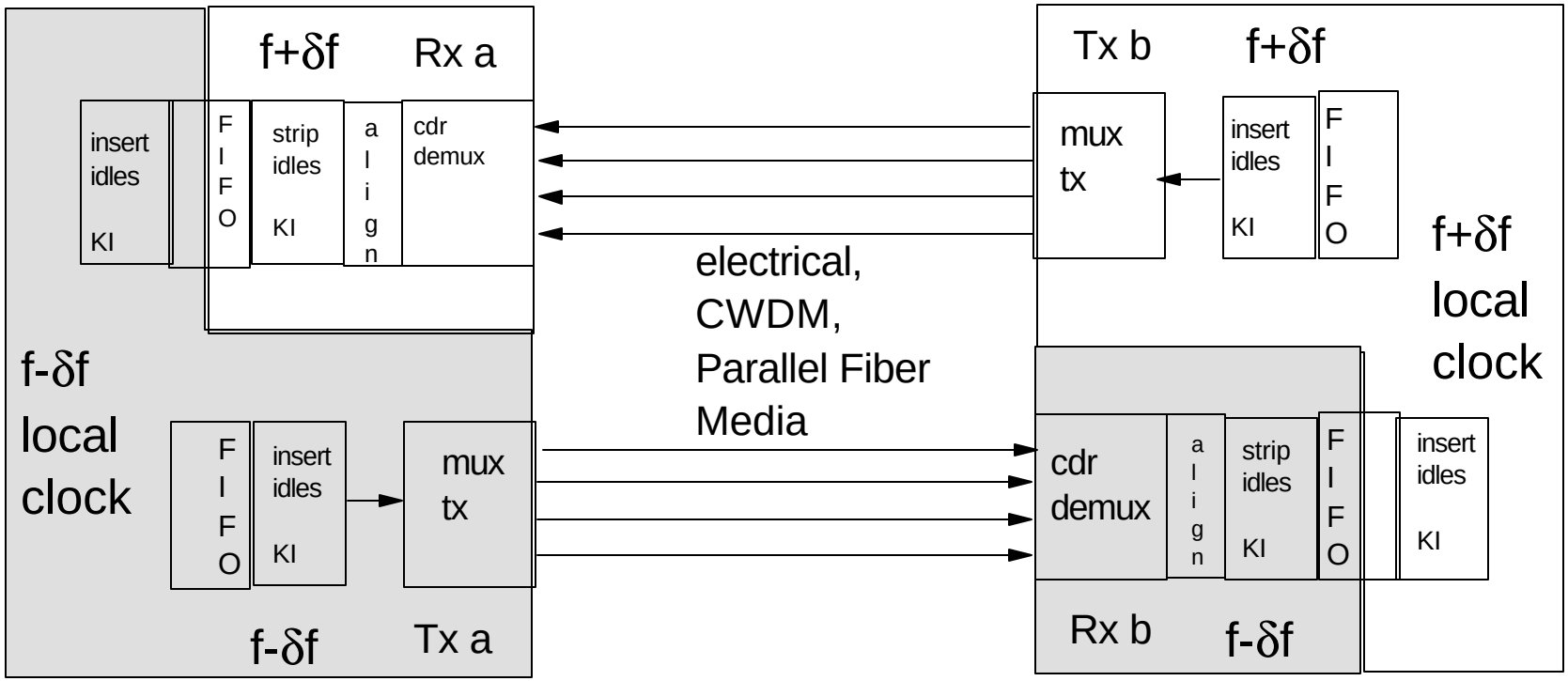


Lane to Lane Skew Elimination



- Recover clock and lane word clock (occasional commas)
- Deserialize and align to word boundaries
- Write into latch with local lane word clock, WC x
- Read from latch with proper phase of master reference lane clock MC x
- Read sequentially, lane 0, 1, 2, 3, 0, 1, 2, 3, 0 ....
- Data is DESKEWED and IN ORIGINAL BYTE ORDER

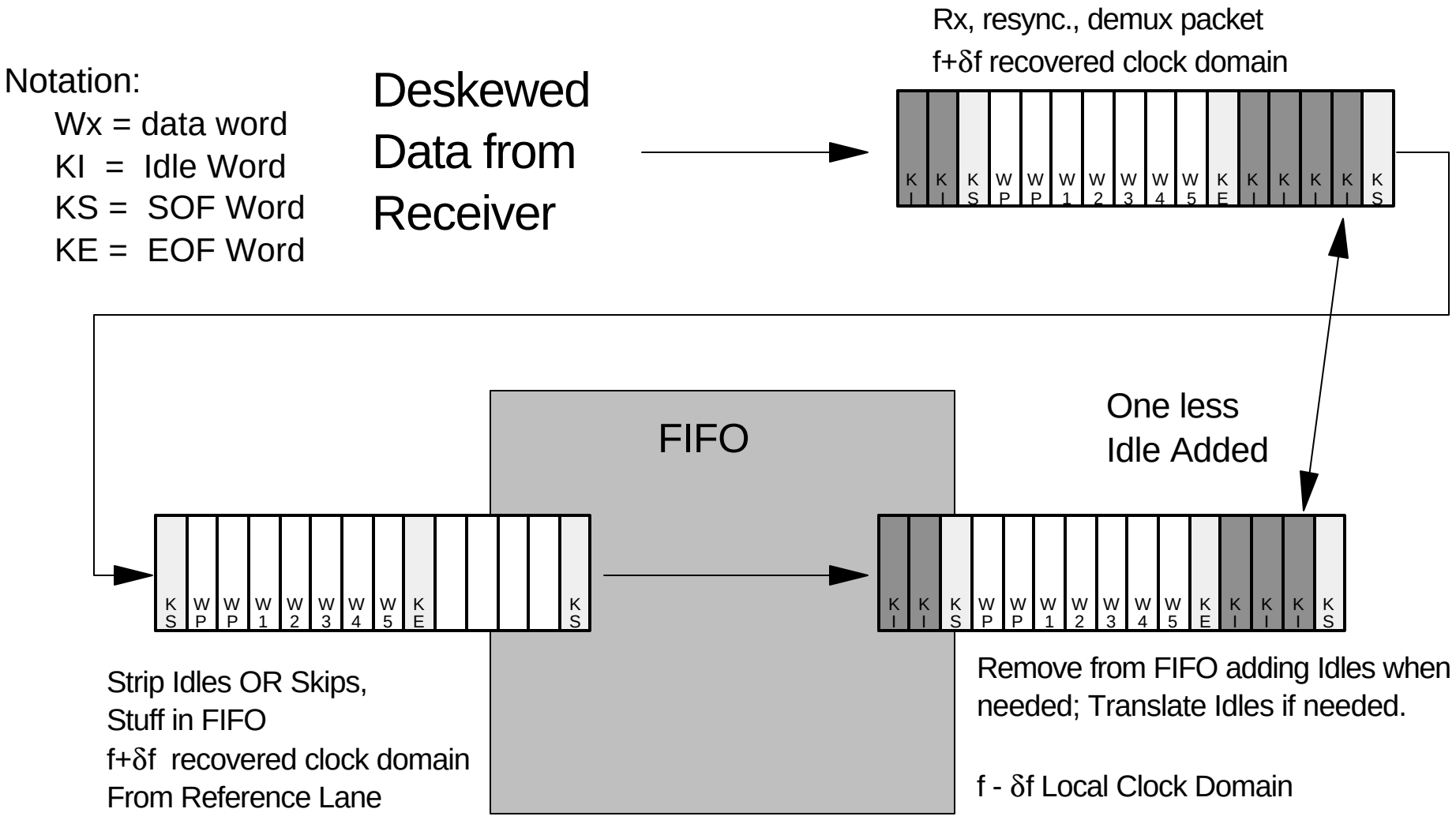
Multiple Clock Domain Issue



Transceiver A,
Local Clock f-δf

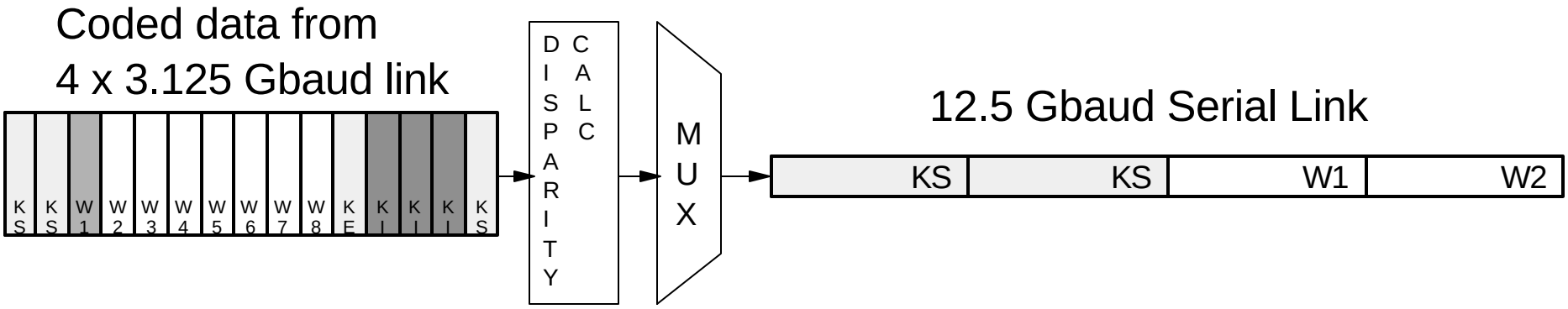
Transceiver B,
Local Clock f+δf

Multiple Clock Domain Insert / Delete



- Required insertions / deletions done at FIFO output with 1 Word Granularity (4B)
- Insert / Delete rules (min IPG) can be programmed via MDIO/MDC interface
- NO DEPENDENCY ON NUMBER OF LANES (1, 4, etc.)

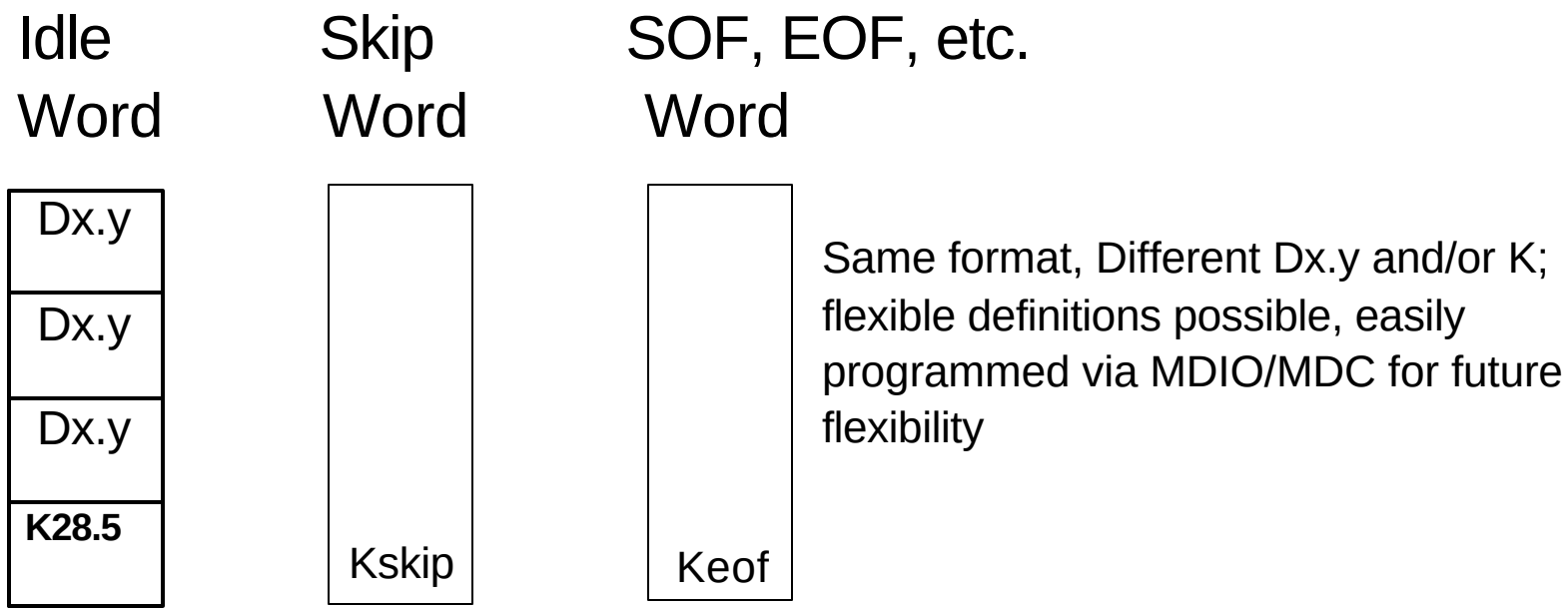
Translation from Parallel Lanes to a Single 12.5 Gbaud Lane



- Can reserialize words with minimal complexity
  - Monitor word to word disparity
  - Complement disparity dependent 6B and 4B vectors when necessary
  - The complexity of disparity recalculation at word rate is much less than an 8B/10B encoder
  - The data from 4 x 3.125 Gbaud link never needs to be decoded
  - Format is compatible with word-rate framing circuits in receiver

Control Codes or Ordered Sets

- Because Control Codes are based on entire WORDS
  - More flexibility to define control codes with error protection
  - Spectral shaping to minimize EM Emissions is easier
  - Huffman distance greater from data or other ordered sets (4Bytes vs. 1 or 2Bytes)
- New Sets for in-band signalling can be defined without resorting to a large number of control characters
  - Better able to accommodate different PMD options
  - In-band signalling aligned with data across interface



CONCLUSIONS:

- ATTRACTIVE ATTRIBUTES OF WORD STRIPING
  - Fixed (Hard Wired) Clocks Eliminate Skew (up to 6 ns) - Easiest Deskew Imaginable; NO TRAINING, NO STATE MACHINE !
    - Word-aligned Commas
    - Synchronization independent of number of lanes
    - Can extend to 12 ns skew tolerance with modest added logic
  - Frame Format and Coding Independent of Number of Lanes
  - Compatible with variety of Traffic (EN or FC)
  - Good match with 12.5 Gbaud serial and accommodates other serial codes
  - No Lane Identification Required
  - Greatest flexibility in control characters for future PMD needs

Backup Foils

10 GMII Data Encapsulation

10 GMII Format

Byte 0	I	I	S	dp	d	d	...	d	d	df	I	I	I	S	dp
Byte 1	I	I	dp	dp	d	d	...	d	df	T	I	I	I	dp	dp
Byte 2	I	I	dp	dp	d	d	...	d	df	I	I	I	I	dp	dp
Byte 3	I	I	dp	S	d	d	...	d	df	I	I	I	I	dp	S

Key: d = data character
S,K = non-comma control
C = comma character

Word Striped Format

Byte 0	di	di	S	dp	d	d	...	d	d	df	di	di	di	S	dp
Byte 1	di	di	dp	dp	d	d	...	d	df	T	di	di	di	dp	dp
Byte 2	di	di	dp	dp	d	d	...	d	df	K	di	di	di	dp	dp
Byte 3	C	C	C	C	d	d	...	d	df	C	C	C	C	C	C

- ALWAYS HAVE ENOUGH COMMAS FOR EACH LANE PER IPG
  - This example: 6 comma words per EN Frame
  - Will always have 5 commas, even for 12 byte minimum IPG
- Byte position of comma C is TBD- flexible. Prefer last byte.
- Exact Idle word TBD, could include C and K
- C could be just K28.5, or could be flexible mix of K28.1, K28.5, K28.7 for marking Skip words

Example of Word Striping and Comma Density

Word striping on lanes

Lane 0	KI	W2	W6	KI	W1	W5	KI	WP	W3
Lane 1	KS	W3	W7	KI	W2	W6	KI	WP	W4
Lane 2	KS	W4	W8	KS	W3	KE	KI	W1	W5
Lane 3	W1	W5	KE	KS	W4	KI	KS	W2	KE

Key:

KI = Idle word

KS = SOF Word

KE = EOF Word

- Packet need not start in lane 0
- Rotation direction should be defined (0,1,2,3,0,1,2,3...)
- Minimum 5 comma words per packet (SOP- KS, EOP-KE commas count!)
- Can add Idles one word at a time
- Idles / Skips inserted / deleted when removing data from FIFO
  - Can program exact algorithm over MDIO/MDC interface