Hari Coding Objectives

- Protocol Independence - 10 GbE, FC, InfiniBand
  - Alignment independence (e.g. word, even/odd, etc.)
- Application Independence
  - Chip-to-PMD, Chip-to-Chip (backplane), Very Short-Haul link, Scalable # Lanes
- PMD Signaling Independent
  - Single-Channel: Serial, Multilevel
  - Multi-Channel: WWDM, Parallel
- KISS for 10 GbE - Simplest Hari Coding
  - Mimic 1000BASE-X PCS Look and Feel
  - No Train-Up, Low Clock Rates, Implementation Flexibility

Hari Coding Functions & Features

- Link Synchronization - Comma - **/K28.5/**
  - Issued at a protocol dependent rate (e.g. IPG)
- Clock Tolerance Compensation - Insert/Remove
  - Applications: PHY-to-PMD, Rx-to-Tx, Tx-to-Tx
  - Multiple Clock Domains are optional
- Lane Deskew - Alignment of Received Columns
  - Required for Insert/Remove Column processing
  - All Hari information can be column aligned allowing the simplest and most flexible processing

Hari Coding Functions & Features 2

- Lane Ordering - Lane ID - **/K27.7/**
  - Identifies Lane 0 in a protocol independent manner
  - Doubles as Start-of-Packet for 10 GbE **/S/**, InfiniBand
- Error Code - **/K30.7/**
  - Signaled when an error is: detected in the received signal or needs to be forced into the transmitted signal

Clock Tolerance Compensation

- Define Insert/Remove code as **/K28.0/** (**/R/**)
- Simultaneously transmitted across all Lanes
  - Incomplete Columns of Insert/Remove codes are allowed
    - Not recognized as Insert/Remove function
- Clock Tolerance Compensation
  - Insert **/R/** column immediately after **/K/** or **/R/** column
  - Remove **/R/** column immediately after **/K/** or **/R/** column
    - I.e. Can't remove single **/R/** column not preceded by **/K/**
  - Lowest granularity, 1 code-group per lane, scaleable
- Proper Disparity code required in each Lane

Lane-to-Lane Skew Budget

- PCB lane-to-lane skew: < 1 UI
- SerDes lane-to-lane skew: < 1 UI
  - E.g. 320 ps at 3.125 GBaud
- Medium lane-to-lane skew: < 16 UI
  - Sufficient for 40 km WWDM links @1300 nm (14.4 UI)
- Total maximum lane-to-lane skew: < 20 UI
  - E.g. 6.4 ns at 3.125 GBaud
  - Total = 2 x PCB + 2 x SerDes + Medium skew

.: 20 UI deskew pattern needs to be 40-bits

Deskew Protocol

- Deskew by lining up commas with the same running disparity in all Hari lanes (i.e. column)
  - Deskew necessary during initialization only
  - Disparity aligned 40-bit Link Sync pattern defined as:

    /+ or - comma/¬comma/any/¬comma/
  - All comma must be of the same running disparity
  - Specified pattern transmitted in all Hari lanes
  - Protocol dependent pattern frequency
- 10 GbE Idle pattern, **/K/R/K/R/**
  - **/-K/+R/+K/-R/** ending RD is - .: the pattern repeats
  - Deskew by aligning + or - commas
  - Simplest deskew, No Training sequence/protocol req'd

Hari Coding Summary

- Simple rules, Protocol/Application independence
  - Common coding rules for 10 GbE, IB, FC
- Cost-effective “system interface” for Serial PMDs
- Leverages high-reliability, ubiquitous 8B/10B code
  - Low gate-count/complexity Encode/Decode, well known
- Virtually identical to 1000BASE-X PCS
- Column aligned data enables simplest Rx process
  - No serialization delays, low speed clocking
  - Implementation flexibility (e.g. 4/8/16 octets/cycle)
- Overall best match for simple 10G System Interface

Example Slides

10 GbE Hari Encoding

Lane 0	K	R	S	d_p	d	d	---	d	d	d	d_f	K	R	K	R
Lane 1	K	R	d_p	d_p	d	d	---	d	d	d_f	T	K	R	K	R
Lane 2	K	R	d_p	d_p	d	d	---	d	d	d_f	R	K	R	K	R
Lane 3	K	R	d_p	d_s	d	d	---	d	d	d_f	R	K	R	K	R

- Same basic code-groups as 1000BASE-X

10 GbE Hari Encoding

Lane 0	K	R	S	d_p	d	d	---	d	d	d	d_f	K	R	K	R
Lane 1	K	R	d_p	d_p	d	d	---	d	d	d_f	T	K	R	K	R
Lane 2	K	R	d_p	d_p	d	d	---	d	d	d_f	R	K	R	K	R
Lane 3	K	R	d_p	d_s	d	d	---	d	d	d_f	R	K	R	K	R

- **/K/R/** repeating Idle pattern

10 GbE Hari Encoding

Lane 0	K	R	S	d_p	d	d	---	d	d	d	d_f	K	R	K	R
Lane 1	K	R	d_p	d_p	d	d	---	d	d	d_f	T	K	R	K	R
Lane 2	K	R	d_p	d_p	d	d	---	d	d	d_f	R	K	R	K	R
Lane 3	K	R	d_p	d_s	d	d	---	d	d	d_f	R	K	R	K	R

- **/S/** Start of Packet Delimiter
  - Also serves as Lane 0 ID

10 GbE Hari Encoding

Lane 0	K	R	S	d_p	d	d	---	d	d	d	d_f	K	R	K	R
Lane 1	K	R	d_p	d_p	d	d	---	d	d	d_f	T	K	R	K	R
Lane 2	K	R	d_p	d_p	d	d	---	d	d	d_f	R	K	R	K	R
Lane 3	K	R	d_p	d_s	d	d	---	d	d	d_f	R	K	R	K	R

- **/d/** Packet Data
  - **/d_p/** Preamble
  - **/d_s/** Preamble SFD
  - **/d_f/** Frame Check Sequence

10 GbE Hari Encoding

Lane 0	K	R	S	d_p	d	d	---	d	d	d	d_f	K	R	K	R
Lane 1	K	R	d_p	d_p	d	d	---	d	d	d_f	T	K	R	K	R
Lane 2	K	R	d_p	d_p	d	d	---	d	d	d_f	R	K	R	K	R
Lane 3	K	R	d_p	d_s	d	d	---	d	d	d_f	R	K	R	K	R

- **/T/** End of Packet Delimiter

10 GbE Hari Encoding

Lane 0	K	R	S	d_p	d	d	---	d	d	d	d_f	K	R	K	R
Lane 1	K	R	d_p	d_p	d	d	---	d	d	d_f	T	K	R	K	R
Lane 2	K	R	d_p	d_p	d	d	---	d	E	d_f	R	K	R	K	R
Lane 3	K	R	d_p	d_s	d	d	---	d	d	d_f	R	K	R	K	R

- **/E/** The “dreaded” Error code-group
  - Same as GbE **/V/** Void code-group

10 GbE - PMD Inserts /R/ column

Lane 0	K	R	S	d_p	d	d	---	d	d	d	d_f	K	R	K	R
Lane 1	K	R	d_p	d_p	d	d	---	d	d	d_f	T	K	R	K	R
Lane 2	K	R	d_p	d_p	d	d	---	d	d	d_f	R	K	R	K	R
Lane 3	K	R	d_p	d_s	d	d	---	d	d	d_f	R	K	R	K	R

PMD Inserts /R/ column here

Lane 0	K	R	S	d_p	d	d	---	d	d	d	d_f	K	R	R	K	R
Lane 1	K	R	d_p	d_p	d	d	---	d	d	d_f	T	K	R	R	K	R
Lane 2	K	R	d_p	d_p	d	d	---	d	d	d_f	R	K	R	R	K	R
Lane 3	K	R	d_p	d_s	d	d	---	d	d	d_f	R	K	R	R	K	R

PMD to 10 GMII Conversion

Lane 0	K	R	S	d_p	d	d	---	d	d	d	d_f	K	R	R	K	R
Lane 1	K	R	d_p	d_p	d	d	---	d	d	d_f	T	K	R	R	K	R
Lane 2	K	R	d_p	d_p	d	d	---	d	d	d_f	R	K	R	R	K	R
Lane 3	K	R	d_p	d_s	d	d	---	d	d	d_f	R	K	R	R	K	R

Hari

10 GMII

D<0:7>	I	I	S	d_p	d	d	---	d	d	d	d_f	I	I	I	I	I
D<8:15>	I	I	d_p	d_p	d	d	---	d	d	d_f	T	I	I	I	I	I
D<16:23>	I	I	d_p	d_p	d	d	---	d	d	d_f	I	I	I	I	I	I
D<24:31>	I	I	d_p	d_s	d	d	---	d	d	d_f	I	I	I	I	I	I

10 GbE Receiver Deskew

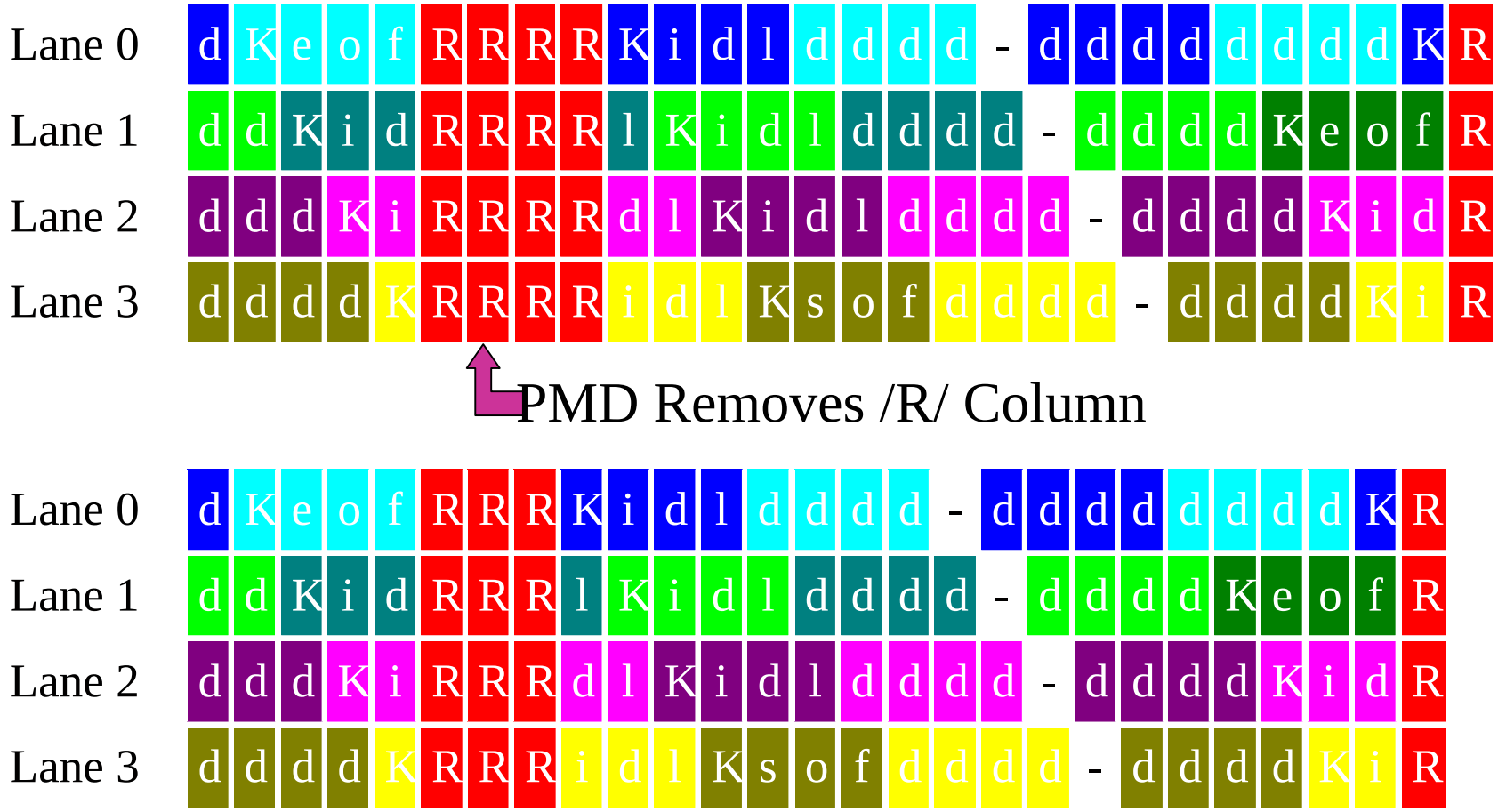
Skewed data at receiver input. Skew ~18 bits

Lane 0	-K	+R	+K	-R	-K	+R	+K	-R	-K	+R	+K	-R
Lane 1	-K	+R	+K	-R	-K	+R	+K	-R	-K	+R	+K	-R
Lane 3	-K	+R	+K	-R	-K	+R	+K	-R	-K	+R	+K	-R
Lane 3	-K	+R	+K	-R	-K	+R	+K	-R	-K	+R	+K	-R

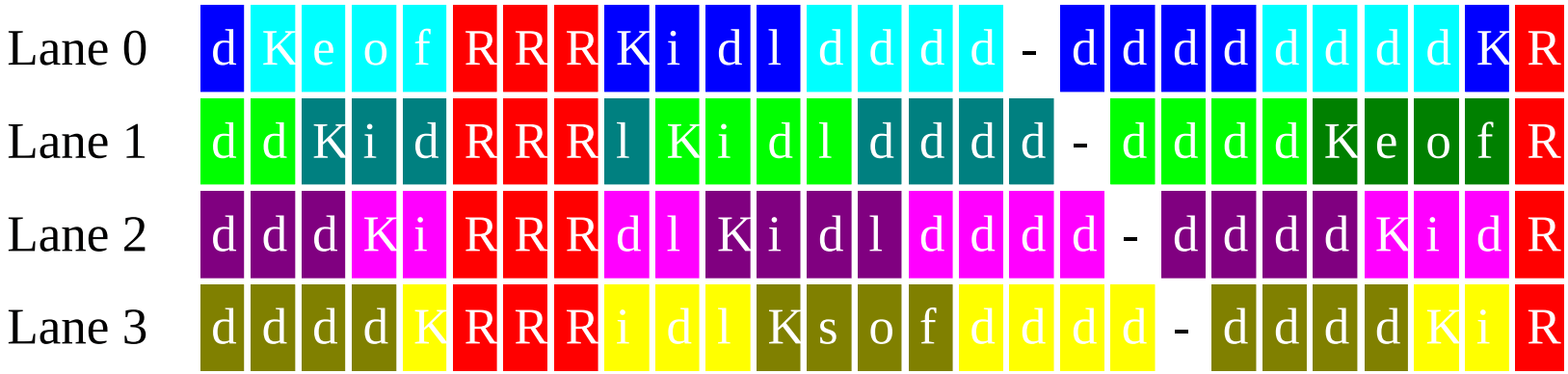
Simply line up like RD commas to deskew. Use Serial Shift Reg, etc.

Lane 0	-K	+R	+K	-R	-K	+R	+K	-R	-K	+R	+K	-R
Lane 1	-K	+R	+K	-R	-K	+R	+K	-R	-K	+R	+K	-R
Lane 3	-K	+R	+K	-R	-K	+R	+K	-R	-K	+R	+K	-R
Lane 3	-K	+R	+K	-R	-K	+R	+K	-R	-K	+R	+K	-R

10 FC - PMD Removes /R/ Column



10 FC - PMD to FC Final Receiver



Hari

FC Final Receiver