

10GE SerDes with GE Topology

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Gigabit Ethernet

- 10 bit parallel interface
- 12.5 Gb/s line rate
- Comma detect and align
- Additional PLL for phase alignment at 10 bit input (MUX)
- CML I/O for interfacing to Bipolar gate-arrays
- SiGe process
- Single supply (-5.0V)
- Available Q2/00 (partners)
Q4/00 (general market)

Critical Issues

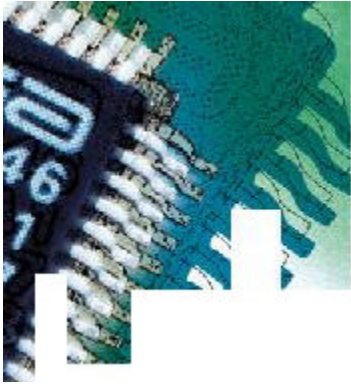
Technology Base

SDH/SONET

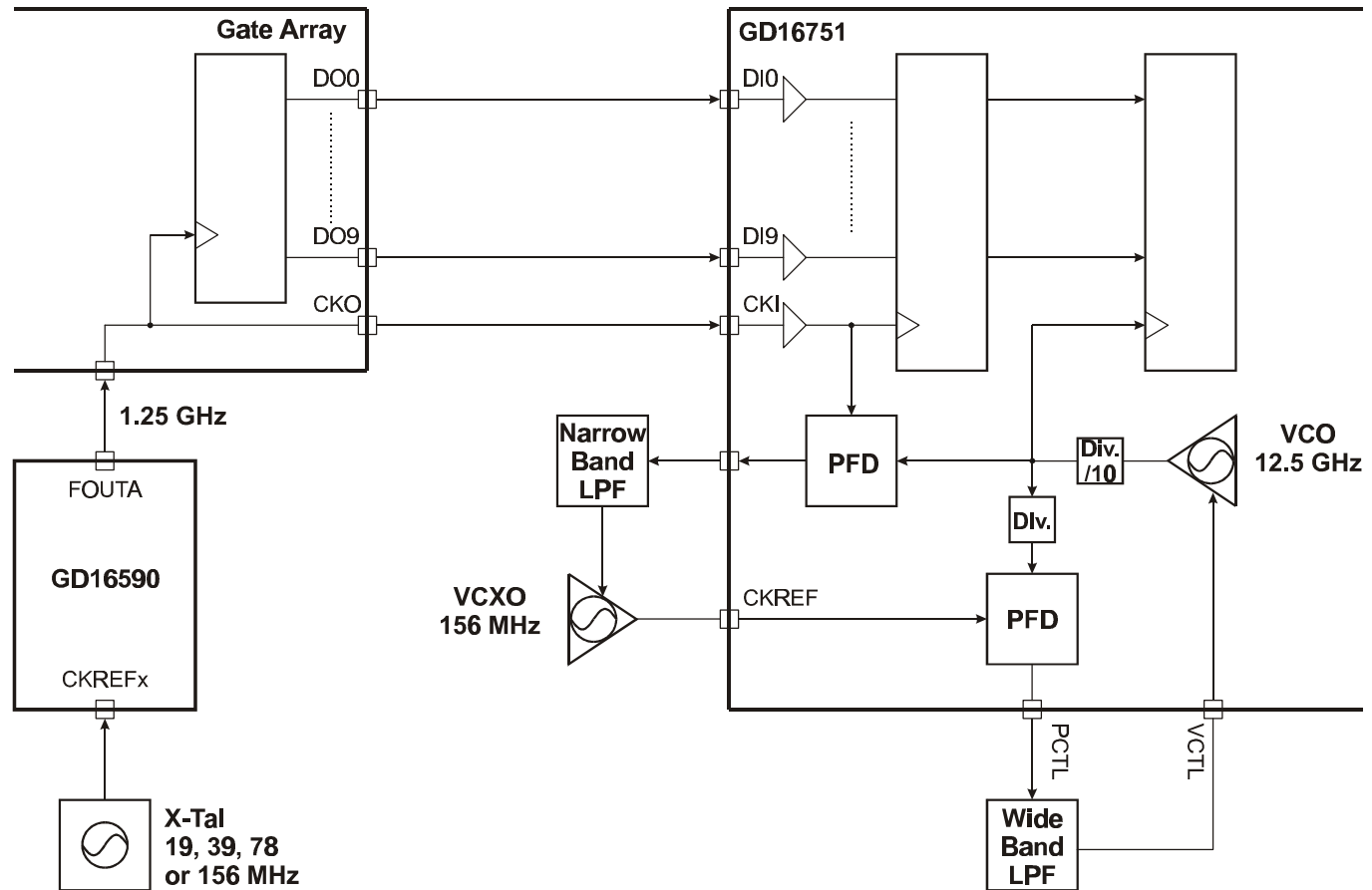
- 16 bit parallel interface
- OC-192/STM-64 line rate
- Mature (reliable) Silicon process
- Single supply (-5.2V)
- Available NOW !

GIGA

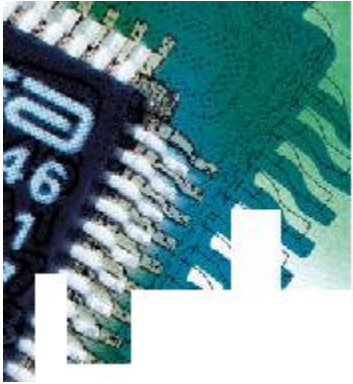
Communication
through innovation



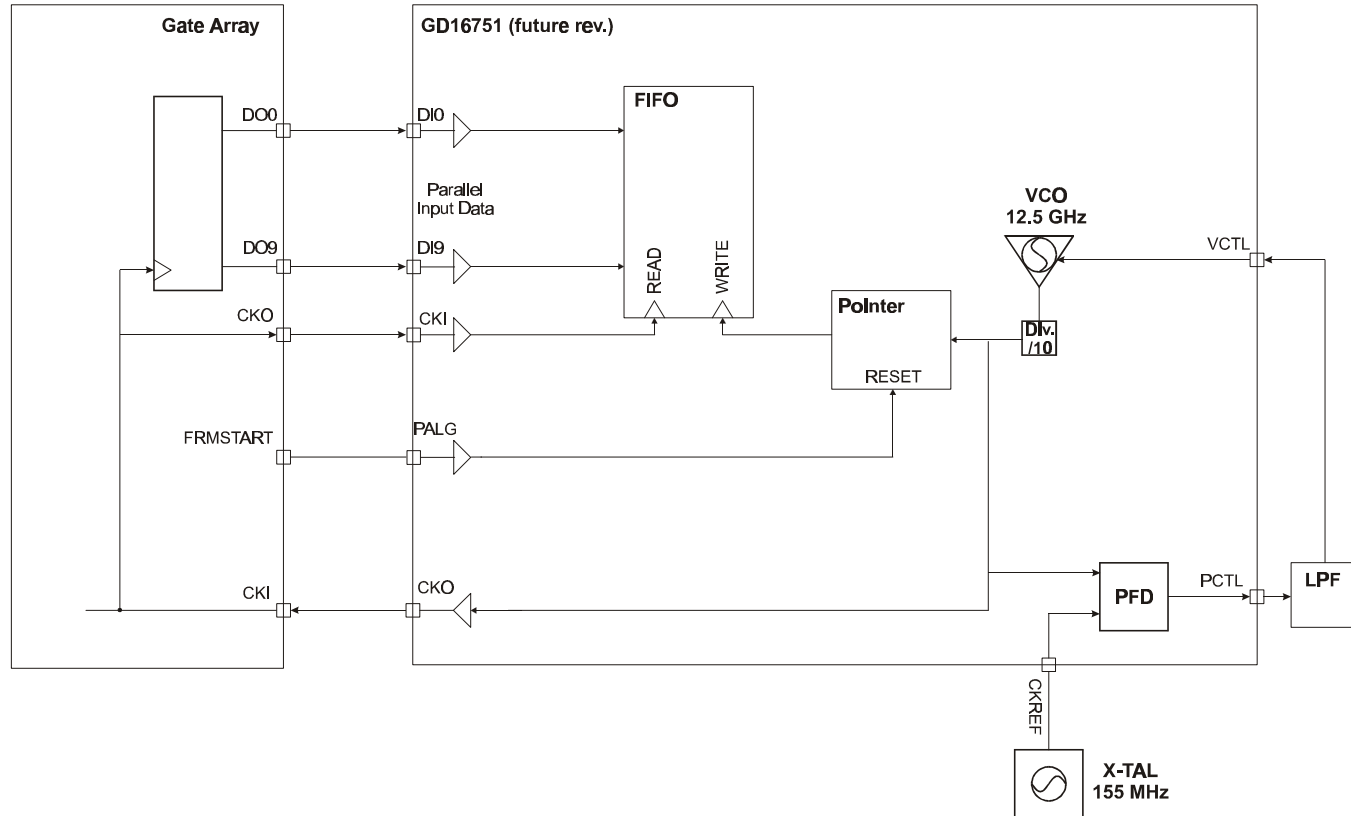
Serializer Clocking

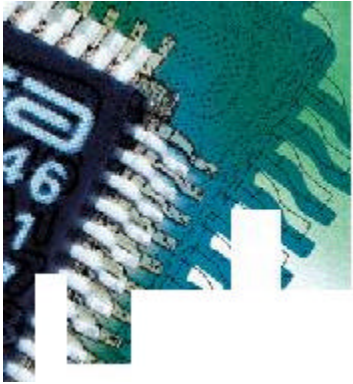


Communication
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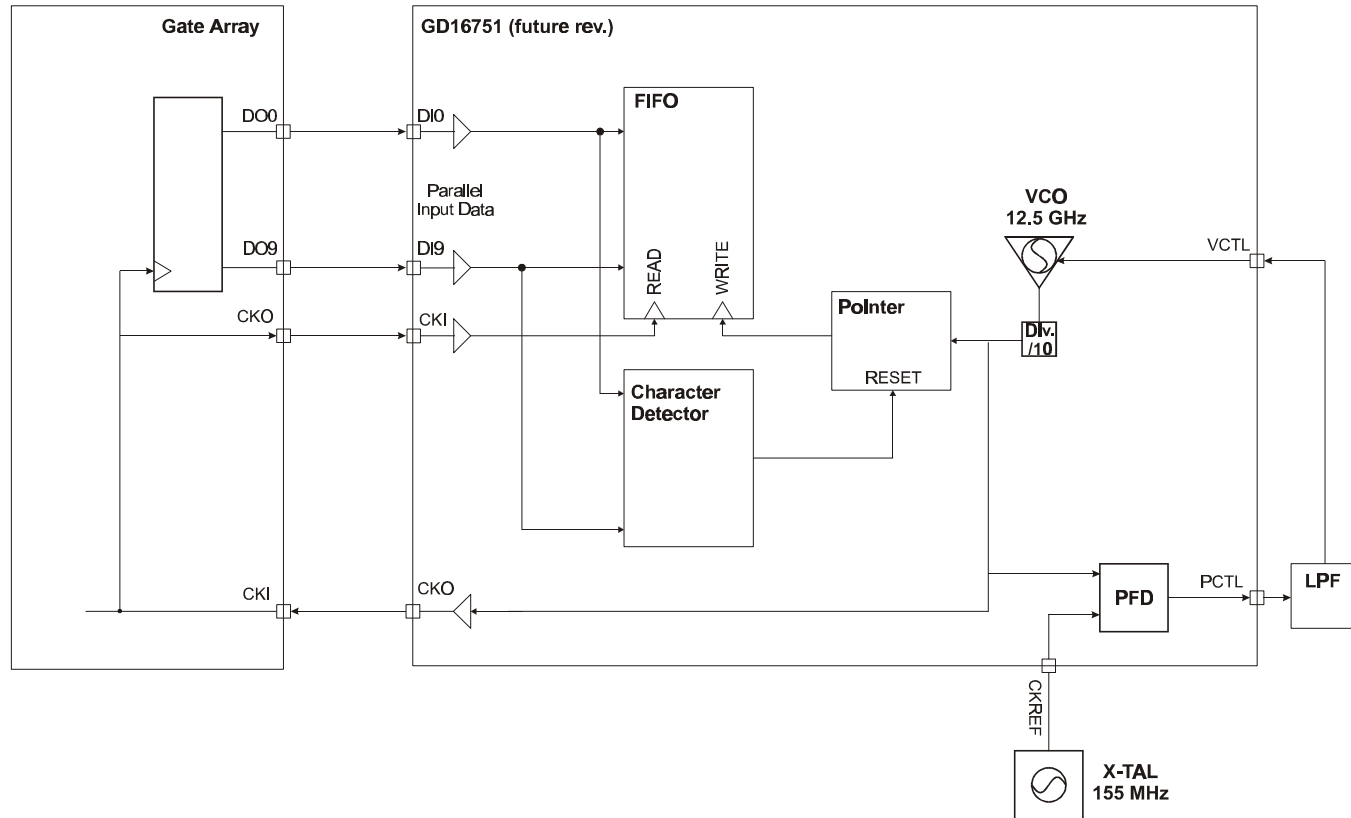


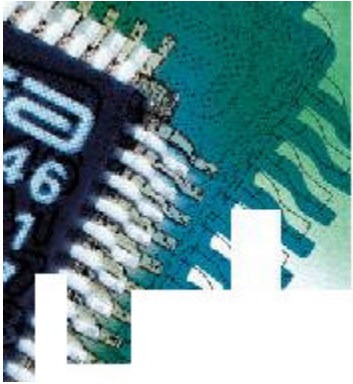
Dynamic Phase Alignment





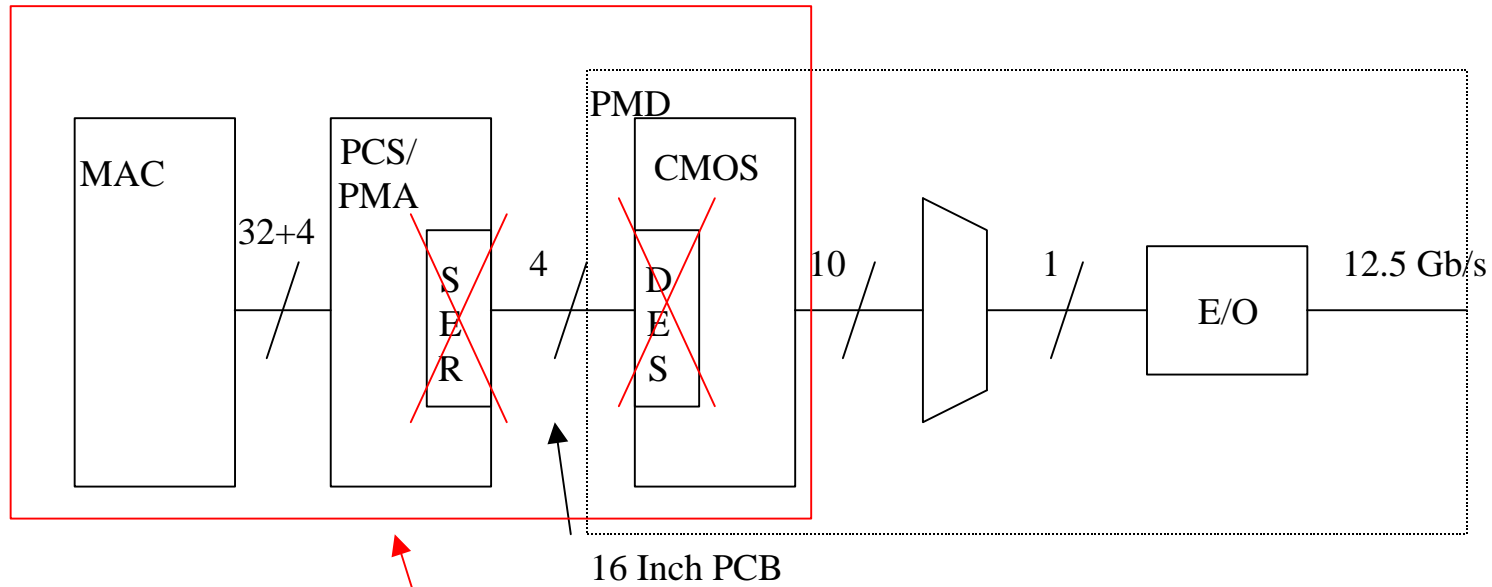
Dynamic Phase Alignment





LAN PHY w/ Serial PMD

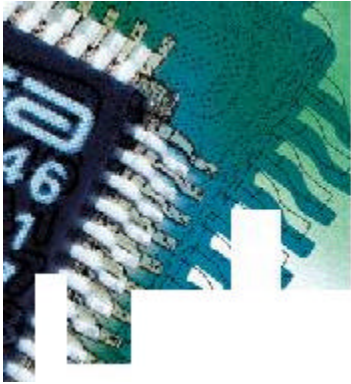
Only transmit path shown for simplicity



If you don't need this
You can put this in one chip
And save this (X)

GIGA

Communication
through innovation



Conclusions

Direct scaling of GE is ...

- Possible
- ... NOW!
- Allows “easy” upgrade of existing architecture
- Uses today's technology, leaving WDM for future, even faster WAN systems (e.g. 4 × 10 Gb/s)

And should be allowed by the standard