

48A.3 Mixed frequency test pattern

The intent of this test pattern is to test the combination of RJ and deterministic jitter (DJ). This mixed frequency test pattern generates a one, or light on, for a duration of 5 bit times, followed by a zero, or light off, for a duration of 1 bit times, followed by a one for 1 bit time followed by a zero for 1 bit time followed by a one for 2 bit times followed by a zero for 5 bit times followed by a one for 1 bit time followed by a zero for 1 bit time followed by a one for 1 bit time followed by a zero for 2 bit times. This pattern repeats continuously for the duration of the test. For example:
1111101011000001010011111010110000010100...

NOTE—This pattern can be generated by the repeated transmission of the K28.5 code-group. Disparity rules are followed.

48A.4 Continuous random test pattern (CRPAT)

The Continuous random test pattern is intended to provide broad spectral content and minimal peaking that can be used for the measurement of jitter at either a component or system level.

NOTE—The derivation of this pattern may be found in NCITS TR-25:1999, “Methodology of Jitter Specification”. This Annex uses similar modifications to fit the RPAT test pattern into an 802.3 frame.

The continuous random test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within delimiters as specified in clause 48 in the ordinary way. The contents of each packet is composed of the following octet sequences, as observed at the XGMII, before 8B/10B coding.

Each packet in the continuous random test pattern consists of 8 octets of PREAMBLE/SFD, followed by 1488 data octets (124 repetitions of the 12-octet modified RPAT sequence), plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE. The Modified RPAT sequence is repeated on each lane:

PREAMBLE/SFD:

55 55 55 55 55 55 55 D5

MODIFIED RPAT SEQUENCE (LOOP 124 TIMES, 31 TIMES ON EACH of 4 LANES)

BE D7 23 47 6B 8F B3 14 5E FB 35 59

CRC

F8 79 05 59

IPG

00 00 00 00 00 00 00 00 00 00 00 00

END

48A.5 Continuous jitter test pattern (CJPAT)

The Continuous jitter test pattern is intended for receiver jitter by exposing a receiver's CDR to large instantaneous phase jumps. The pattern alternates repeating low transition density patterns with repeating high transition density patterns. The repeating code-group durations should be longer than the time constants in the receiver clock recovery circuit. This assures that the clock phase has followed the systematic pattern jitter and the data sampling circuitry is exposed to large systematic phase jumps. This stresses the timing margins in the received eye. The following test bit sequences are proposed for receive jitter testing.

NOTE—The derivation of this pattern may be found in NCITS TR-25:1999, "Methodology of Jitter Specification". This Annex uses similar modifications to fit the JTPAT test pattern into an 802.3 frame.

The Continuous jitter test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within delimiters as specified in clause 48 in the ordinary way. The contents of each packet is composed of the following octet sequences, as observed at the XGMII, before 8B/10B coding.

Each packet in the continuous random test pattern consists of 8 octets of PREAMBLE/SFD, followed by 1504 data octets, plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE. The Modified JTPAT sequence is repeated on each lane:

PREAMBLE/SFD:

55 55 55 55 55 55 55 D5

MODIFIED JTPAT SEQUENCE

7E for 528 Bytes - Low Density Transition Pattern;

F4 for 4 Bytes - Phase Jump;

EB for 4 Bytes - Phase Jump;

F4 for 4 Bytes - Phase Jump;

EB for 4 Bytes - Phase Jump;

F4 for 4 Bytes - Phase Jump;

EB for 4 Bytes - Phase Jump;

F4 for 4 Bytes - Phase Jump;

AB for 4 Bytes - Phase Jump;

B5 for 160 Bytes - High Density Transition Pattern

F4 for 4 Bytes - Phase Jump;

EB for 4 Bytes - Phase Jump;

F4 for 4 Bytes - Phase Jump;

EB for 4 Bytes - Phase Jump;

F4 for 4 Bytes - Phase Jump;

EB for 4 Bytes - Phase Jump;

F4 for 4 Bytes - Phase Jump;

1 EB for 4 Bytes - Phase Jump;
2 7E for 528 Bytes - Low Density Transition Pattern;
3
4 F4 for 4 Bytes - Phase Jump;
5 EB for 4 Bytes - Phase Jump;
6 F4 for 4 Bytes - Phase Jump;
7 EB for 4 Bytes - Phase Jump;
8 F4 for 4 Bytes - Phase Jump;
9 EB for 4 Bytes - Phase Jump;
10 F4 for 4 Bytes - Phase Jump;
11 EB for 4 Bytes - Phase Jump;
12 F4 for 4 Bytes - Phase Jump;
13 AB for 4 Bytes - Phase Jump;
14 B5 for 160 Bytes - High Density Transition Pattern
15 F4 for 4 Bytes - Phase Jump;
16 EB for 4 Bytes - Phase Jump;
17 F4 for 4 Bytes - Phase Jump;
18 EB for 4 Bytes - Phase Jump;
19 F4 for 4 Bytes - Phase Jump;
20 EB for 4 Bytes - Phase Jump;
21 F4 for 4 Bytes - Phase Jump;
22 EB for 4 Bytes - Phase Jump;
23 F4 for 4 Bytes - Phase Jump;
24 EB for 4 Bytes - Phase Jump;
25 F4 for 4 Bytes - Phase Jump;
26 EB for 4 Bytes - Phase Jump;
27 F4 for 4 Bytes - Phase Jump;
28 EB for 4 Bytes - Phase Jump.
29

Editors' Note: To be removed prior to final publication. The number of times that the low/high data values are repeated in the frame may need to be adjusted to account for line rate differences between Fibre Channel and 10GBASE-LX4. For example the low high values above are repeated twice within a maximum length 802.3 frame.

30
31
32
33
34
35 CRC
36
37 D5 7A 06 01
38
39 IPG
40
41 00 00 00 00 00 00 00 00 00 00 00
42
43 END
44
45
46
47
48
49
50
51
52
53
54