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OPEN Alliance BroadR-Reach® (OABR) Physical Layer Transceiver Specification For Automotive Applications

V3.1

May 21st, 2014

Broadcom Corporation

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PREFACE

While every precaution has been taken in the preparation of this specification, Broadcom assumes no responsibility for errors or omissions, and makes no warranties, expressed or implied, of functionality or suitability for any purpose.

Revisions History

REVISION #	DATE	NOTES
Draft 1.0	Feb. 15, 2010	Initial Draft
Draft 1.1	Feb. 24, 2010	Updated Sections 3 and 4
Draft 2.0	March 4, 2010	Created/Updated Sections 1,2,4,5 6,7, 8, 9 and Annex 1A & 1B
Draft 2.1	March 25, 2010	Misc. Corrections
Draft 2.2	May 19, 2011	TBDs are defined
Draft 2.3	June 14, 2011	Misc. Corrections
Draft 2.4	August 1, 2011	Misc. corrections & definitions are added
Draft 2.5	Jan 30, 2012	Updated Section 1.9, 3.3.1, 5.4.3; Updated Section 3.3.4 & 5.4.5; Misc. clarifications & definitions are added
Version 1.0	March 14, 2012	First OPEN release
Version 1.1	November 15th, 2012	Updated Sections 3.2, 3.3, 5.4.2, 5.4.4, 7.1; Added Sections 5.1.1, 5.1.2, 5.5.3, 7.2, 8.2.2, references Misc. clarifications & definitions are added
Version 1.2	January 24th, 2013	Removed Section 3.4. Misc. clarifications are added
Version 2.0	November 1st, 2013	Updated Section 1.8.11, 1.8.15, 1.8.16, 3.2.3, 3.2.4.4.4, 3.3.1.1, 5.2, 5.3, 5.4, 7.1.2, 7.1.3, 8.2.2, References; Misc. clarifications are added
Version 2.0.1	April 18th, 2014	Updated Preface, and Section 3.2.4.6 (Generation of symbol sequence) for editorial clarification
Version 3.0	May 7, 2014	Editorial changes prior to submission to IEEE 802.3 1TPCE Study Group. Changes include reference to IEEE 802.3-2012 Clauses, from references to IEEE 802.3ab. Section numbers changed due to general formatting associated with the change.
Version 3.1	May 21, 2014	Editorial changes for typographical corrections, inclusion of the mode conversion limit line in Section 7.1.4.

Abstract:

Type BroadR-Reach PCS (BR-PCS), type BroadR-Reach PMA sublayer (BR-PMA), and type BroadR-Reach Medium Dependent Interface (BR-MDI), used in BroadR-Reach PHY (BR-PHY) are defined. This specification provides fully functional and electrical specifications for the type BR-PHY. This specification also specifies the baseband medium used with BroadR-Reach.

Keywords:

Automotive Cable, BroadR-Reach, Copper, Ethernet, Gigabit, MASTER-SLAVE, Medium Dependent Interface, Physical Coding Sublayer, Physical Layer, Physical Medium Attachment.

1.0 OVERVIEW

BroadR-Reach® is a Broadcom® point-to-point Ethernet PHY technology, adopted by the OPEN Alliance (http://www.opensig.org) as the OPEN Alliance BroadR-Reach PHY (OABR PHY), that specifies a PHY operating full-duplex over one pair of unshielded twisted pair (UTP) cable at 100 Mb/s.

BroadR-Reach Physical Layer (BR-PHY) Transceiver supports standard media access controller (MAC) interfaces via MII (IEEE Standard 802.3 Clause 22). For Automotive applications, each copper port supports one twisted pair line connection. BroadR-Reach provides data rate of 100 Mb/s at the MAC interface over one pair of UTP cable.

This specification, with reference to IEEE Standard 802.3-2012, defines the BroadR-Reach PHY type, operating at 100 Mb/s, Physical Coding Sublayer (BR-PCS) and type Physical Media Attachment (BR-PMA) sublayer. Together, the BR-PCS and the BR-PMA sublayers comprise the BroadR-Reach Physical layer (BR-PHY).

This specification is written in the spirit of IEEE 802.3 [1] standard, and intended to be an interoperable specification. BroadR-Reach PHY follows the common practice used in IEEE 802.3 baseband PHY specifications, where the transmit path is completely defined and the receiver is left to the implementer. It is suggested that this specification is reviewed in conjunction with IEEE Standard 802.3, and in particular, 100 Mb/s PHY (Clauses 21 through 25) and 1000 Mb/s PHY (Clauses 34 through 40) (which can be obtained from http://standards.ieee.org/about/get/802/802.3.html).

1.1 *Objectives*

The followings are the objectives of BR-PHY:

a) Provide a PHY that supports full duplex operating at 100 Mb/s over one pair unshielded twisted pair (UTP) or better cable.

b) Provide compatibility with the MII (IEEE 802.3 Clause 22) and IEEE 802.3 MAC operating at 100 Mb/s.

c) Bit Error Rate of less than or equal to 1e-10 over a nominal channel (over a one pair UTP cable).

1.2 *Relationship of BR-PHY to other Ethernet PHYs*

IEEE 802.3 1000BASE-T, or Gigabit, PHY is specified in Clause 40 of IEEE Standard 802.3-2012, and it operates over four pairs of a channel compliant with its Clause 40.7. In contrast, BR-PHY operates over one pair channel.

BR-PHY provides features that are comparable to the standard Ethernet product specified in IEEE 802.3. BR-PHY architecture interfaces to IEEE 802.3-2012 Clause 22 MII. BR-PMA is similar to Clause 40 of IEEE 802.3-2012, but with significant differences in BR-PCS, as specified in Section 3.0.

BR-PMA functionality is defined in Section 4.0 with reference to Clause 40 of IEEE 802.3. The BR-PCS and BR-PMA functions are illustrated in Figure 1-2, which are presented in Sections 3.0 and 4.0.

BR-PHY leverages 1000BASE-T PHYs, with parts of IEEE 802.3 100BASE-TX in operation at 100 Mb/s, and introduces new PCS, PMA, and other modifications in support of BR-PHY. The following are the similarities and differences from BR-PHY architecture to the 1000BASE-T and 100BASE-TX architectures.

The design features that enable achieving the objectives are:

- Adopt full-duplex communication (and therefore echo cancellation) on a single twisted pair channel to reduce cabling while preserving Ethernet MAC compatibility
- Adopt Pulse Amplitude Modulation 3 (PAM3) to help minimize the bandwidth such that communication occurs in the best part of a twisted pair channel, reduce EMI, and allow a more aggressive EMC filtering and also allow for lower cost (often lower quality) cabling

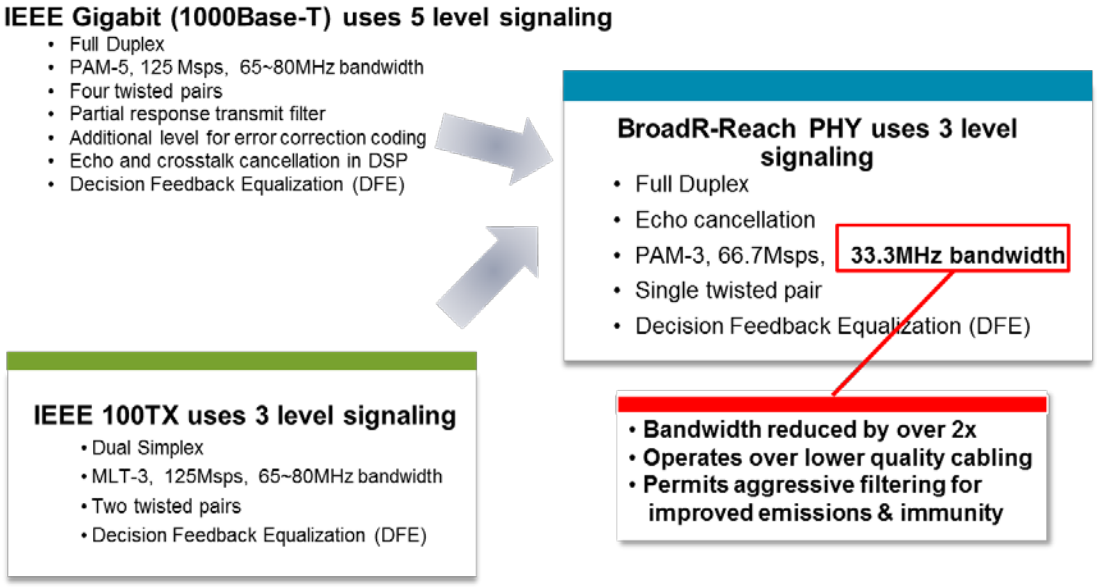


Figure 1-1 BR-PHY relationship to other IEEE 802.3 PHYs

Section 5.0 presents the BR-PMA Electrical specifications.

Section 6.0 defines the Management Interface.

Sections 7.0 and 8.0 cover the Link Segment specification and MDI for Automotive application.

Section 9.0 defines the delay constraints of BroadR-Reach PHY.

References are made herein to IEEE 802.3 and differences are outlined accordingly.

1.3 *Physical Coding Sublayer (PCS)*

BR-PCS transmits/receives signals to/from a Media Independent Interface (MII) as described in IEEE 802.3 Clause 22, to/from signals on a BroadR-Reach PMA, which supports one pair twisted pair medium.

1.4 *Physical Medium Attachment (PMA) sublayer*

BR-PMA transmits/receives signals to/from the BR-PCS onto the balanced one pair twisted pair cable medium and supports the link management and BR-PHY Control function. The BR-PMA provides full duplex communications at 100 Mb/s.

1.5 *Signaling*

BroadR-Reach signaling shares the same objectives as the Clause 40.1.4 of the IEEE 802.3 Standard b) with the exception that change "…octet data to a quartet symbols" to "…nibble data to ternary symbols…", c), d) with the exception that "on any pair combination" is not relevant to a single pair system, g), h), and i)

1.6 *Notation*

Notation definitions in Clause 1.2.1 in IEEE 802.3-2012 are used in State diagrams, variable definitions, etc., in this specification.

1.7 *Service specification*

Service specification methods in Clause 1.2.2 in IEEE 802.3-2012 are used in this specification.

1.8 *Timer specification*

All timers operate in the manner described in IEEE 802.3-2012 Clause 40.4.5.2.

1.9 *Reference Notation and Legends*

1.9.1 References to IEEE 802.3-2012

References to IEEE 802.3-2012 are made throughout this specification. To help make it easier to the reader, the following designations used,

often in differences table between this specification and the IEEE 802.3-2012 standard.

1.9.1.1 No Change – NC

No changes to the referenced respective clause(s) in IEEE 802.3-2012 and deemed normative.

1.9.1.2 Local Definition – LD

The terminology, heading, etc., may take on the same wording as the IEEE 802.3-2012 standard, but the definition takes on new definition and/or normative specification in this document, e.g. the PCS Sublayer may use similar construct as the IEEE 802.3-2012 standard, but the PCS Sublayer in BR-PHY is largely unique to this BroadR-Reach specification.

1.9.1.3 Modified Definition – MD

The terminology, heading, etc., may take on the same wording as the IEEE 802.3-2012 standard, and the definition takes on appropriate modified definition and/or normative specification in this document, e.g. specification related to GMII in Clause 40 of IEEE 802.3-2012 is modified to relate to MII.

1.9.1.4 DIFF statements

Local notation of "**DIFF**: <editing instructions>" to make it clearer to the readers when Clauses from IEEE 802.3-2012 are referenced with changes. An example is as follows.

DIFF: change <text string 1> to <text string 2>, or
delete the sentence <text string 3>.

In this example, <text string 1> is from the text used in the referenced clause in IEEE 802.3-2012, <text string 2> is the text to replace <text string 1> to compose BR-PHY specification.

If there is a conflict between the DIFF statement and text, the text is normative and overrules the DIFF statement.

1.9.2 Red Fonts and Orange Blocks in Diagrams

Text in Red notes a change from the referenced state machine diagrams in IEEE 802.3 Standard, and Orange color blocks note States that may be of the same or similar name, but functionality therein are defined in this document.

These emphases are added to help to make it clearer to the readers to distinguish major changes, and any color coded emphases themselves is not normative part of this standard.

1.9.3 Use of “BR-“ prefix

The prefix “BR-“ with PHY, PCS, etc., e.g. BR-PHY, BR-PCS, BR-PMA, is used to help clarify which sublayer being referred. For example, “BR-PCS” is the PCS (Physical Coding Sublayer) of a BroadR-Reach PHY. This use is liberal and intended to help to make this standard text clearer to the readers. Use of the sublayer name, i.e. without the prefix, is used when there is little room for confusion.

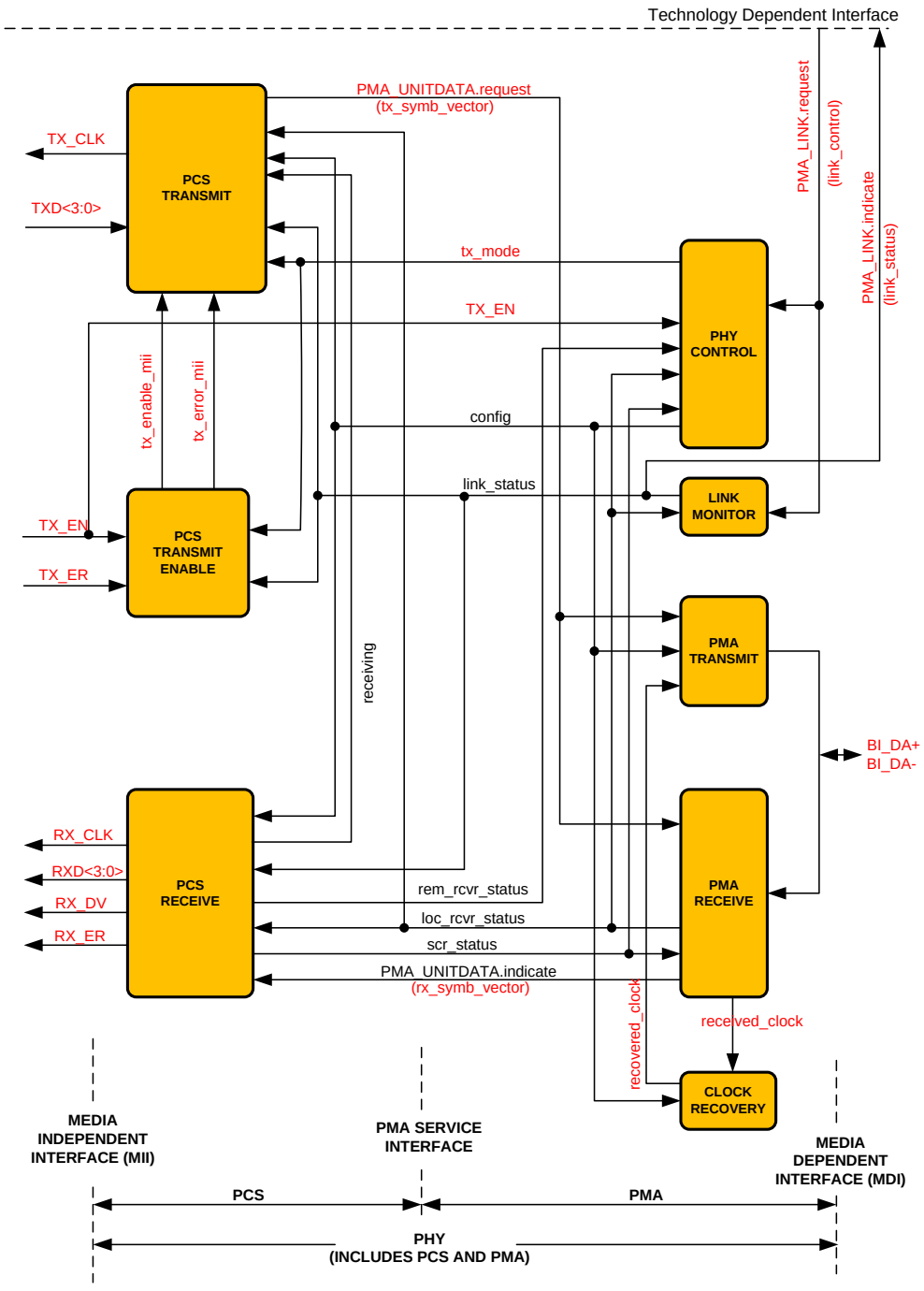


Figure 1-2 Functional Block Diagram, noting the differences from IEEE 802.3 Figure 40-3

Note: Please refer to Figure 40-3 in IEEE 802.3 Clause 40 for a good illustration of PCS and PMA functional relationship.

The BR-PHY supports normal operation and link training operation. In training operation, the BR-PCS ignores signals from MII and sends only the idle signals to the BR-PMA until training process is complete (signaled by the link partner). The training process usually includes descrambler lock, timing acquisition, echo cancellation and equalizer convergence, etc.

1.10 *Compatibility*

All BR-PHY implementations are compatible at the MDI and shall be compliant to IEEE 802.3 Clause 22 MII. This specification may be implemented in variety of methods between these two interfaces.

1.11 *Compliance and Completeness*

This specification contains textual descriptions, specifications, state machines, variables, functions and procedures. Reasonable efforts were made to make this specification complete and correct. Should any unclear or conflicting behavior be found, please contact via e-mail: BR-info-list@broadcom.com.

The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

1.12 *Definitions*

The terminology and their definitions used in this document are chosen to reduce any ambiguity, and those chosen to be in common with IEEE 802.3-2012 are listed in Table 1-1. Any differences and exceptions are noted.

New Terminology in this Standard

1.12.1 **Automotive Cabling:**

Balanced 100 Ω one pair cable and associated hardware having specified transmission characteristics are provided in Section 7.1.

1.12.2 **4B3B:**

In BR-PHY, the data encoding technique used by BR-PHY when converting MII data (4B-4 bits) with 25 MHz clock to 3 bits (3B) wide of data that is transmitted during one $33\frac{1}{3}$ MHz clock period. (See Section 3.2)

1.12.3 **1D-PAM3:**

The symbol encoding method used in BR-PHY is 1D-PAM3. The one-dimensional ternary (1D) code groups from BR-PCS Transmit (See Section 3.2) are transmitted using three voltage levels (PAM3). One symbol is transmitted in each symbol period.

1.12.4 **PHY-Initialization:**

The fast link acquisition requirement for automotive application prohibits using the IEEE 802.3 auto-negotiation process (which could take a few seconds). A primitive PHY-Initialization procedure is used for MASTER and SLAVE assignment. The start-up procedure, from link_control=ENABLE to valid data, shall be completed within 200 ms for BroadR-Reach channel compliant 1-pair 15m UTP link segments.

1.12.5 **Side-Stream Scrambling:**

In BR-PHY, a data scrambling technique, used by BR-PCS to randomize the sequence of transmitted symbols and avoid the presence of spectral lines in the signal spectrum. Synchronization of the scrambler and descrambler of connected PHYs is required prior to operation defined in 3.2.4.

Table 1-1 Terminology Common with IEEE 802.3-2012

IEEE 802.3-2012, reference clause & terms	BR-PHY	Notes
Code Group (1.4.142)	A set of ternary PAM3 symbols (out of 9 possible combinations), when representing data, conveys 3 bits, as defined in Section 3.3.1.	LD – new Local Definition for BR-PHY
Control mode (1.4.157)	TX_EN reference is to MII and when TX_EN is set to FALSE, End-of-	MD – Modified for BR-PHY

	Stream (ESD) symbols are transmitted **DIFF**: change “1000BASE-T” to “BR-PHY”. change “..occurs when the GMII..” to “..occurs when the MII”, and delete “These include two …”, and delete “(See IEEE…40.)”	
Data mode (1.4.163)	TX_EN reference is to MII and TXD<3:0> is used. When TX_EN is set TRUE for data transmission. This mode begins with transmission of Start-of-Stream delimiter code-groups followed by code-groups encoded from the data nibbles arriving on TXD<3:0> via the MII. (See Section 3.2). **DIFF**: change “1000BASE-T” to “BR-PHY”. change “..which the GMII..” to “..which the MII”, change “..arriving on TXD<7:0> via the GMII.” to “..arriving on TXD<3:0> via the MII.”, and delete “(See IEEE…40.)”	MD – Modified for BR-PHY
End of Stream delimiter (ESD), (1.4.183)	This delineates data transmission from idle. ESD consists of the code-group of 3 consecutive ternary pairs named as ESD1-3 as defined in Section 3.3.1 of this specification.	LD – new Local Definition for BR-PHY
Medium Dependent Interface (MDI), (1.4.256)	Note: The same definition to be applied to BR-PHY	NC – No change
Multiport Device (1.4.265)	Note: No change	NC – No change
Physical Coding Sublayer (PCS), (1.4.313)	A sublayer used in the PHY between the Media Independent Interface (MII) and the Physical Medium Attachment (BR-PMA). The BR-PCS encodes data from MII into code-groups that are transmitted over the physical medium as specified in Section 3.0, and decodes received code-groups from the physical medium into data to MII.	LD – new Local Definition for BR-PHY

Physical Layer entity (PHY), (1.4.314)	Note: The same definition that are relevant to 100 Mb/s system, i.e. MII, applied to BR-PHY	NC – No change
Physical Medium Attachment (PMA) sublayer, (1.4.315)	The functions that reside between BR-PCS and PMD, i.e. transmission/reception of code group, and (depending on the MASTER/SLAVE status) clock recovery. (See Section 4.0)	ND – New local Definition for BR-PHY
receiver training (1.4.340)	This is a start-up routine for MASTER/SLAVE PHYs to get receivers ready to operate in normal data mode. It includes (but is not limited to) scrambler synchronization, echo cancellation, equalizer convergence and timing acquisition.	LD – new Local Definition for BR-PHY
Retraining (1.4.350)	Note: The same definition to be applied to BR-PHY **DIFF**: change “connected 100BASE-T2…1000BASE-T” to “connected BR-PHY”	MD – Modified for BR-PHY
Single-port device (1.4.368)	Note: No change.	NC – No Change
Start-of-Stream Delimiter (SSD) (1.4.377)	A code-group pattern between two distinct data transmission onto MDI. SSD consists of the code-group of 3 consecutive ternary pairs named as SSD1-3 as defined in Section 3.3.1 of this specification.	LD – new Local Definition for BR-PHY
symbol (1.4.380)	Note: The same definition to be applied to BR-PHY that uses ternary symbols.	NC – No Change
symbol period (1.4.381)	In BR-PHY, this is 15 ns. **DIFF**: change “1000BASE-T” to BR-PHY, and change “eight nanoseconds” to “fifteen nanoseconds”.	MD – Modified for BR-PHY
symbol rate (SR), (1.4.382)	The same definition to be applied to BR-PHY with the symbol rate of $66\frac{2}{3}$ MBd. **DIFF**: add “for BR-PHY, the symbol rate is $66\frac{2}{3}$ MBaud.” at the end of the	MD – Modified for BR-PHY

	existing definition.	
Ternary Symbol, (1.4.385)	Note: The same definition to be applied to BR-PHY (See 3.2.4.5). **DIFF**: change “100BASE-T4” to “BR-PHY” and delete “(See IEEE… 23)”).	MD – Modified for BR-PHY
twisted pair (1.4.396)	Note: No change.	NC
unit interval (UI) (1.4.409)	Note: No change.	NC
unshielded twisted-pair cable (UTP) (1.4.410)	Note: No change.	NC

2.0 BR-PHY Service Primitives and Interfaces

BR-PHY adopts the Service Primitives and Interfaces in IEEE 802.3-2012 Clause 40.2, with exception of the following clarifications and differences noted in this section, in support of 100 Mb/s operations over a one twisted pair channel.

General Clarifications and Differences

a) BR-PHY uses Media Independent Interface (MII) as specified in IEEE 802.3-2012 Clause 22.
b) BR-PHY does not use IEEE 802.3-2012 Clause 40.2 support of LPI (Low Power Idle) related functions.
c) BR-PHY does not use IEEE 802.3-2012 style auto-negotiation due to associated latency that does not meet start-up time requirements of automotive networks. BR-PHY uses FORCE mode.

The specific clarifications and differences are specified Section 2.1 Technology-Dependent Interface, and Section 2.2 BR-PMA Service Interface.

2.1 *Technology Dependent Interface*

BR-PHY incorporates the IEEE 802.3-2012 Clause 40.2.1 with the following specific clarifications and differences. Table 2-1 lists BR-PHY specifications in its relationship to IEEE Standard, and note further clarifications and differences. Only the referenced Clauses are normative for BR-PHY specifications.

Table 2-1 Relationship of Technology Dependent Interface in BR-PHY to Clause 40.2.1 in IEEE 802.3-2012

802.3-2012 Clause 40.2.1	BR-PHY	Notes
40.2.1 (Technology-Dependent Interface)	Note: Control signal as referenced to Clause 28 (Auto-Negotiation) is not used.	MD

	DIFF: change “1000BASE-T” to “BR-PHY”, and change “Interface …Clause 28.” to “Interface.”	
40.2.1.1 (PMA_LINK.request)	Note: Management allows to enable/disable and Clause 28 (Auto-Negotiation) is not used. See Section 4.4 for the definition. **DIFF**: replace the sentence with “This primitive is set by management and FORCE mode configuration.”	LD
40.2.1.1.1 (Semantics of the primitive)	Note: SCAN_FOR_CARRIER is not an allowed value and Auto-Negotiation is not used. **DIFF**: change “values: SCAN_FOR_CARRIER, DISABLE..” to “values: DISABLE..”, delete “SCAN_FOR_CARRIER Used… FAIL.PHY”, and replace the definition of DISABLE and ENABLE as follows: DISABLE Set by the BR-PHY-initialization. BR-PHY processes are disabled. This allows the BR-PHY-initialization to determine how to configure the link ENABLE Set by management and used by BR-PHY-initialization to turn control over to the BR-PHY for data processing functions.	LD
40.2.1.1.2 (When generated)	Note: link_control is set by management or FORCE mode as defined in see Section 4.4	LD

	DIFF: replace the sentence with "link_control is set by management and FORCE mode configuration."	
40.2.1.1.3 (Effect of receipt)	Note: The same definition, except that BR-PMA Link Monitor function is defined in Section 4.5. **DIFF**: change "..in 40.4.2.5" to "..in Section 4.5".	MD
40.2.1.2 (PMA_LINK.indication)	Note: The same definition, except that BR-PMA Link Monitor function informs status of the underlying link as defined in Section 4.5. **DIFF**: change "..in 28.2.6.1" to "..in Section 4.5", and delete "…, and Auto-Negotiation… underlying link.".	MD
40.2.1.2.1 (Semantics of the primitive)	Note: The same definition, except the value READY (associated with Auto-Negotiation) is not used. **DIFF**: delete "READY The Link… be established.", change "..valid 1000BASE-T link.." to "valid BR-PHY link..".	MD
40.2.1.2.2 (When generated)	Note: The same definition, except with the reference to Section 4.5. **DIFF**: change "..in Figure 40-17." To "..in Section 4.5.".	MD
40.2.1.2.3 (Effect of receipt)	Note: The same definition, except with a reference to Section 4.5. **DIFF**: change "specified in 40.3.3.1".	MD

	to “..specified in Section 4.5.”.	

2.2 *BR-PMA Service Interface*

BR-PMA the same Service interface uses the IEEE 802.3-2012 Clause 40.2.2 PMA Service Interface, as indicated in Figure 2-1, with the exceptions that the following optional service primitives associated with LPI are NOT used in BR-PMA:

PMA_LPIMODE.indication,
PMA_LPIREQ.request,
PMA_REMLPIREQ.request,
PMA_UPDATE.indication, and
PMA_REMUPDATE.request

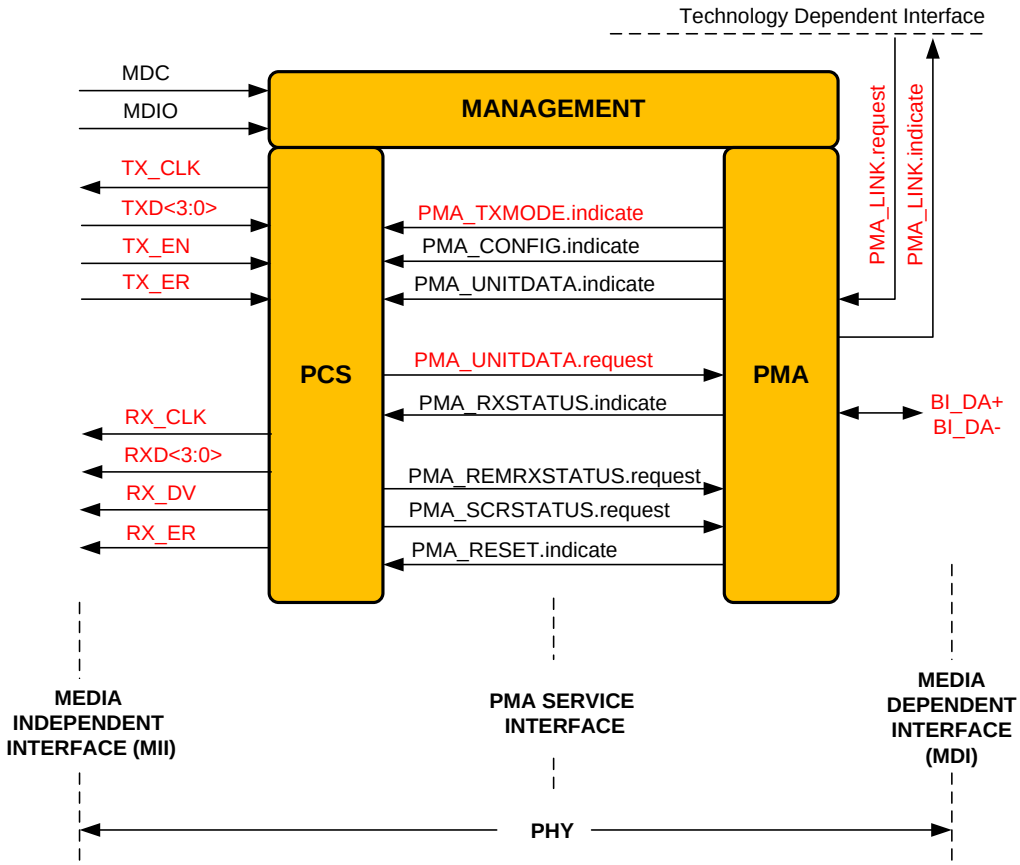


Figure 2-1: BR-PHY PMA services interfaces, noting the differences from IEEE 802.3 Figure 40-4

2.3 *BR PMA Service Primitives*

BR-PMA incorporates the IEEE 802.3-2012 Clause 40.2.3 through 40.2.10 with the following specific clarifications and differences. Table 2-2 lists BR-PMA specifications in its relationship to IEEE Standard, and note further clarifications and differences. Only the referenced Clauses are normative for BR-PMA specifications.

Table 2-2 Relationship of BR-PMA to Clause 40.2.3 in IEEE 802.3-2012

802.3-2012 Clause 40.2.3	BR-PMA	Notes
40.2.3 (PMA_TXMODE.indi	Note: The same definition, except for BR-PHY link (from 1000BASE-T link) and	MD

cation)	over the one pair (from four pairs) to MII (from GMII). **DIFF**: change “1000BASE-T” to “BR-PHY”, “..the four pair,” to “..the one pair,”, and “GMII” to “MII”.	
40.2.3.1 (Sementics of the primitive)	Note: The same definition, except SEND_N pertains to MII data stream (from GMII), and SEND_I and SEND_Z as defined in 3.2.4.5. **DIFF**: change “…representing GMII data…” in SEND_N description to “…representing MII data..”.	MD
40.2.3.2 (when generated)	Note: The same definition.	NC
40.2.3.3 (Effect of receipt)	The same definition, except reference to Section 3.2. **DIFF**: change “…in 40.3.1.3.” to “…in Section 3.2.”.	MD
40.2.4 (PMA_CONFIG.indication)	In BR-PHY link, MASTER-SLAVE configuration is determined during by FORCE mode. Note: Auto-Negotiation is not used. **DIFF**: change “..a 1000BASE-T..” to “..a BR-PHY..”, change “..determined during…(40.5).” to “..determined by FORCE mode.”.	LD
40.2.4.1 (Semantics of the primitive)	Note: The same definition.	NC
40.2.4.2 (When generated)	Note: The same definition.	NC

40.2.4.3 (Effect of receipt)	Note: The same definition.	NC
40.2.5 (PMA_UNITDATA.request)	Note: The same definition, except encoding rules are defined in Section 3.2 of this specification to represent MII.	MD
40.2.5.1 (Semantics of the primitive)	Note: The same definition, except for BI_DB, BI_DC, BI_DD are not used, because BR-PMA uses only one transmit pair. **DIFF**: change "..over each of the four transmit pairs…" to "..over one transmit pair.."; change "BI_DA, DI_DB, BI_DC, and BI_DD." to "BI_DA"; change the paragraph "SYMB_4DA vector of four… +2." to "SYMB_1D: A vector of one ternary symbol transmitted over a single transmit pair BI_DA. Each ternary symbol may take on one of the values {-1, 0, or +1}."; change "The quinary.." to "The ternary…"; and "…called, according … tx_symb_vector[BI_DD]." to "…called tx_symb_vector [BI_DA].".	LD
40.2.5.2 (When generated)	Note: The same definition, except that the primitive uses PMA_UNITDATA.request (SYMB_1D). **DIFF**: change "SYMB_4D" to "SYMB_1D"	MD
40.2.5.3 (Effect of receipt)	Note: The same definition, except that signals received on only one pair, BI_DA.	LD

	DIFF: change "…on pairs BI_DA… BI_DD." to "pair BI_DA."	
40.2.6 (PMA_UNITDATA.indication)	Note: The same definition.	NC
40.2.6.1 (Semantics of the primitive)	Note: The same definition, except for BI_DB, BI_DC, BI_DD are not used, because BR-PMA uses only one transmit pair. **DIFF**: change "…on each of four… BI_DD." to "…on BI_DA."; change the paragraph "SYMB_4DA…+2" to "SYMB_1D: A vector of one ternary symbol for a single transmit pair BI_DA. Each ternary symbol may take on one of the values {-1, 0, or +1}."; change "The quinary symbols…" to "The ternary symbols…"; and change "…are called .. rx_symb_vector [BI_DD]." to "…are called rx_symb_vector [BI_DA].	LD
40.2.6.2 (When generated)	Note: The same definition, except it is changed to PMA_UNITDATA.indication (SYMB_1D) and the nominal rate of the primitive is $66\frac{2}{3}$ MHz. **DIFF**: change "(SYMB_4D)" to "(SYMB_1D)"; and change "...is 125 MHz..." to "…is $66\frac{2}{3}$ MHz…".	MD
40.2.6.3 (Effect of receipt)	Note: The same definition.	NC
40.2.7 (PMA_SCRSTATUS.	Note: The same definition.	NC

request)		
40.2.7.1 (Semantics of the primitive)	Note: The same definition.	NC
40.2.7.2 (When generated)	Note: The same definition.	NC
40.2.7.3 (Effect of receipt)	Note: The same definition, except reference to Sections 4.3, and 4.4. **DIFF**: change "…in 40.4.2.3, 40.4.2.4, and 40.4.6.1" to "…in Sections 4.3, and 4.4.".	NC
40.2.8 (PMA_RXSTATUS.indication)	Note: The same definition.	NC
40.2.8.1 (Semantics of the primitive)	Note: The same definition.	NC
40.2.8.2 (When generated)	**Note: The same definition.**	NC
40.2.8.3 (Effect of receipt)	The same definition, except references to Figure 4-4, Figure 4-5 and Sections 2.0, 4.4, and 4.5. **DIFF**: change "…specified in Figure 40-16a and subclauses 40.2 and 40.4.6.2" to "…specified in Figure 4-4, Sections 2.0, 4.4, and 4.5".	NC
40.2.9 (PMA_REMRXSTATUS.request)	The same definition.	NC
40.2.9.1 (Semantics of the primitive)	The same definition.	NC
40.2.9.2 (When	The same definition.	NC

generated)		
40.2.9.3 (Effect of receipt)	The same definition, except referenced to Figure 4-4, and Sections 2.0, 4.4, and 4.5. **DIFF**: change "…is specified in Figure 40-16a" to "…is specified in Figure 4-4.	MD
40.2.10 (PMA_RESET.indication)	The same definition.	NC
40.2.10.1 (When generated)	The same definition, except reference to Clause 2.1. **DIFF**: change "…is specified in 40.2.1" to "…is specified in Clause 2.1".	MD
40.2.10.2 (Effect of receipt)	The same definition, except reference to Clause 2.1. **DIFF**: change "…is specified in 40.2.1" to "…is specified in Clause 2.1".	MD

3.0 BR-PHY Physical Coding Sublayer (BR-PCS) Functions

This section is analogous to Clause 40.3 of IEEE 802.3-2012 in layering function, but specifies BroadR-Reach PCS (BR-PCS) layer functions.

The BR-PCS performs a 4B3B conversion of the nibbles received at the MII interface, creates the ternary symbols, and then sends the symbols to the PMA for further processing. It receives 4 bits at the MII with 25 MHz clock, and converts the stream of 4-bits at 25 MHz to a stream of 3-bits at the $33\frac{1}{3}$ MHz clock. The bits are then scrambled and converted through BR-PCS encoding to a stream of ternary symbols pairs. These ternary pairs are then multiplexed to a serialized stream of symbols at $66\frac{2}{3}$ MHz. As shown in Figure 3-1, the BR-PCS operating functions are PCS Reset, PCS Transmit, and PCS Receive. PCS passes the 1-D 3 level (+1, 0, -1) coding to the PMA to convert to electrical signaling.

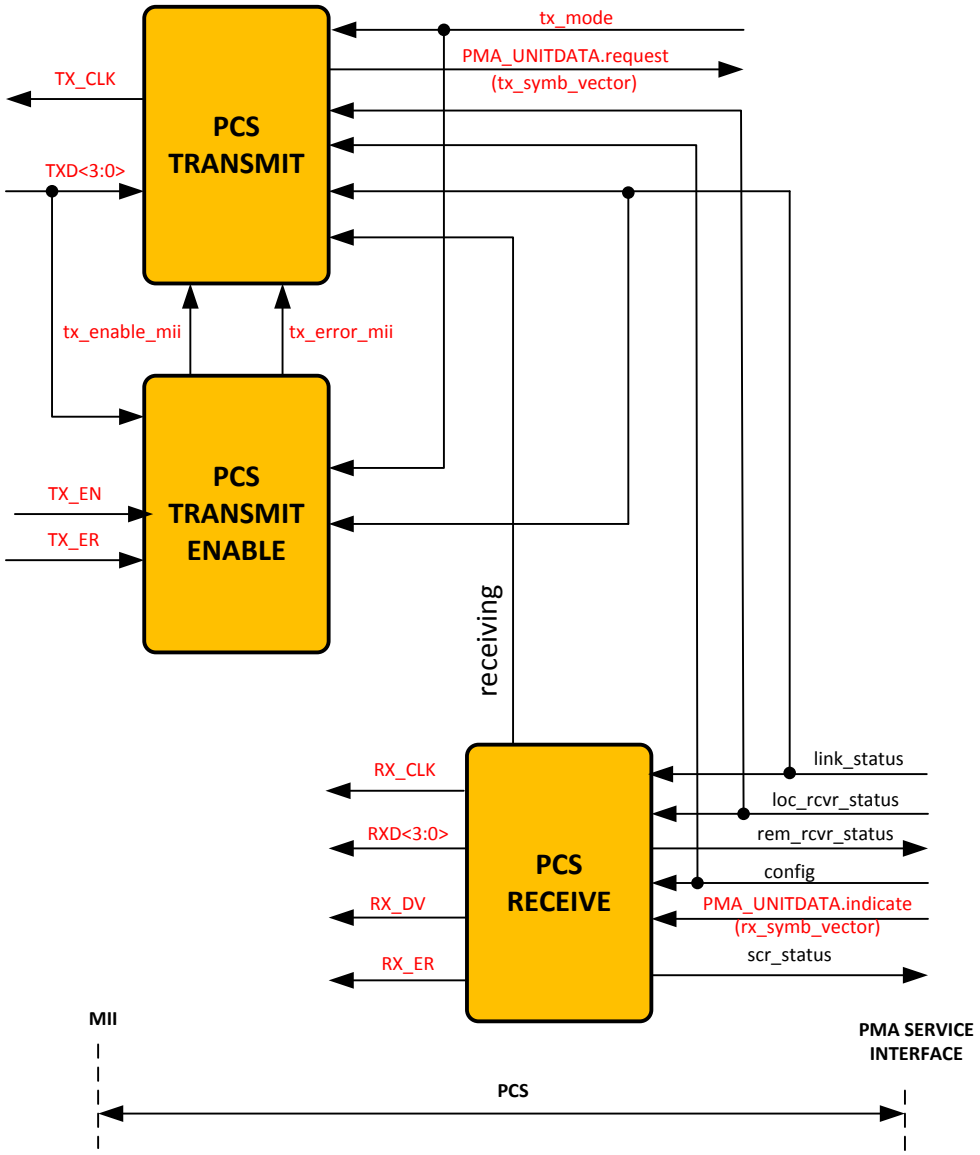


Figure 3-1: BR-PCS reference diagram, noting differences from IEEE 802.3-2012 Figure 40-5

3.1 *PCS Reset function*

This function adopts the Clause 40.3.1.1 of IEEE 802.3-2012 without any exception.

3.2 *PCS Transmit function*

3.2.1 PCS transmit enabling

As depicted in Figure 3-2, the PCS Data Transmission Enabling process generates the signals tx_enable_mii and tx_error_mii, which follow MII signals TX_EN and TX_ER when tx_mode is SEND_N, and set as FALSE otherwise.

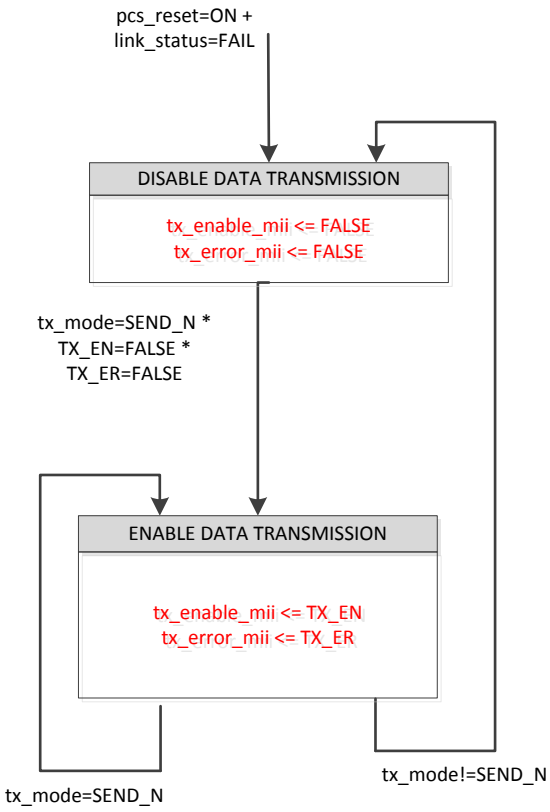


Figure 3-2: PCS Data Transmission Enabling state diagram, noting the differences from IEEE 802.3-2012 Figure 40-8

3.2.1.1 Variables

New Variables in this standard

tx_enable_mii: It is generated by PCS Data Transmission Enabling state diagram as specified in Figure 3-2, and Figure 3-3.

tx_error_mii: It is generated by PCS Data Transmission Enabling state diagram as specified in Figure 3-2, and Figure 3-3.

Table 3-1 Relationship of Transmitter Enabling State Variables to Clause 40.3.3.1 in IEEE 802.3-2012

802.3-2012 40.3.3.1	BR-PCS Transmission Enabling State Diagram Variables	Notes
link_status	The same definition.	NC
pcs_reset	The same definition.	NC
TX_EN	Note: The same definition but referencing signal in MII. **DIFF**: change "GMII as specified in 23.2.2.3" to "MII as specified in 22.2.3".	MD
TX_ER	Note: The same definition but referencing signal in MII. **DIFF**: change "GMII as specified in 23.2.2.3" to "MII as specified in 22.2.5".	MD
tx_mode	Note: Same definition.	NC

3.2.2 **4B3B conversion**

3.2.2.1 4B3B conversion for control signals

Signals tx_enable_mii, tx_error_mii and TXD[3:0], synchronized to MII TX_CLK are the input of 4B3B conversion. After 4B3B conversion, the transmit signals tx_data[2:0], tx_enable and tx_error shall be synchronized with PCS transmit clock pcs_txclk. The frequencies of TX_CLK and pcs_txclk are 25 MHz and $33\frac{1}{3}$ MHz respectively to keep the same bitwise throughput with 4B3B conversion. TX_CLK could be from local crystal or oscillator if it is in MASTER mode or from recovered clock if it is in SLAVE mode. The pcs_txclk could be derived from the same clock source as TX_CLK, however, with proper clock division factor to get to the required frequency.

3.2.2.2 4B3B conversion for MII data

The transmit data (TXD[3:0]) at the MII interface shall first be converted into 3 bits as a group (tx_data[2:0]). As shown in Figure 3-3, when the number of bits of a packet is not multiple of three, the function of 4B3B conversion shall append stuff bits to the end of a packet (1 or 2 bits), and correspondingly, tx_enable signal shall stay high till all the bits in a packet (appended with stuff bits if applicable) are rate converted. Those stuff bits could be padded randomly, which is left to implementer, and shall be discarded at the receiver side upon the boundary of the last nibble at MII RX domain. The minimum 12 byte IPG period between packets helps to flush out the extra stuff bits to prevent FIFO overflow.

3.2.3 PCS transmit function

The PCS Transmit function shall conform to the PCS Transmit State Diagram in Figure 3-4, and the associated state variables, functions, timers and messages.

In each symbol period, PCS Transmit generates a sequence of symbols A_n to the PMA, operating in one of three different modes (TXMODE), where symbol A_n is a ternary code that can take values of (-1, 0, 1). The PMA transmits symbol A_n over a wire pair BI_DA. The integer, n, is time index introduced to establish a temporal relationship between different symbol periods. A symbol period, T, is nominally equal to 15ns. In normal mode of operation, between streams of data indicated by the parameter tx_enable, PCS Transmit generates sequences of vectors using the encoding rules defined for the idle mode. Upon assertion of tx_enable, PCS Transmit passes SSD of 6 consecutive symbols to PMA, replacing the first 9 bits of preamble. Following SSD, tx_data[2:0] is encoded using PAM3 technique into a vector of ternary symbols until tx_enable is de-asserted. Following the de-assertion of tx_enable, special code ESD (or ERR_ESD when transmit error is encountered) of 6 consecutive symbols are generated, after which the transmission of idle mode is resumed. As shown in Figure 3-3, if

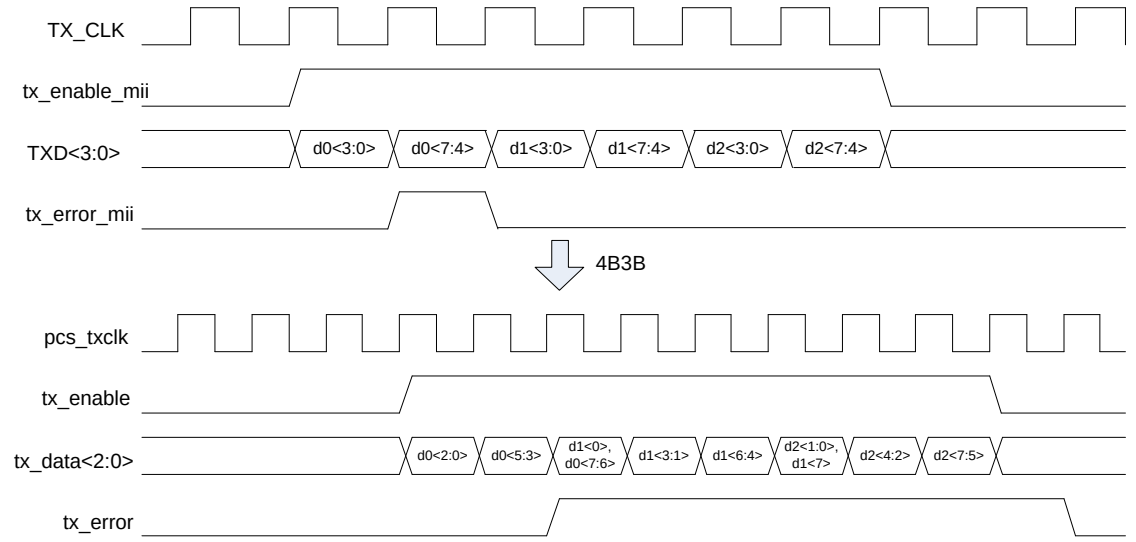
tx_error_mii is ever asserted (due to MII TX_ER assertion) during the data packet period, tx_error is set as TRUE and stays TRUE till the end of packet to record such an occurrence. Unlike 100TX or 1000BT in IEEE 802.3 where symbols shall be exclusively assigned for TX_ER assertion occurrence, BroadR-Reach only has one special symbol pair (0, 0) that is not used by Idle or Data symbols. Therefore, rather than insert ERROR symbols at the place TX_ER is asserted, in BroadR-Reach, at the end of data packet, tx_error is examined to determine whether ESD3 or ERR_ESD3 should be transmitted following two consecutive special pairs (0, 0) for ESD1 and ESD2, as shown in Figure 3-4. When implementing the PCS Transmit State Diagrams shown in Figure 3-4, it should be interpreted similarly to IEEE 802.3. For example, STD is an alias for symb_timer_done, and PUDR stands for PMA_UNITDATA.request(tx_symb_vector), a signal to PMA Transmit indicating tx_symb_vector is available.

If TXMODE has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA.

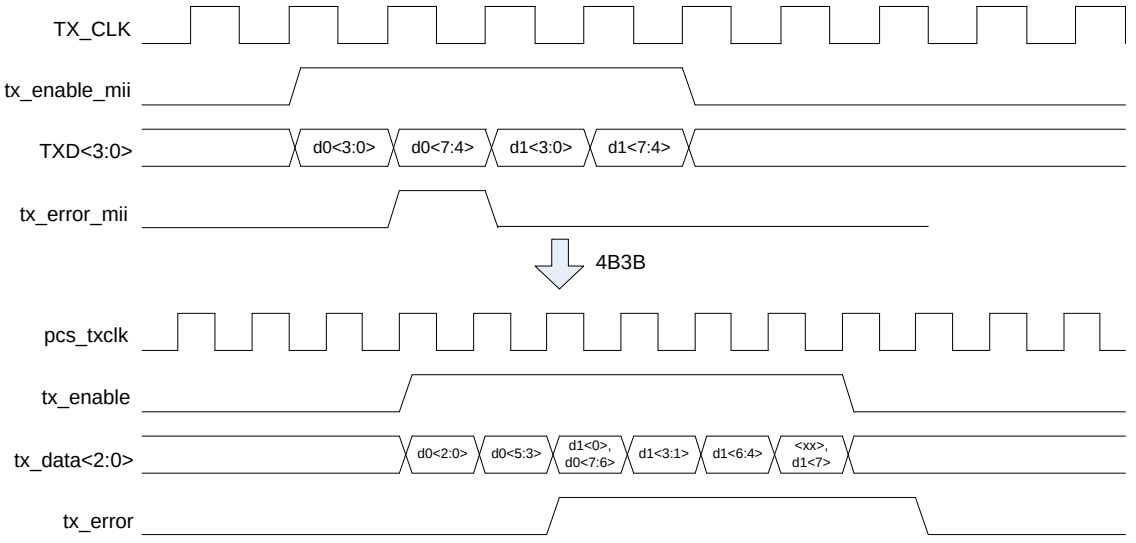
If TXMODE has the value SEND_I, PCS Transmit generates sequences of symbols according to the encoding rule in training mode as described in the following subsections.

If TXMODE has the value SEND_N, PCS Transmit generates symbol A_n, at each symbol period, that are representing data, special control symbols like SSD/ESD or IDLE symbols which are defined in the following subsections. The transition from idle to data is signaled by inserting a SSD, and the end of transmission of data is signaled by an ESD.

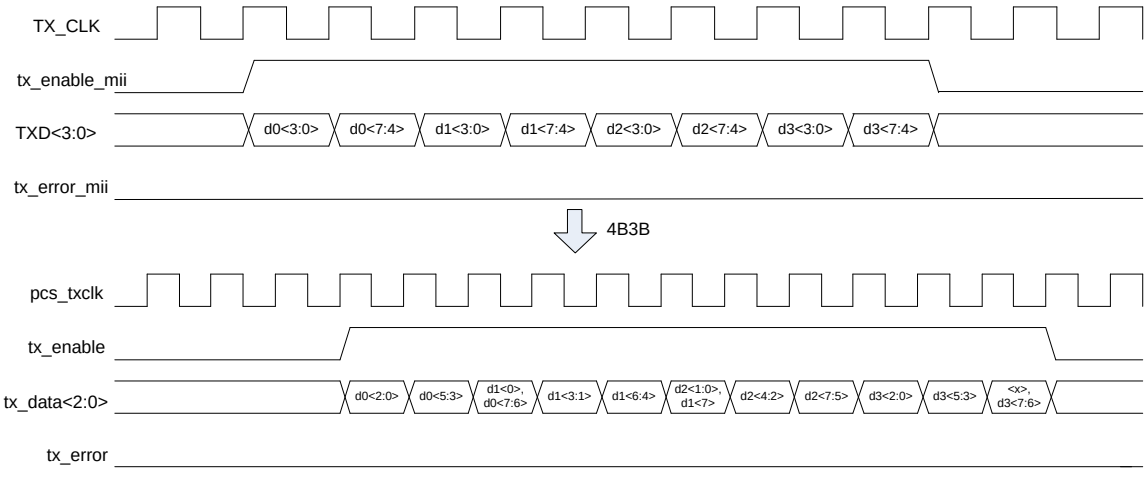
At training or retraining stage when PHY is in SEND_I mode, transmitted symbols are used at receiver side to acquire timing synchronization and open the eye for link up. When link is up, PHY enters SEND_N mode and the transmitted PAM3 symbols are used at receiver PHY for continued clock frequency/phase tracking.



Case 1: 4B3B MII signals conversion (3n-bit data, no stuff bit appended)



Case 2: 4B3B MII signals conversion ((3n+1)-bit data, 2 stuff bits appended)



Case 3: 4B3B MII signals conversion ((3n+2)-bit data, one stuff bit appended)

Figure 3-3: 4B3B MII control signal conversion

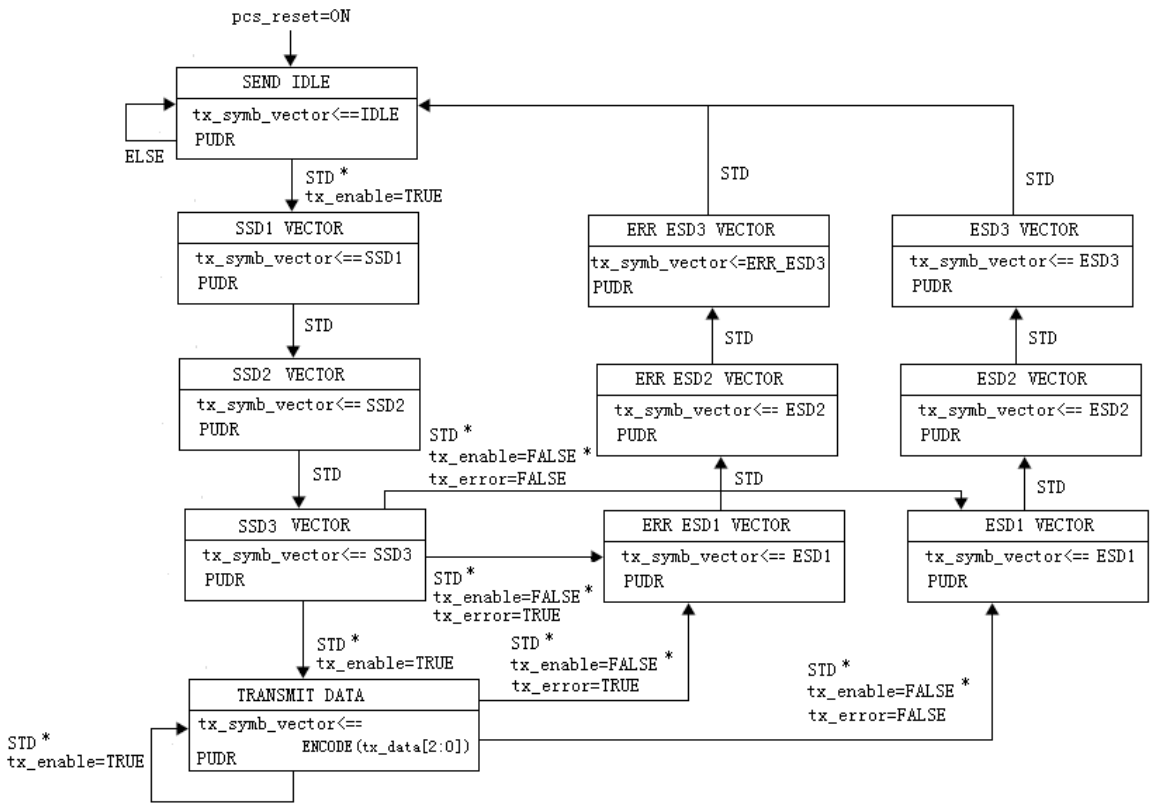


Figure 3-4: PCS Transmit State Diagram to replace IEEE 802.3-2012 Figure 40.10

3.2.3.1 Variables

New variables in this standard

ERR_ESD3: A vector of two ternary symbols in the third code-group of ESD in case of tx_error (-1, -1)

ESD2: A vector of two ternary symbols in the second code-group of ESD (0, 0), as specified in Section 3.2.3.

ESD3: A vector of two ternary symbols in the third code-group of ESD (1, 1), as specified in Section 3.2.3.

SSD3: A vector of two ternary symbols in the third code-group of SSD (0, 0) as specified in Section 3.2.4.5.

tx_data[2:0]: Generated by PCS Transmit, transmit data is synchronous to pcs_txclk ($33\frac{1}{3}$ MHz clock).

Table 3-2 Relationship of Transmitter State Variables to Clause 40.3.3.1 in IEEE 802.3-2012

802.3-2012 Clause 40.3.3.1	BR-PCS Transmitter State Variables	Notes
ESD1	A vector of two ternary symbols in the first code-group of ESD (0, 0). **DIFF**: change "…four quinary symbols…" to "…two ternary symbols…", and "…specified in 4.3.1.3" to "…specified in Section 3.2.3".	LD
pcs_reset	Note: The same definition.	NC
SSD1	A vector of two ternary symbols in the first code-group of SSD (0, 0). **DIFF**: change "…four quinary symbols…" to "…two ternary symbols…", and "…specified in 4.3.1.3.5" to "…specified in Section 3.2.4.5".	LD
SSD2	A vector of two ternary symbols in the second code-group of SSD (0, 0). **DIFF**: change "…four quinary symbols…" to "…two ternary symbols…", and "…specified in 4.3.1.3.5" to "…specified in Section 3.2.4.5.	LD
tx_enable	Note: The same definition, except the reference is to Figure 3-2. **DIFF**: change "…in Figure 40-8" to "…in Figure 3-3".	LD
tx_error	Note: The same definition, except the	LD

	reference is to Figure 3-2. **DIFF**: change "…in Figure 40-8" to "…in Figure 3-3".	
tx_symb_vector	Note: The same definition, except the value this takes on is SYMB_1D. **DIFF**: change "SYMB_4D" to "SYMB_1D".	LD

3.2.3.2 Functions

Table 3-3 Relationship of Transmitter Functions to Clause 40.3.3.2 in IEEE 802.3-2012

802.3-2012 Clause 40.3.3.2	BR-PCS Transmitter State Functions	Notes
ENCODE	The same definition, except this function first converts its argument tx_data[2:0] from 3-bits to 2-D ternary symbols and then, interleaves 2-D ternary symbols to 1-D ternary symbols, tx_symb_vector. **DIFF**: change "GMII TXD <7:0>" to " tx_data[2:0]", and "…rules outlined in 40.2.5.1" to "Section 2.3 Table 2-2 entry for 40.2.5.1".	LD

3.2.3.3 Timer

Table 3-4 Relationship of Timers to Clause 40.3.3.3 in IEEE 802.3-2012

802.3-2012 Clause 40.3.3.3	BR-PCS Transmitter State Messages	Notes
symb_timer	The same definition as in IEEE 802.3. Clause 40.3.3.3, except its duration is	MD

	30ns nominal and it shall be generated synchronously with pcs_txclk. **DIFF**: change “8 ns” to “30 ns”, and change “… in 40.6.1.2.6” to “…in Section 5.1.3”.	

3.2.3.4 Messages

Table 3-5 Relationship of Timers to Clause 40.3.3.4 in IEEE 802.3-2012

802.3-2012 Clause 40.3.3.4	BR-PCS Transmitter State Messages	Notes
PUDR	Note: The same definition.	NC
STD	Note: The same definition.	NC

3.2.4 PCS transmit symbol mapping

The reference diagram of PCS Transmit symbol mapping is indicated in Figure 3-5.

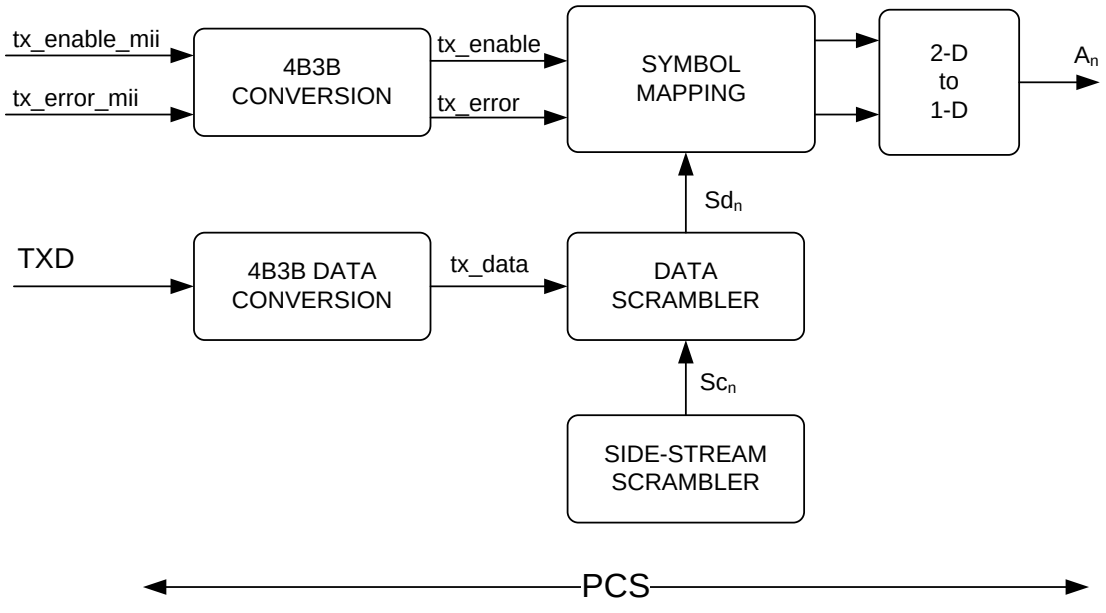


Figure 3-5: PCS Transmit Symbol Mapping

3.2.4.1 Side-stream scrambler polynomial

This scrambler function adopts the Clause 40.3.1.3.1 and associated Figure 40-6 of IEEE 802.3-2012 without any exceptions.

3.2.4.2 Generation of $Sy_n[2:0]$

Generation of $Sy_n[2:0]$ and $Sc_n[2:0]$ adopts the encoding rules, when applicable, from the Clause 40.3.1.3.2 in IEEE 802.3-2012. $Sy_n[2:0]$ vector in this specification is three bits, while the Clause 40.3.1.3.2 vector is four bits. As such, the PCS Transmit encoding of $Sy_n[2:0]$ and then $Sc_n[2:0]$ are performed, at time n, and used to eliminate the correlation of transmit data tx_data[2:0] and to generate idle and training symbols.

From scrambler state $Scr_n[0]$ and polynomial $g(x) = x^3 \wedge x^8$, three bits $Sy_n[2:0]$ shall be generated as defined in 40.3.1.3.2 for $Sy_n[2]$, $Sy_n[1]$, and $Sy_n[0]$. Note that $Sy_n[3]$ is not used by definition.

3.2.4.3 Generation of $Sc_n[2:0]$

The bits $Sc_n[2:1]$ are analogous to Clause 40.3.1.3.3 in IEEE 802.3-2012, but uses different encoding in this specification. bits $Sc_n[2:1]$ shall be generated as follows:

$$Sc_n[2:1] = \begin{cases} [0 \quad 0] & if\ (tx\_mode = SEND\_Z) \\ Sy_n[2:1] & else \end{cases}$$

And the bit $Sc_n[0]$ is defined to be the same as the Clause 40.3.1.3.3 definition.

3.2.4.4 Generation of scrambling bits Sdn[2:0]

The bits $Sd_n[2:0]$ performs analogous function to Clause 40.3.1.3.4 in IEEE 802.3-2012, but uses local definition of tx_data[2:0] specific to this document. The tx_data[2:0] is a three bit vector after 4B3B conversion, and is not analogous to TXD[7:0] used in Clause 40.3.1.4.

From scrambler bits $Sc_n[2:0]$ and tx_data[2:0], bits $Sd_n[2:0]$ shall be generated as follows:

$$Sd_n[2] = \begin{cases} Sc_n[2] \wedge tx\_data_n[2] & if\ (tx\_enable_{n-3} = 1) \\ Sc_n[2] \wedge 1 & else if\ (loc\_rcvr\_status = OK) \\ Sc_n[2] & else \end{cases}$$

$$Sd_n[1:0] = \begin{cases} Sc_n[1:0] \wedge tx\_data_n[1:0] & if\ (tx\_enable_{n-3} = 1) \\ Sc_n[1:0] & else \end{cases}$$

3.2.4.5 Generation of ternary pair (*TA$_n$*, *TB$_n$*)

The bits $Sd_n[2:0]$ performs analogous function to Clause 40.3.1.3.5 in IEEE 802.3-2012, but specific ternary pair is used in this document.

The bits $Sd_n[2:0]$ are used to generate ternary pair (***TA$_n$***, ***TB$_n$***). The ternary symbol (0,0) is used in the special codes of SSD, ESD, and ESD with tx_error. Sequences of (0,0), (0,0), (0,0) represent SSD, (0,0), (0,0), (1,1) represent ESD and (0,0), (0,0), (-1,-1) represent ESD with tx_error.

3.2.4.5.1 Generation of (TAn, TBn) when TXMODE = SEND_I

Among the 9 possible values for the ternary pair (***TA$_n$***, ***TB$_n$***) only 6 values are used in the training sequence as indicated in Table 3-6. The SSD/ESD ternary pairs are not used for training.

Table 3-6:Idle symbol mapping in training

$Sd_{n[2:0]}$	**Ternary A**	**Ternary B**
000	-1	0
001	0	1
010	-1	1
011	0	1

Used for SSD/ESD	0	0
100	1	0
101	0	-1
110	1	-1
111	0	-1

3.2.4.5.2 Generation of (TA_n, TB_n) when TXMODE = SEND_N, tx_enable = 1

The mapping from $Sd_n[2:0]$ to ternary pairs in data mode is indicated in Table 3-7.

Table 3-7 :Data symbols when TXMODE=SEND_N

$Sd_{n[2:0]}$	Ternary A	Ternary B
000	-1	-1
001	-1	0
010	-1	1
011	0	-1
Used for SSD/ESD	**0**	**0**
100	0	1
101	1	-1
110	1	0
111	1	1

3.2.4.5.3 Generation of (TA_n, TB_n) for idle sequence when TXMODE=SEND_N

The extra scrambling bit Sx_n is introduced to balance the power density for ternary pair (TA_n, TB_n). Sxn shall be generated as follows

$$Sx_n = Scr_n[7] \wedge Scr_n[9] \wedge Scr_n[12] \wedge Scr_n[14]$$

The ternary pair (TA_n, TB_n) is generated according to Table 3-8.

Table 3-8: Idle symbols when TXMODE=SEND_N

	tx_mode = SEND_N			
	SX_n = 0		SX_n = 1	
Sdn[2:0]	Ternary A	Ternary B	Ternary A	Ternary B
000	-1	0	-1	0
001	0	1	1	1
010	-1	1	-1	1
011	0	1	1	1
100	1	0	1	0
101	0	-1	-1	-1
110	1	-1	1	-1
111	0	-1	-1	-1

3.2.4.5.4 Generation of (TA_n, TB_n) when TXMODE=SEND_Z

The ternary pair (TA_n, TB_n) simply shows as zero vector (0, 0) when TXMODE=SEND_Z.

3.2.4.6 Generation of symbol sequence

The generation of one-dimensional symbol sequence from ternary pair (***TA_n***, ***TB_n***) is illustrated in the Figure 3-6.

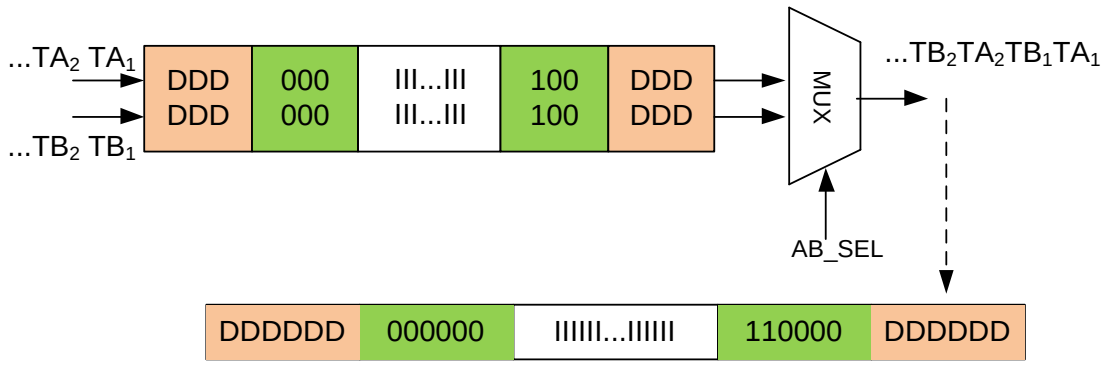


Figure 3-6: 2-D symbol to 1-D symbol conversion

The symbol is sent to one sequence in the form of interleave in the order from right to left. The serial stream is created by interleaving either (***TA$_n$***, ***TB$_n$***) with ***TA$_n$*** followed by ***TB$_n$*** or (***TB$_n$***, ***TA$_n$***) with ***TB$_n$*** followed by ***TA$_n$***. The receiver implementation shall de-interleave the sequence accordingly. The ESD (after one DATA packet) is followed by IDLE symbols, then SSD, and then by DATA. The symbol rate is twice as fast as pcs_txclk.

3.3 *PCS Receive*

3.3.1 **PCS Receive overview**

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 3-7, and associated state variables.

To prevent any miss detection of ESD1 and ESD2 that make PCS Receive state machine locked up in DATA state, a JAB state machine as shown in Figure 3-8 is implemented to make sure the maximum dwelling time in DATA state shall be less than a certain time specified by rcv_max_timer. When rcv_max_timer expires, PCS Receive state machine is reset and transition to IDLE state is forced.

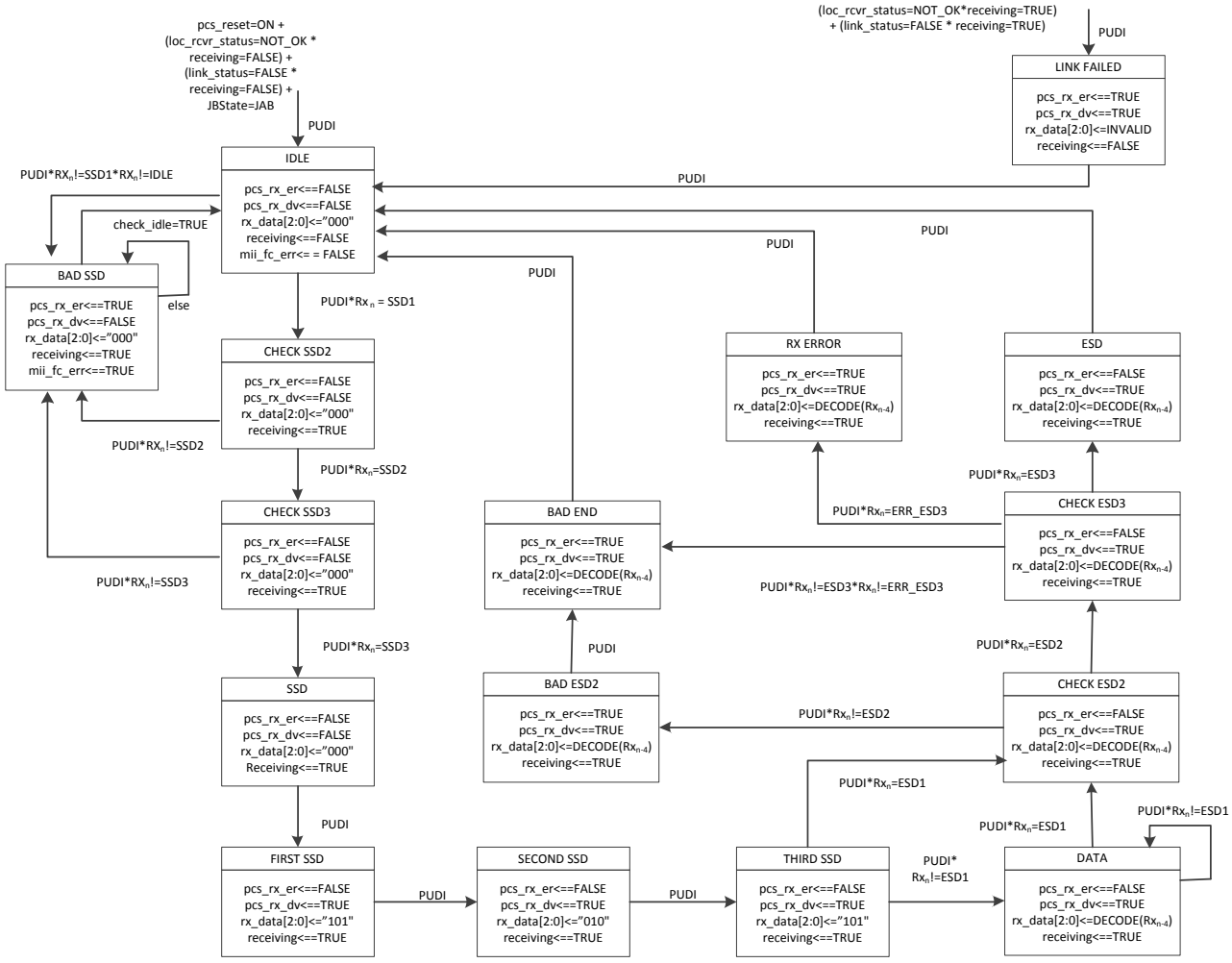


Figure 3-7: **PCS Receive state diagram to replace IEEE 802.3-bit2012 Clause 40 Figure 40.11a**

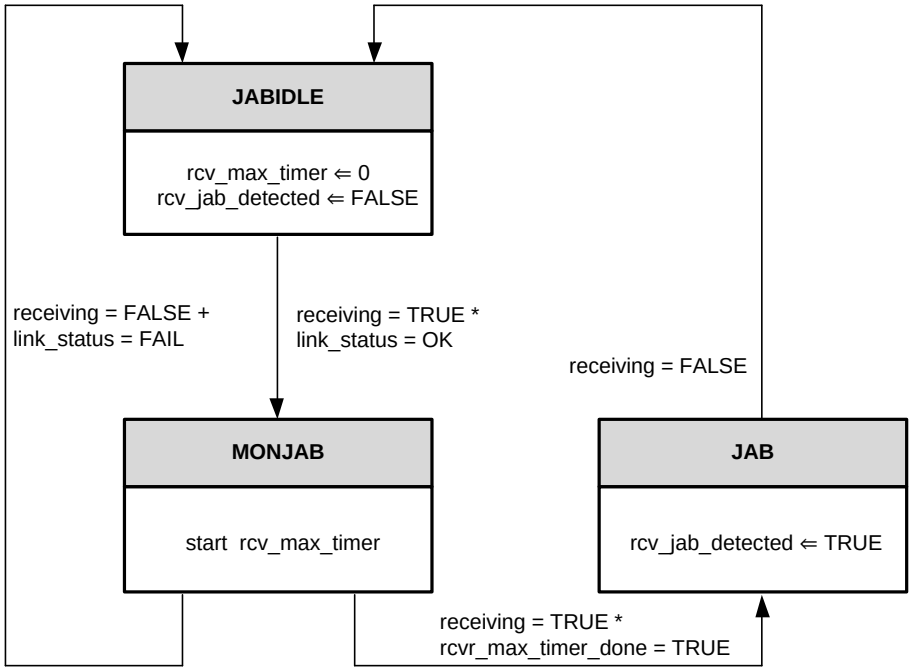


Figure 3-8: JAB state diagram

Note that, in Figure 3-7 the PCS Receive state diagram, there are totally 4 states after SSD3 detection before DATA state; meanwhile, there are also 4 states before IDLE state (including DATA state) that shall do DATA decoding. In this way, the depth of data flush-in delay line is the same as the flush-out delay line depth for proper data packet receiving at MII interface.

The PCS Receive function accepts received symbols provided by PMA Receive function. The received symbols are converted to 2-D ternary pair (***RA$_n$***, ***RB$_n$***) first. To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode. PCS Receive generates the sequence of symbols and indicates the reliable acquisition of the descrambler state by setting the parameter scr_status to OK. The received ternary pairs (***RA$_n$***, ***RB$_n$***) are decoded to generate signals rx_data[2:0], rx_dv, and rx_error, that are processed through 3B4B conversion to generate signals RXD[3:0], RX_DV and RX_ER at the MII interface.

The state variables in Figure 3-7 and Figure 3-8 are defined as below.

3.3.1.1 Variables

New Variables used in this standard

mii_fc_err: Indicates that the line has false carrier error.

receiving: Generated by the PCS Receive function; if set as TRUE, it indicates that the line is in Data phase.

Rxn: most recently received symbol generated by PCS Receive at time n.

pcs_rx_er: PCS receive error indication signal synchronous to pcs_rxclk.

pcs_rx_dv: PCS receive data valid indication signal synchronous to pcs_rxclk.

rx_data[2:0]: PCS decoded data synchronous to pcs_rxclk, nominally $33\frac{1}{3}$ MHz.

JBstate: variable indicating the JAB state status in Figure 3-8.

rcv_jab_detected: parameter set as TRUE when in JAB state as shown in JAB state diagram in Figure 3-8 else it is set FALSE

INVALID: any random three-bit outputs are invalid and disregarded

Table 3-9 Relationship of Receiver State Variables to Clause 40.3.3.1 in IEEE 802.3-2012

802.3-2012 Clause 40.3.3.1	BR-PCS Receiver State Variables	Notes
pcs_reset	Note: The same definition.	NC
loc_rcvr_status	Note: The same definition.	NC
link_status	Note: The same definition.	NC

3.3.1.2 Functions

Table 3-10 Relationship of Functions to Clause 40.3.3.2 in IEEE 802.3-2012

802.3-2012 Clause 40.3.3.2	BR-PCS Receiver State Functions	Notes
check_idle	The same definition, except it operates on next five 2-D ternary symbols after rx_symb_vector is de-interleaved. **DIFF**: Change "..on the current rx_symb_vector.." to "on the current 2-D ternary symbols after de-interleaving rx_symb_vectors.." and change "..next three rx_symb_vectors.." to "..next five 2-D ternary symbols after de-interleaving rx_symb_vectors..".	MD
DECODE	The same definition, except this function first de-interleaves its argument rx_symb_vector from 1-D ternary symbols to 2-D ternary symbols, and then, converts 2-D ternary symbols to, rx_data[2:0]. **DIFF**: change "GMII RXD <7:0> octet" to "rx_data[2:0]", and "…rules outlined in 40.2.5.1" to "Section 2.3 Table 2-2 entry for 40.2.6.1".	LD

3.3.1.3 Timer

New Timer used in this standard

rcv_max_timer: expires after counting 36K (+/- 1.8K) pcs_rxclk clock cycles.

3.3.1.4 Messages

Table 3-11 Relationship of Messages to Clause 40.3.3.4 in IEEE 802.3-2012

802.3-2012 Clause 40.3.3.4	BR-PCS Receiver State Messages	
PUDI	Note: The same definition.	NC

3.3.2 PCS Receive symbol decoding

When PMA Receive indicates normal operations and sets loc_rcvr_status = OK, the PCS Receive function shall check the symbol sequences and search for SSD or receive error indicator.

PCS Receive sets pcs_rx_dv=TRUE when it receives SSD, and sets pcs_rx_dv=FALSE when it receives ESD or ESD with error. The number of bits received in a frame is always a multiple of 3 that shall go through the process of 3B4B conversion, discarding the residual 1 bit or 2 bits of data.

PCS Receive shall set pcs_rx_er = TRUE when it receives bad ESDs, ERR_ESD, or bad SSDs. When the state machine reaches the IDLE state, pcs_rx_er gets reset to FALSE.

3.3.3 PCS Receive descrambler polynomial

This function adopts the Clause 40.3.1.4.2 of IEEE 802.3-2012, with the exception that it applies to rx_data[2:0].

DIFF: Change "…generation of RXD<7:0>…" to "…generation of rx_data[2:0]…".

3.3.4 PCS Receive Automatic Polarity Detection (An Optional Feature)

During training, the automatic polarity detection can be done in PCS Receive as an optional feature with proper decoding procedures. In the IDLE mode, $Sd_n[2:0]$ are generated by side-stream scrambler with

$Sd_n[0]=Scr_n[0]$. According to Table 3-6, when $Sd_n[0]$ is 0, $\boldsymbol{TA_n}$ is either +1 or -1; otherwise, $\boldsymbol{TA_n}$ is 0. Based on this rule, $Scr_n[0]$ shall be decoded solely depending on the value of $\boldsymbol{RA_n}$, then fed back to the shift registers of side-stream descrambler to achieve reliable state acquisition. After that, in every symbol cycle, $Scr_n[0]$ should be compared with the processed $\boldsymbol{RA_n}$ value. Continuous consistency within a certain period means the scrambler has been successfully locked. Polarity can also be automatically detected with similar techniques in a recursive process: one assumption of polarity is made first and the descrambler synchronization is monitored within a certain period to determine whether such an assumption is correct; if not, the same procedure is repeated with a different polarity assumption.

Given the two-step link up process for BroadR-Reach PHYs, a half-duplex step and a full duplex step, polarity detection and correction can be done simultaneously at the earliest stage. Link up starts with the half duplex step when only the MASTER PHY sends symbols to the SLAVE PHY. During this initial stage, all hand-shaking signal status, such as rem_rcvr_status, shall be known as FALSE. With this a priori knowledge, polarity should be accurately detected by the SLAVE side during the half duplex step. If a polarity flip is detected, the SLAVE changes the sign of its received signals ($\boldsymbol{RA_n}$, $\boldsymbol{RB_n}$) to correct the polarity. Furthermore, it also changes the sign of its transmitted signals ($\boldsymbol{TA_n}$, $\boldsymbol{TB_n}$). When the SLAVE PHY starts sending symbols to the MASTER PHY during the full duplex step, since polarity correction has been taken care of by the SLAVE PHY, the polarity would always be observed as correct by the MASTER PHY.

3.3.5 PCS Receive MII signal 3B4B conversion

The MII receive signals RXD[3:0], RX_DV and RX_ER are synchronized with clock RX_CLK of frequency 25 MHz; while PCS Receive generated signals rx_data[2:0], rx_dv, and rx_error shall be synchronized with pcs_rxclk of frequency $33\frac{1}{3}$ MHz to keep the same bitwise throughput after 3B4B conversion. Generation of pcs_rxclk is implementation dependent. RX_CLK could be derived from the same clock source as

TX_CLK if the PHY is in MASTER mode or from the recovered clock if the PHY is in SLAVE mode. The pcs_rxclk could be derived from the same clock source as RX_CLK, however, with proper clock division factor to get to the required frequency.

The conversion from pcs_rxclk domain signals to MII signals are shown in Figure 3-9. If the number of bits from the rx_data stream in pcs_rxclk domain is not a multiple of four, the residual bits are actually the stuff bits appended during 4B3B conversion at the transmitter side. With 3B4B conversion, those bits shall be discarded. RX_DV should be deasserted right after the last nibble is converted.

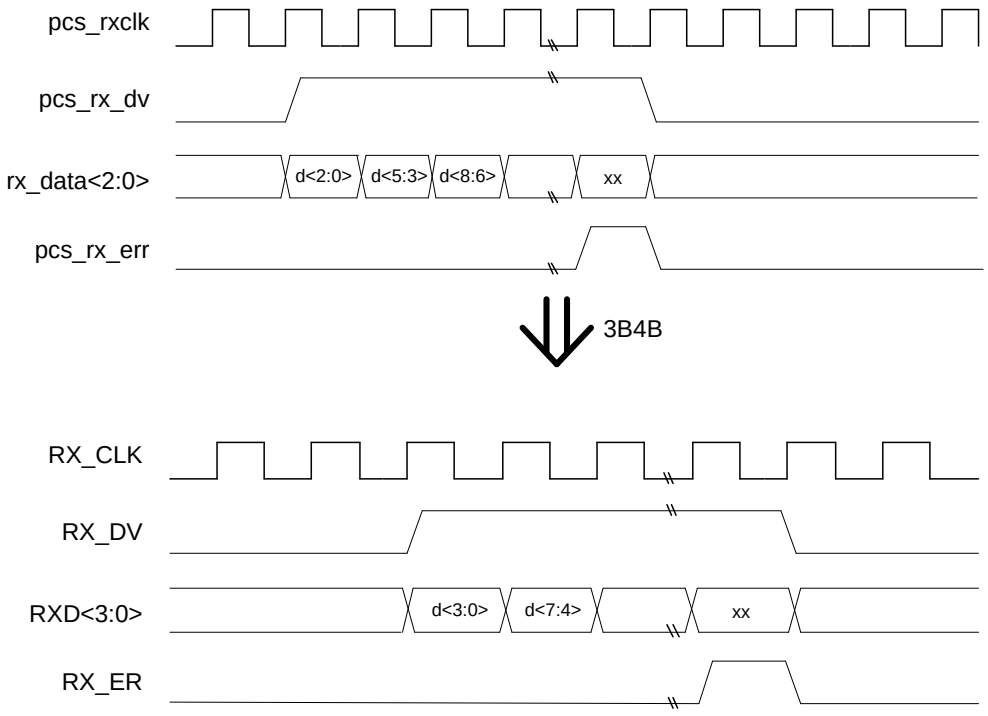


Figure 3-9: PCS Receive 3B4B conversion reference diagram

4.0 Physical Media Attachment (BR-PMA) Sublayer

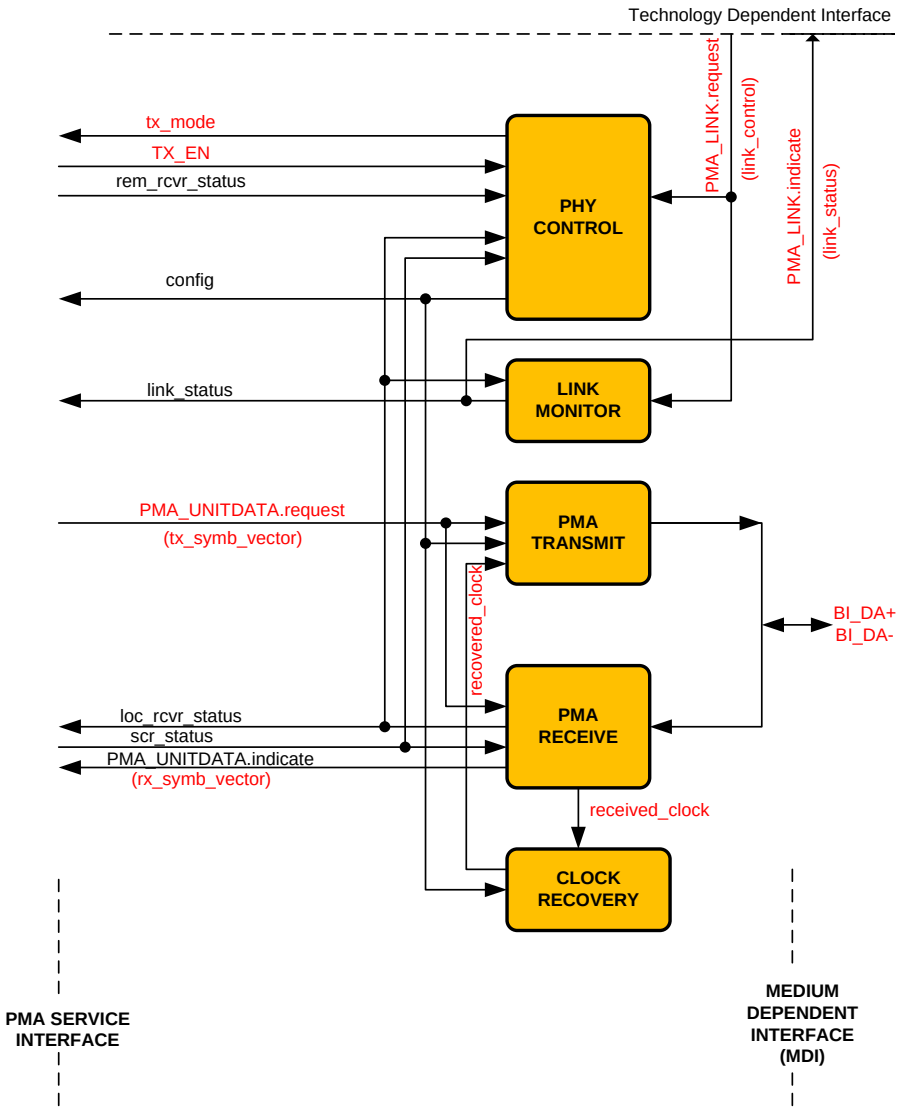
The BR-PMA provides the interface between the PCS and MDI for one pair Automotive BR-PHY. The primary role of BR-PMA is to transmit and receive the incoming data stream coming to and from the MDI via PAM3 which is a voltage dependent signaling between MDI/PMA. This functionality is analogous to Clause 40.4 of IEEE 802.3-2012, 1000BASE-T standard but for a single channel only (versus four channels in 1000BASE-T). The BR-PMA uses 3-level Pulse Amplitude Modulation (PAM3) which outputs 3 discrete differential voltage levels [-1, 0, +1] volts.

There are BR-PMA sublayer functions analogous to IEEE 802.3 Clause 40, and apply to the use of a single channel operation only, and the supports for optional LPI function is not included.

BR-PMA functions are illustrated in Figure 4-1, which notes differences from the PMA diagram in Figure 40-14 of IEEE 802.3-2012 in Clause 40.

4.1 *PMA Reset Function*

This function adopts the Clause 40.3.1.1 of IEEE 802.3-2012 without any exceptions, noting that the Clause 36.2.5.1.3 reference is valid and conditional LPI reference is not used.



NOTE: The recovered_clock shown indicates delivery of the recovered clock back to PMA TRANSMIT for loop timing.

Figure 4-1: BR-PMA Differences from PMA Reference IEEE 802.3-2012 Figure 40-14

4.2 *PMA Transmit Function*

BR-PMA Transmit function is analogous to IEEE 802.3-2012 Clause 40.4.2.2. Figure 4-2 illustrates signal flow of BroadR-Reach PMA Transmit. During the transmission, PMA_UNITDATA.request conveys to

the PMA using tx_symb_vector the value of the symbols to be sent over the single transmit pair.

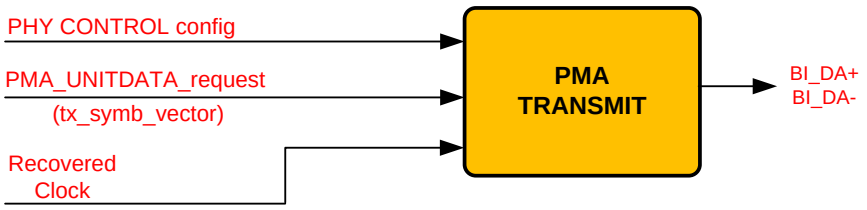


Figure 4-2 PMA Transmit

PHY Control Config will set tx_mode to SEND_N (transmission of normal MII Data Stream, Control Information, or idle), SEND_I (transmission of IDLE code groups), or SEND_Z (transmission of zero code groups). A single transmitter is used to generate the PAM3 signals BI_DA on the wire, using the transmit clock TX_TCLK in $66\frac{2}{3}$ MHz frequency which is the reference clock for the MASTER. When PMA_CONFIG indicates MASTER mode then the PMA Transmit Function will source the TX_TCLK from a local clock source. When PMA_CONFIG indicates SLAVE mode then the PMA Transmit Function will source the TX_TCLK from the recovered clock.

4.3 *PMA Receive Function*

BR-PMA Receive function is similar to IEEE 802.3-2012 Clause 40.4.2. Figure 4-3 illustrates the signal flow of BroadR-Reach PMA Receive. There are 3 primary PMA Receive characteristics: Receivers, Abilities, Sub-Functions.

BroadR-Reach PMA Receive comprises of a single receiver for ternary PAM signals on a single wire, BI_DA. PMA Receiver has the ability to translate the received signals on the single pair into the PMA_UNIDATA.indicate parameter rx_symb_vector. It detects ternary symbol sequences from the signals received at the MDI over one channel and presents these sequences to the PCS Receive function.

PMA Receive has Signal Equalization and Echo Cancellation sub-functions. These sub-functions are used to determine the receiver performance and generate loc_rcvr_status (general status of local receiver). loc_rcvr_status is generated by PMA Receive to indicate the status of the receive link at the local PHY. This primitive conveys to the PCS Transmit, PCS Receive, PMA PHY Control function and Link Monitor the information on whether the status of the overall received link is ok or not. SCR_STATUS is generated by PCS Receive to communicate the status of the descrambler for the local PHY. It conveys the message to the PMA Receive function that the scrambler has achieved synchronization.

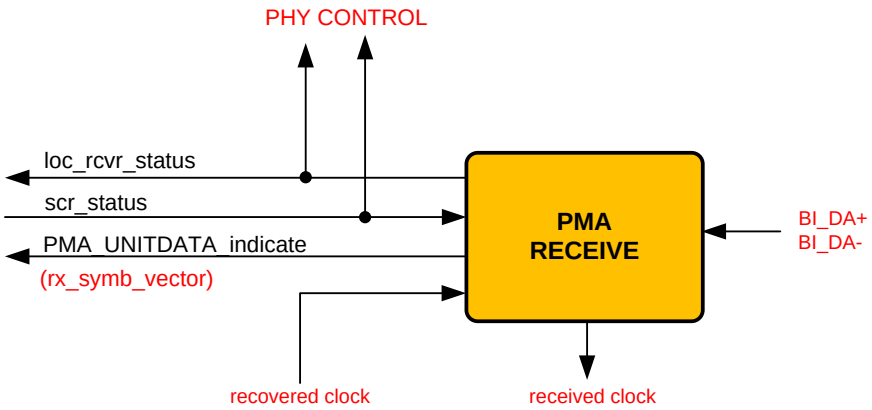


Figure 4-3 PMA Receive

4.4 *PHY Control Function*

BR-PHY Control function is analogous to the IEEE 802.3-2012 Clause 40.4.2.4 but as stated, no auto-negotiation is used. For BR-PHY, FORCE mode is used to achieve link acquisition between two BroadR-Reach link partners. During FORCE mode, PMA_CONFIG is pre-determined to be Master or Slave via management control during initialization or via default hardware set-up. It governs the control actions needed to bring the PHY into the mode of operation when frames are exchanged with the link partner. PMA PHY Control also generates the signals that control PCS and PMA sublayer operations. It determines whether the PHY operates in a normal state, enabling data

transmission over the link segment, or whether the PHY sends special code-groups that represent the idle mode. Figure 4-4 illustrates the differences between BR-PHY control and Figure 40-16a in IEEE 802.3-2012.

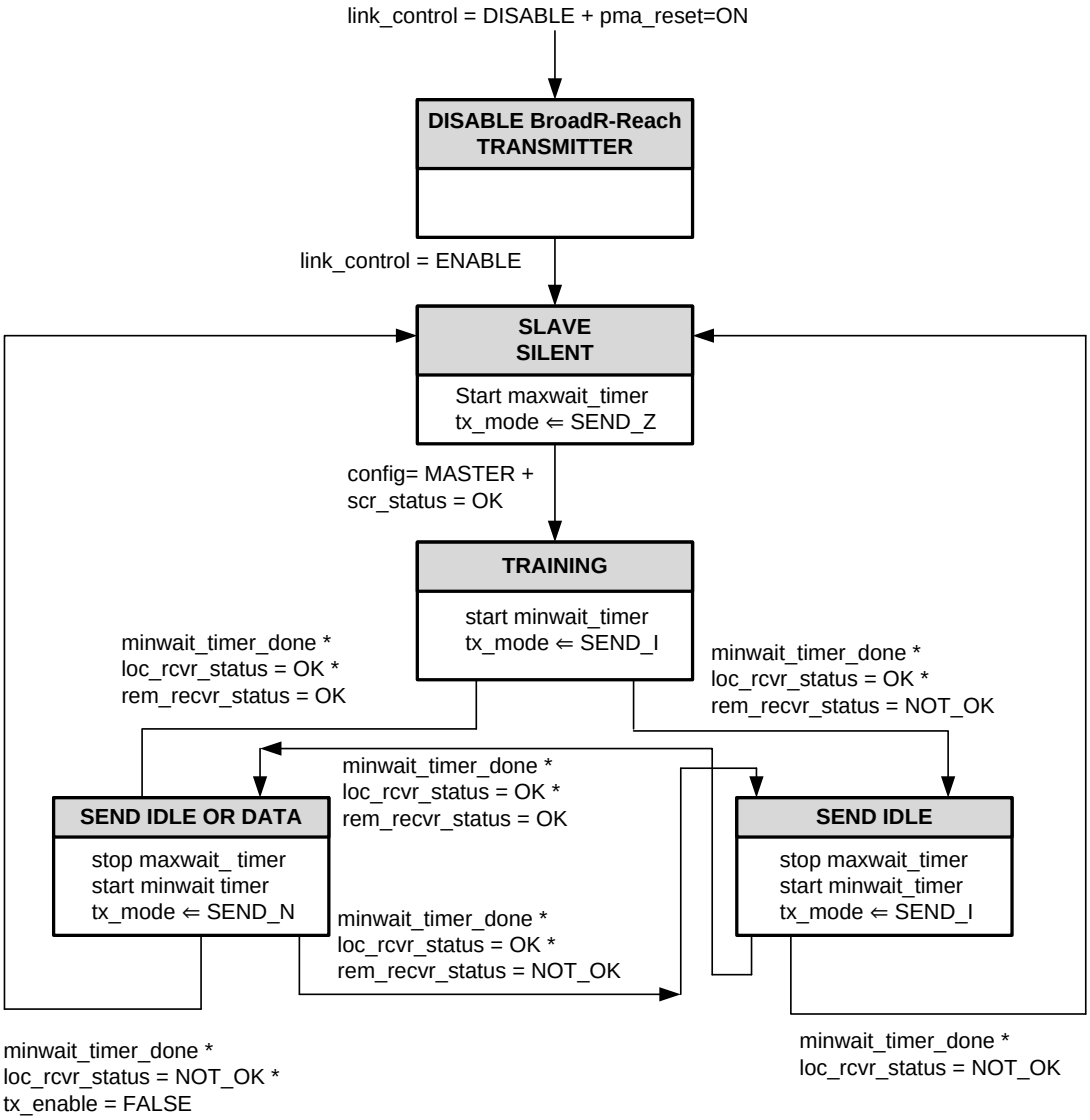


Figure 4-4 PHY Control State Diagram to replace IEEE 802.3-2012 Figure 40-16a

4.5 *Link Monitor Function*

This function adopts the Clause 40.4.2.5 and associated Figure 40-17 of IEEE 802.3-2012 with the exception that Auto-Negotiation is not supported.

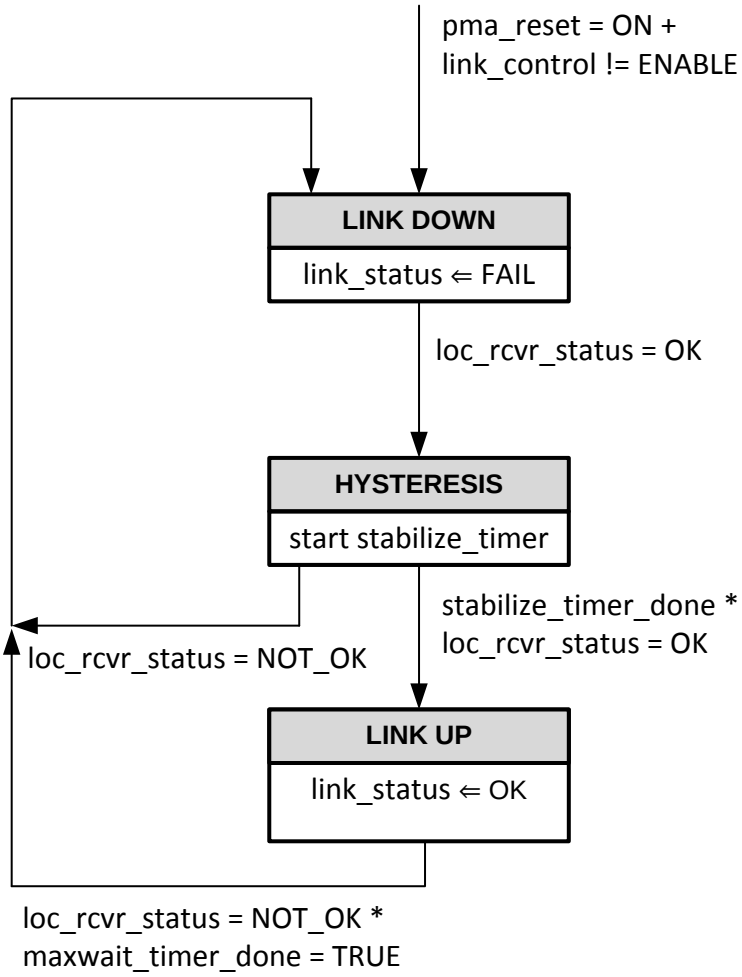


Figure 4-5 Link Monitor State Diagram [Adapted from IEEE 802.3-2012 Clause 40 Figure 40-17]

DIFF: Delete three sentences that begins “Upon power on, …”, through ending “… link_control=ENABLE”.

As such, this function shall comply to Figure 40-17 Link Monitor state diagram in IEEE 802.3-2012, with the exceptions that in NOTE 1, the maxwait_timer reference is to Figure 4-4 (from Figure 40-16a of IEEE 802.3-2012, and NOTE 2 does not apply.

FORCE mode is used to set link_control to ENABLE during the PHY initialization. In FORCE mode, Link Monitor State diagram supports BR-PHY Control operation.

4.6 *PMA Clock Recovery*

This PMA function recovers the clock from the received stream. It is coupled to the receiver in order to provide the clock for optimum sampling of the channel. PMA Clock recovery outputs are also used as input variable for other PMA Functions.

4.7 *State Variables*

4.7.1 State diagram variables

Table 4-1 Relationship of Variables to Clause 40.4.5.1 in IEEE 802.3-2012

802.3-2012 Clause 40.4.5.1	BR-PMA variables	
pma_reset	Note: The same definition.	NC
config	Note: The same definition.	NC
link_control	This variable is configured by management or set by default. Valid values are ENABLE and DISABLE.	LD
link_status	The same definition, except in nested reference from Clause 40.4.5.1 to Clause 28.2.6.1 in IEEE 802.3-2012, the Auto-Negotiation is not used. **DIFF**: change in 28.2.5.1, “PCS, repeater… Auto-Negotiation” to “PCS”.	MD
loc_rcvr_status	Note: The same definition.	NC

pma_reset	Note: The same definition.	NC
rem_rcvr_status	Note: The same definition.	NC
scr_status	Note: The same definition and with a further note that optional EEE capability is not defined.	NC
tx_enable	Note: The same definition except referenced to Figure 3-4. **DIFF**: change “Figure 40-8” to “Figure 3-4”, and delete “as per 40.3.3.1” (circular reference in Std and not necessary).	MD
tx_mode	Note: The same definition except reference to BR-PCS codes groups in 3.2.3. **DIFF**: change “…representing a GMII data stream…” to “…representing an BR-PCS codes groups in 3.2.3…”.	MD

4.7.2 **Timers**

Table 4-2 Relationship of Timers to Clause 40.4.5.2 in IEEE 802.3-2012

802.3-2012 Clause 40.4.5.2	BR-PMA Timers	
maxwait_timer	The same definition except that it shall expire 1406 ms +/- 18ms if config = MASTER or 656 ms +/- 9ms if config = SLAVE. **DIFF**: replace ‘..750 ms +/- 10 ms..” with “..1406 ms +/- 18ms..”, and “..350 ms +/- 5 ms..” with “..656 ms +/-	MD

	9ms..”.	
minwait_timer	The same definition except it shall expire in 1.8us +/- 0.18us. **DIFF**: replace ‘..1 us +/- 0.1 us..’ with “..1.8us +/- 0.18us..”.	MD
stabilize_timer	The same definition except it shall expire in 1.8us +/- 0.18us. **DIFF**: replace ‘..1 us +/- 0.1 us..’ with “..1.8us +/- 0.18us..”.	MD

5.0 PMA Electrical Specifications

This section defines the electrical characteristics of the Physical Media Attachment (PMA) for a BroadR-Reach Ethernet PHY.

5.1 *EMC Requirements*

Systems containing a BroadR-Reach Ethernet PHY shall be able to meet the Electromagnetic Compatibility (EMC) requirements of the automotive applications. In CISPR 25, test methods have been defined to measure the EMC performance of the PHY in terms of RF immunity and RF emission.

5.1.1 **Immunity --- DPI test**

In a real application radiofrequency (RF) common mode (CM) noise at the PHY is the result of electromagnetic interference coupling to the cabling system. Additional differential mode (DM) noise at the PHY is generated from the CM noise by mode conversion of all parts of the cabling system and the MDI. The Direct Power Injection (DPI) test method according to IEC62132-4 shall be used to measure the sensitivity of the DUT's PMA receiver to radiofrequency CM RF noise.

5.1.2 **Emission --- 150Ohm conducted emission test**

The 150Ohm test method according to IEC61967-4 shall be used to measure the emission of the DUT's PMA transmitter to its electrical environment.

5.1.3 **Transmit clock frequency**

The ternary symbol transmission at the MDI shall be $66\frac{2}{3}$ MHz +/- 100 ppm.

5.2 *Test Modes*

These test modes are analogous to Clause 40.6.1.1.2 in IEEE 802.3-2012, and reflect test modes for BR-PHY. The test modes described

below in Table 5-1 are provided to allow for testing of the transmitter waveform, transmitter distortion, transmitted jitter, and transmitter droop.

These test modes shall only change the data symbols provided to the transmitter circuitry and not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal operation. These modes shall be enabled by setting a 3-bit control register.

Table 5-1: BR-PHY management register settings for Test Modes

Register			Mode
0	0	0	Normal operation.
0	0	1	Test mode 1 – Transmit droop test mode
0	1	0	Test mode 2 – Transmit jitter test in MASTER mode
0	1	1	Test mode 3 – Transmit jitter test in SLAVE mode (reserved)
1	0	0	Test mode 4 – Transmitter distortion test
1	0	1	Test mode 5 – Normal operation at full power. This is for the PSD mask
1	1	0	Reserved, operations not defined
1	1	1	Reserved, operations not defined

Table 5-2 The Differences between BR-PHY test modes and Clause 40.6.1.1.2 in IEEE 802.3-2012

802.3-2012 Clause 40.6.1.1.2	BR-PMA Timers	
Test mode 1	Test mode 1 is for testing transmitter droop. When test mode 1 is enabled, the PHY shall transmit N “+1” symbols followed by N “-1” symbols. The value of N should be chosen such that N symbol period is greater than 500 ns. This sequence is repeated continually. For example, a PHY transmitting 40 symbols (600 ns) will be long enough for a 500	LD

	ns droop measurements.	
Test mode 2	The same specification except that data symbol sequence is {+1,-1}, and symbol clock uses $66\frac{2}{3}$ MHz +/- 0.01%. **DIFF**: replace "{+2, -2}" with "{+1, -1}", and "..from a 125.00 MHz +/- 0.01% clock.." with "..from a $66\frac{2}{3}$ MHz +/- 0.01% clock..".	MD
Test mode 3	Test mode 3 is optional, and there is no requirement for transmitter timing jitter in SLAVE test mode 3. However, in section 5.4.3, there is a transmitter Timing jitter requirement for SLAVE devices in normal mode when linked up with a MASTER device. As an optional feature, when the Test mode 3 is enabled, the PHY shall transmit the data sequence {+1,-1} repeatedly on the channel. The transmitter shall time the transmitted symbols from a symbol rate clock in the SLAVE timing mode.	LD
Test mode 4	The same specification except that data symbol interval is 15 ns, transmit symbols are as shown Table 5-3, and clock is $66\frac{2}{3}$ MHz +/- 0.01%. A typical transmitter output for test mode 4 is not shown. **DIFF:** replace "symbol interval (8 ns)" with 'symbol interval (15 ns)", "..symbols from a 125.00 MHz ± 0.01% clock.." with "..symbols from a $66\frac{2}{3}$ MHz ± 0.01% clock..", and delete the sentence "A typical transmitter… shown	MD

	in Figure 40-22.”.	

Table 5-3 Transmitter test mode 4 symbol mapping

$x1_n$	$x0_n$	Transmit PAM3 symbol
0	0	0
0	1	1
1	0	0
1	1	-1

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask. When test mode 5 is enabled, the PHY shall transmit a random sequence of PAM3 symbols, generated by the scrambling function described in Section 3.2.4.

5.3 *Test Fixtures*

The following fixtures, or their equivalents, as shown in Figure 5-1, Figure 5-2, and Figure 5-3, in stated respective tests, shall be used for measuring the transmitter specifications. The tolerance of resistors should comply with IEEE standard 802.3 Clause 40.6. All the transmitter tests are defined at MDI. It may include passive components between PHY and MDI as long as the measurements at MDI for all the defined tests are BR-PHY transmitter specification compliant.

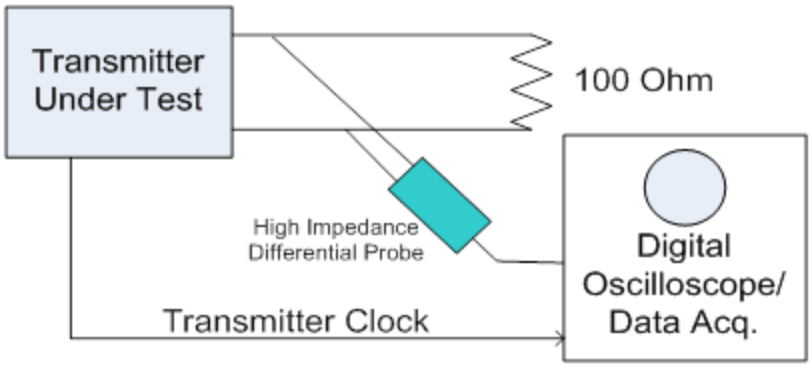


Figure 5-1 Transmitter Test Fixture 1: Droop, Jitter

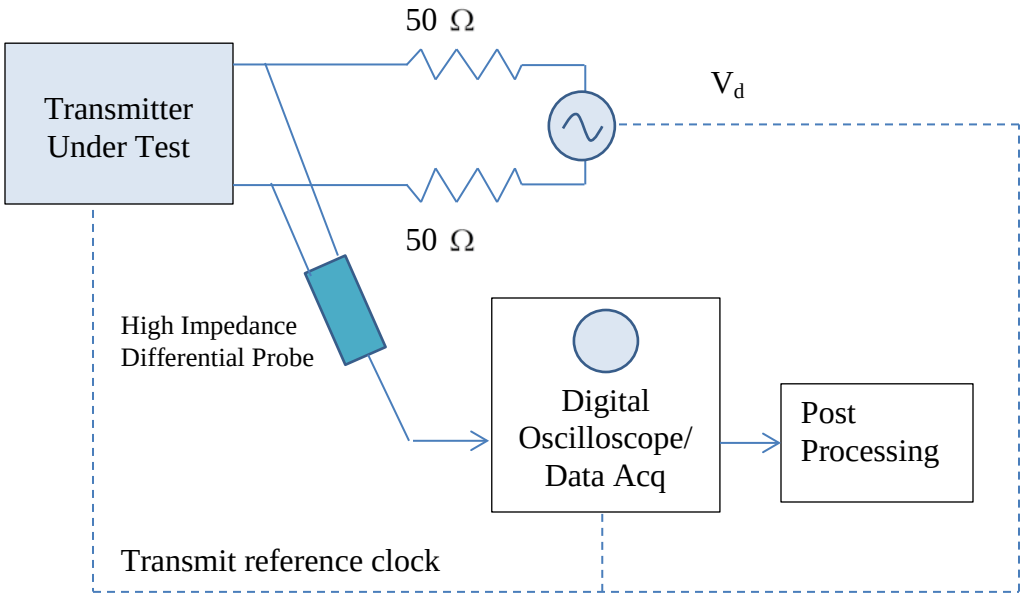


Figure 5-2 Transmitter Test Fixture 2: Distortion

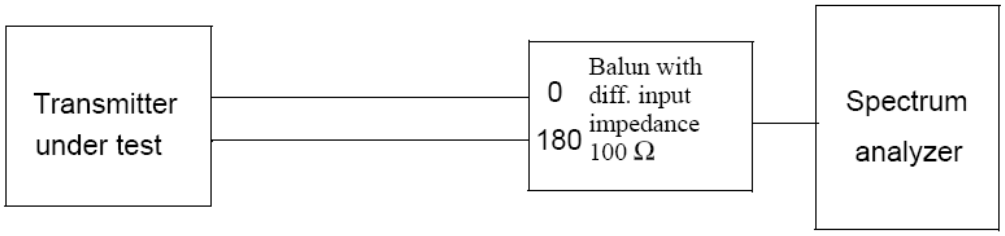


Figure 5-3 Transmitter Test Fixture 3: PSD Mask

To allow for measurement of transmitted jitter in SLAVE modes, the PHY shall provide access to the symbol rate clock, TX_TCLK in $66\frac{2}{3}$ MHz frequency, that times the transmitted symbols. The PHY shall provide a means to enable this clock output if it is not normally enabled.

The disturbing signal V_d, shall have amplitude of 5.4 volts peak-to-peak differential, and frequency given by one-sixth of the symbol rate synchronous with the test pattern.

The generator of the disturbing signal must have sufficient linearity and range so it does not introduce any appreciable distortion when connected to the transmitter output.

5.4 *Transmitter Electrical Specifications*

This specification is analogous to Clause 40.6.1.2. The PMA shall operate with AC coupling to the MDI. Where a load is not specified, the transmitter shall meet the requirements of this section with a 100 Ω (the value can vary within ± 1% range) resistive differential load connected to each transmitter output.

5.4.1 Transmitter Output Droop

The test mode 1 output droop is illustrated in Figure 5-4. With the transmitter in test mode 1 and using the transmitter test fixture 1, the magnitude of both the positive and negative droop measured with respect to an initial peak value after the zero crossing and the value 500 ns after the initial peak, shall be less than 26.9%.

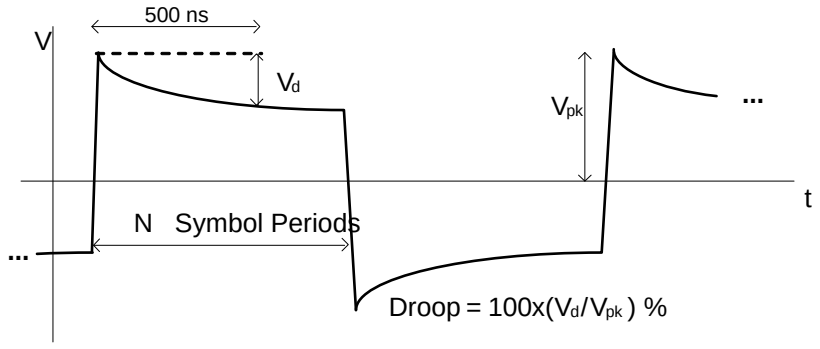


Figure 5-4 Test Mode 1 Output (not to scale)

5.4.2 Transmitter Distortion

This section is analogous to Clause 40.6.1.2.4 in IEEE 802.3-2012. The transmitter distortion is measured by capturing the test mode 4 waveform using transmitter test fixture 2. The peak distortion is determined by sampling the differential signal output with the symbol rate clock at an arbitrary phase and processing a block of consecutive

samples with MATLAB code given below or equivalent. The peak distortion values measured at minimum 10 different equally-spaced phases of a single symbol period should be less than 15 mV.

The MATLAB code removes the disturbing signal from the measured data and computes the peak distortion. The code assumes the disturber signal and the data acquisition clock are frequency locked to the DUT transmit clock.

```
% BroadReach 100 Mb/s single pair Ethernet PHY
% Test mode4: TX Distortion Post Processing
% Assumes frequency lock for PHY, data capturing clock and disturber

clear
Ns=2047; % Scrambler length
Nc=70;  % Canceller length

% Generate scrambler sequence
scr=ones(Ns,1);
for i=12:Ns
  scr(i)=mod(scr(i-11) + scr(i-9),2);
end

% PAM3 assignment
tm4=scr.*(1-2*mod(circshift(scr,1) + circshift(scr,4),2));

% Test mode4 matrix
for i=1:Nc
    X0(i,:)=circshift(tm4,1-i);
end

% Read captured data file
% 200us long, 2GSample/sec, 8bits or more accuracy
fid=fopen('RawData.bin','r');
tx = fread(fid,inf,'int16');
fclose(fid);

% LPF 33 1/3 MHz, not required if data capture accuracy is 10 bits or
more
[A,B]=butter(3,1/30,'low');
tx=filter(A,B,tx);
tx=tx(1:3:end); % decimate to 10x oversampling

% HPF 1.07 MHz
tx = filter([1,-1],[1,-exp(-2*pi/625)],tx);

% Select six periods, 10x oversampling, a row vector
tx=tx((1:6*Ns*10)+2e3)'; % removes HPF transient

% Disturber removal and integration (average) of six periods
TX=fft(tx);
tx=ifft(TX(1:6:end)); % averaged and disturber frequency rejected

% Level normalization
tx=tx/(max(tx)-min(tx))*2;
```

```
% Compute distortion for 10 phases
for n=1:10
tx1=tx(n:10:end);

% Align data and test pattern
temp=xcorr(tx1,tm4);
index=find(abs(temp)==max(abs(temp)));
X=circshift(X0, [0, mod(index(1)+Nc-10,Ns)]);

% Compute coefficients that minimize squared error in cyclic block
coef=tx1/X;

% Linear canceller
err=tx1-coef*X;

% Peak distortion
dist(n) = max(abs(err));
end

% Print results in mV for 10 sampling phases
format bank
peakDistortion_mV = 1000*dist'
```

5.4.3 Transmitter Timing Jitter

When in test mode 2, the RMS (Root Mean Square) value of the MDI output jitter, J_{TXOUT}, relative to an unjittered reference shall be less than 50 ps. No High Pass Filter (HPF) is defined here for jitter measurement. The very low frequency components are expected to be filtered out in the setup via the memory size of the oscilloscope. For example, a digital sampling oscilloscope with 20 GSample/s with a 20 Mbytes sample memory size can only capture down to 1 kHz frequency.

When in the normal mode of operation as the SLAVE, similar to IEEE 802.3 1000BASE-T, jitter on the received signal reflects jitter on the TX_TCLK for SLAVE. Receiving valid signals from a compliant PHY operating as the MASTER with test port connected to the SLAVE, the RMS value of the SLAVE TX_TCLK jitter relative to an unjittered reference shall be less than 0.01 UI (Unit Interval) after the receiver is properly receiving the data. The test setup is shown in Figure 5-5.

For all jitter measurements, the RMS value shall be measured over an interval of not less than 1 ms and unjittered reference is a constant clock frequency extracted from each record of captured periodic wave. It is based on linear regression of frequency and phase that produces minimum Time Interval Error.

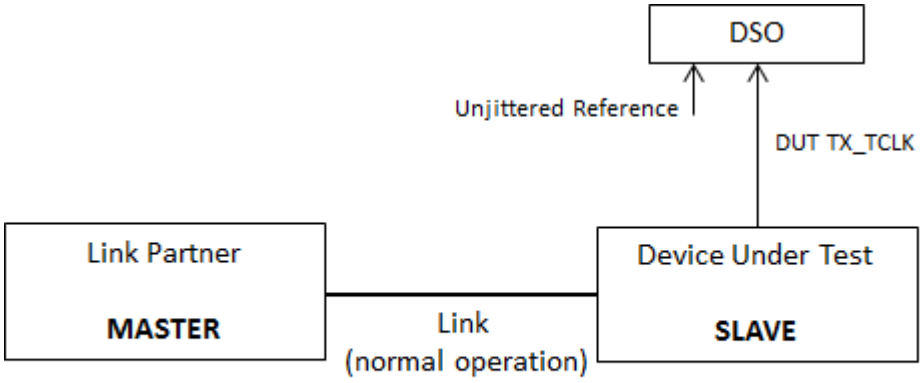


Figure 5-5 Setup for Slave Transmit Timing Jitter in Normal Mode

5.4.4 Transmitter Power Spectral Density (PSD)

When test mode 5 is enabled, the PHY shall transmit a random sequence of ternary codes {-1, 0, +1} which are mapped to 3 discrete differential voltage levels [-1, 0, +1] volts correspondingly. Other than that, the time domain templates for voltage levels and rise/fall times are not defined in this document because a PSD mask is defined which gives the flexibility to do spectral shaping for EMC emissions, if needed. This mask is one of the necessary conditions for transmitter compliance. The time domain templates, however, will not allow the same capability.

In test mode 5, the power spectral density (PSD) of the transmitter, using the test fixture shown in Figure 5.3, shall be between the upper and lower bounds specified in the table below. The upper and lower limits are piece-wise linear masks connecting points given in Table 5-4 (shown in Figure 5-6). A lower PSD mask is provided to ensure the tolerances.

Table 5-4 Power Spectral Density Min & Max Mask Definition

Frequency	PSD Upper Bound (dBm)*	PSD Lower Bound (dBm)*
@ 1 MHz	-23.3	-30.9
@ 20 MHz	-24.8	-35.8
@ 40 MHz	-28.5	-49.2
57 MHz – 200 MHz	-36.5	-

* Settings: RBW=10 kHz, VBW=30 kHz, sweep time>1 min, RMS detector.

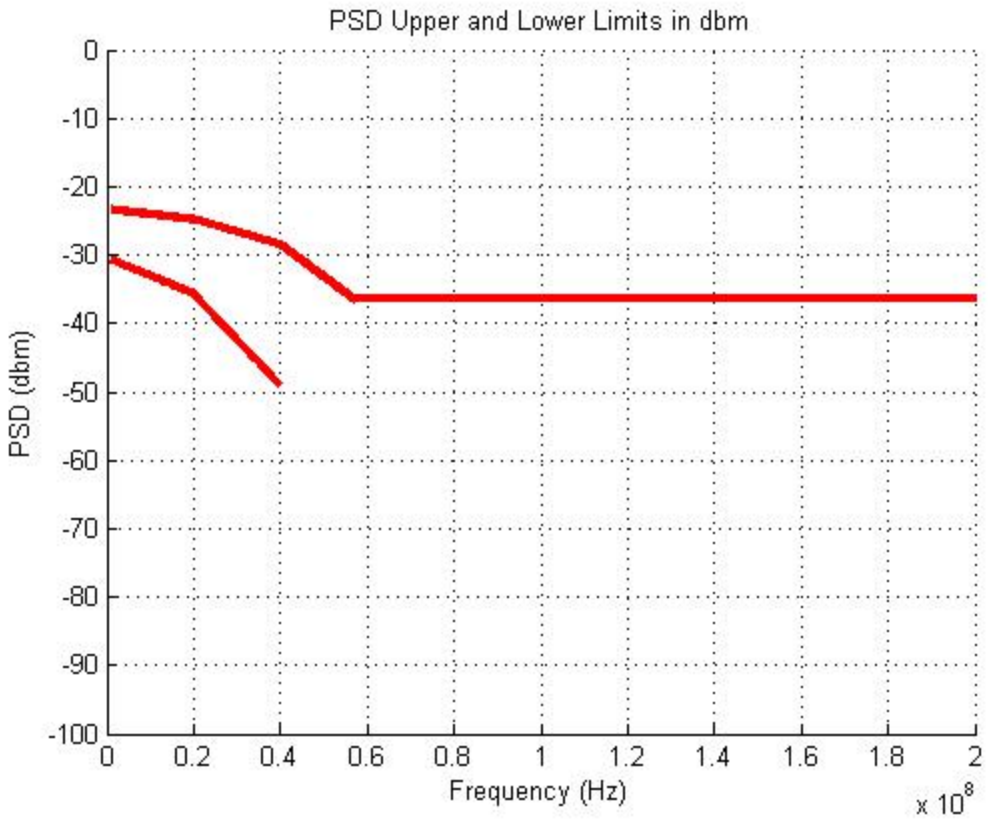


Figure 5-6 PSD Upper and Lower Limits

5.4.5 Transmit Clock Frequency

The symbol transmission rate of the BR-PHY in MASTER mode shall be within the range:

Mode	Frequency
100 Mb/s, 1 pair	$66\frac{2}{3}$ MHz ± 100 ppm

5.5 *Receiver Electrical Specifications*

This specification is analogous to Clause 40.6.1.3 of IEEE 802.3-2012. The BR-PMA shall meet the Receive function specified in Section 4.3 and the electrical specifications of this section. The one pair cabling system used in test configurations shall be within the limits specified in Section 7.0.

5.5.1 Receiver Differential Input Signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of Transmitter Electrical Specifications and have passed through a link specified in Link segment characteristics (1-pair UTP cable), are received with a bit error ratio less than 10^{-10} and sent to the PCS after link reset completion.

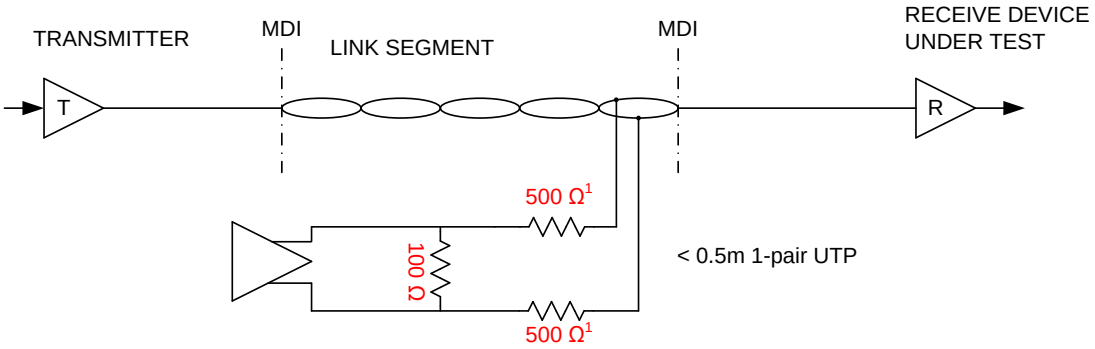
5.5.2 Receiver Frequency Tolerance

The receiver shall properly receive incoming data with a symbol rate within the range:

Mode	Frequency
100 Mb/s, 1 pair	$66\frac{2}{3}$ MHz $\pm$ 100 ppm

5.5.3 Alien Crosstalk Noise Rejection

This specification is provided to verify the DUT's tolerance of alien crosstalk noise. A noise source consisting of a 100 Mb/s BroadR-Reach compliant transmitter sending idle symbols is connected through a resistive network to the test cable. The level of the noise at the MDI is nominally 100 mV peak-to-peak, approximately 26 dB lower than the transmitted signal. The receive DUT is connected to a BroadR-Reach transmitter with the test cable. The BER should be less than 1e-10. The test setup is shown in Figure 5-7.



NOISE SOURCE (BroadR-Reach 100Mbps COMPLIANT TRANSMITTER SENDING IDLES NONSYNCHRONOUS TO THE BroadR-Reach TRANSMITTER UNDER TEST

[1] Resistor matching to 1 part in 1000

Figure 5-7 Alien Crosstalk Noise Rejection Test Setup, analogous to IEEE 802.3-2012 Figure 40-29

6.0 Management Interface

BroadR-Reach makes use of the management functions provided by the MII Management Interface (IEEE 802.3-2012 Clause 22.2.4), and the Automotive specific configuration <PHY-Initialization> which is described in the following section.

6.1 *MASTER-SLAVE configuration resolution*

All BroadR-Reach PHYs will default to configure as SLAVE upon power up or reset until a management system (for example, processor/micro controller) configures it to be MASTER.

MASTER-SLAVE assignment for each link configuration is necessary for establishing the timing control of each PHY.

6.2 *PHY-Initialization*

Both PHYs sharing a link segment are capable of being MASTER or SLAVE. In IEEE 802.3-2012, MASTER-SLAVE resolution is attained during the Auto-Negotiation process (see IEEE 802.3-2012 Clause 28). However, the latency for this process is not acceptable for automotive application. A forced assignment scheme is employed depending on the physical deployment of the PHY within the car. This process is conducted at the power-up or reset condition. The station management system manually configures the BroadR-Reach PHY to be MASTER (before the link acquisition process starts) while the link partner defaults to SLAVE (un-managed).

6.3 *MDC (management data clock)*

MDC is specified in IEEE 802.3-2012 Clause 22.2.2.11.

6.4 *MDIO (management data input/output)*

MDIO is specified in IEEE 802.3-2012 Clause 22.2.2.12.

7.0 Link segment characteristics

BR-PHY is designed to operate over one-pair balanced cabling system. The one pair UTP cable supports an effective data rate of 100 Mb/s in each direction simultaneously. The link segment for a BroadR-Reach PHY system is defined as in Figure 7-1 which comprises one pair 15m UTP balanced copper cabling, two inline connectors and two end connectors.

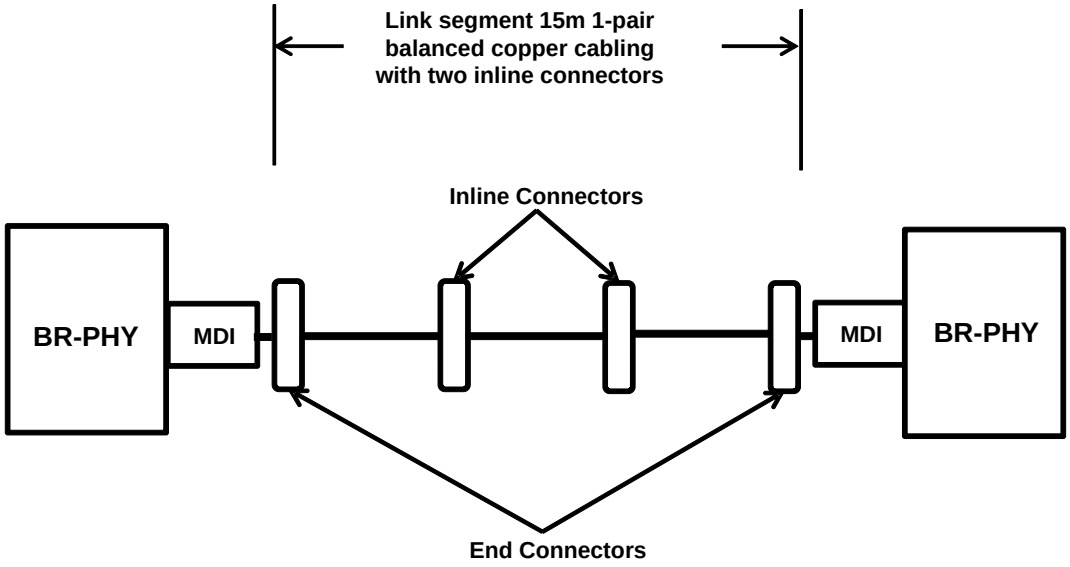


Figure 7-1 Link Segment Definition

7.1 *Cabling system characteristics*

The cabling system used in Figure 7-1 to support BR-PHY requires one pair of balanced cabling with impedance in the range of [90Ω - 110Ω] (nominal 100 Ω) to support 100 Mb/s in each direction simultaneously. The cabling system components used in Figure 7-1 comprise 1-pair UTP cables up to 15m length.

The transmission parameters contained in this specification ensure that a 1-pair UTP cable link segment will provide a reliable medium.

The transmission parameters of the link segment include insertion loss, return loss and characteristic impedance.

7.1.1 Characteristic Impedance

The characteristic impedance of the cable should be 100 Ω +/-10% measured with TDR and rise-time set not slower than 700 psec.

7.1.2 Insertion Loss

The insertion loss of the channel (one pair 15 meter UTP link segment as shown in Figure 7-1) shall be less than:

Insertion_Loss(f) :	< 1.0 dB	at f = 1 MHz
	< 2.6 dB	at f = 10 MHz
	< 4.9 dB	at f = 33 MHz
	< 7.2 dB	at f = 66 MHz

This insertion loss includes the attenuation of the balanced 1-pair UTP cabling pair, equipment cables and connector losses. The insertion loss for the path from PHY to MDI connector, including choke or any extra low-pass filters, might be separately specified from cabling system.

7.1.3 Return Loss

The return loss shall of the link segment in Figure 7-1 shall meet or exceed the following equation for all frequencies from 1 MHz to 66 MHz (with 100 Ω reference impedance):

Return Loss (f) :	18 (dB)	for f = 1 - 20 MHz
	18 – 10*log10(f/20) (dB)	for f = 20 - 66 MHz

7.1.4 **Mode Conversion**

The common mode to differential mode conversion of the link segment in Figure 7-1 shall meet or exceed the following equation for all frequencies from 1 MHz to 200 MHz:

Mode Conversion(f) : 46 (dB) for f = 1 - 66 MHz

46 – 10*log10(f/66) (dB) for f = 66 - 200 MHz

7.2 ***Noise Environment***

In the BroadR-Reach automotive environment, there are several types of noise sources.

a) Echo from the local transmitter on the same cable pair, is caused by the hybrid function for bidirectional data transmission in the BroadR-Reach duplex channel and by the impedance discontinuities in the link segment. Echo cancellation techniques, up to each PHY implementer, shall be used to achieve the objective BER level.
b) The typical background noise is mainly due to thermal noise. Thermal noise, with level roughly at -140 dBm/Hz, is not a critical contributor that would impact performance. BroadR-Reach signaling allows a robust margin over a 15m UTP channel to combat thermal noise.
c) There is no FEXT or NEXT as BroadR-Reach is a one pair solution. When multiple cable pairs are bundled, the alien XTALK (NEXT/FEXT) become interference sources. Since the transmitted symbols from the alien noise source in one cable are not available to another cable, cancellation cannot be done. When there are multiple pairs of UTP cables bundled together, where all pairs carry 100 Mb/s links, then each duplex link is disturbed by neighboring links, degrading the signal quality on the victim pair. In order to limit the near end crosstalk noise for a 6-pair bundle UTP cable, the power sum NEXT loss shall be:

Power Sum NEXT LOSS (dB) > 31.5 – 10*log10 (f/100)

Moreover, the Power Sum Equal Level Far End Crosstalk (ELFEXT) for a 6-pair bundle UTP cable shall be:

Power Sum ELFEXT (dB) > 16.5 – 20*log10 (f/100)

where f is the frequency over 1 MHz - 100 MHz range.

8.0 MDI Specification

This section defines the MDI for BroadR-Reach Automotive application.

8.1 *MDI Connectors*

The mechanical interface to the balanced cabling could be a 2-pin connector or a multi-pin connector. These connectors shall not degrade the signals, in terms of the insertion loss or return loss, worse than a 15 meter 1-pair UTP cable.

8.2 *MDI electrical specification*

The MDI connector mated with a specified one pair UTP cable connector shall meet the electrical requirements specified in 7.1.

8.2.1 MDI Characteristic Impedance

Characteristic impedance of any mated in-line connectors shall be 100 Ω +/-10% measured with TDR and rise-time set not slower than 700 psec.

8.2.2 MDI Return Loss

The MDI return loss shall meet or exceed the following equation for all frequencies from 1 MHz to 66 MHz (with 100 Ω reference impedance) at all times when the PHY is transmitting data or control symbols.

Return Loss (f) : 20 (dB) for f = 1 - 30 MHz

26 - 0.2*f (dB) for f = 30 - 66 MHz

9.0 Delay constraints

This delay constraint specification is analogous to Clause 40.11 of IEEE 802.3-2012. Every BroadR-Reach PHY associated with MII shall comply with the bit delay constraints for full duplex operation. The delay for the transmit path, from the MII input to the twisted pair, shall be less than 240 ns. The delay for the receive path, from the twisted pair to the MII output, shall be less than 780 ns.

Annex 1A (Informative) MII Registers and Software Requirements

BroadR-Reach PHYs provide full access to IEEE defined registers set [Media Independent Interface] (compliant with Clause 22 of IEEE standard 802.3) through MDIO (Management Data Input/Output) interface. MDIO functions to transfer control and status information between PHY and STA (Station Management) entities synchronously. The bidirectional MDIO signal is synchronous with MDC (Management Data Clock). In addition to IEEE registers set, other PHY registers are also accessible through MDIO interface. These registers are utilized for control and monitor purposes. Typical standard Ethernet PHYs mostly operate in unmanaged systems. So, PHY control settings are not anticipated to be changing after power-up conditions.

Annex 1B (Informative) System Level Test Modes

BroadR-Reach PHY supports two loopback test modes to assist MAC to test PHY functionality without having the need to have link partner. These test modes are as the following:

(a) Internal Loopback Function

(b) External Loopback Function

1B.1 Internal Loopback Function

The internal loopback data flow (may also be called loopback at PCS Receive/transmit) is illustrated in Figure 1B-0-1. When the PHY is in the internal loopback test mode, instead of getting symbols from the PMA Receive function, the PCS Receive function gets PAM3 symbols directly from the PCS Transmit function.

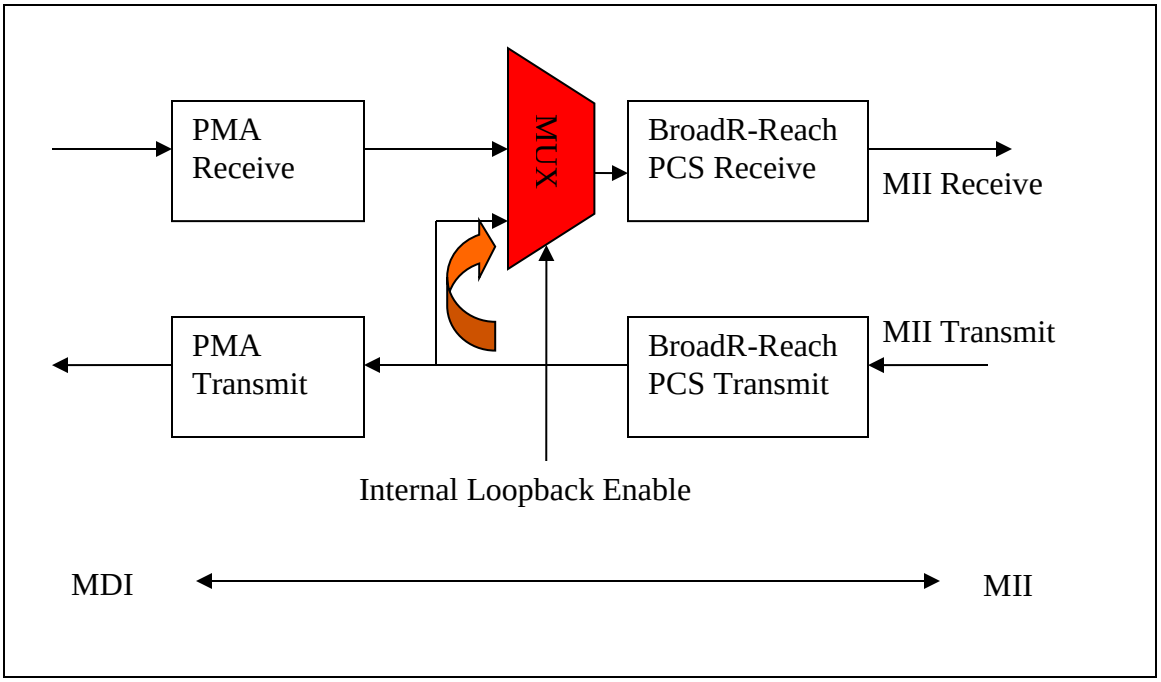


Figure 1B-0-1: Internal Loopback

The MAC compares the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the functionality of BroadR-Reach PCS functions.

1B.2 External Loopback Function

When the PHY is in the external loopback test mode (may also be called loopback at PMA Receive/transmit), the PMA Receive function utilizes the echo signals from the un-terminated MDI and decodes these signals to pass the data back to the MII Receive interface. The data flow of the external loopback is shown in Figure 1B-0-2.

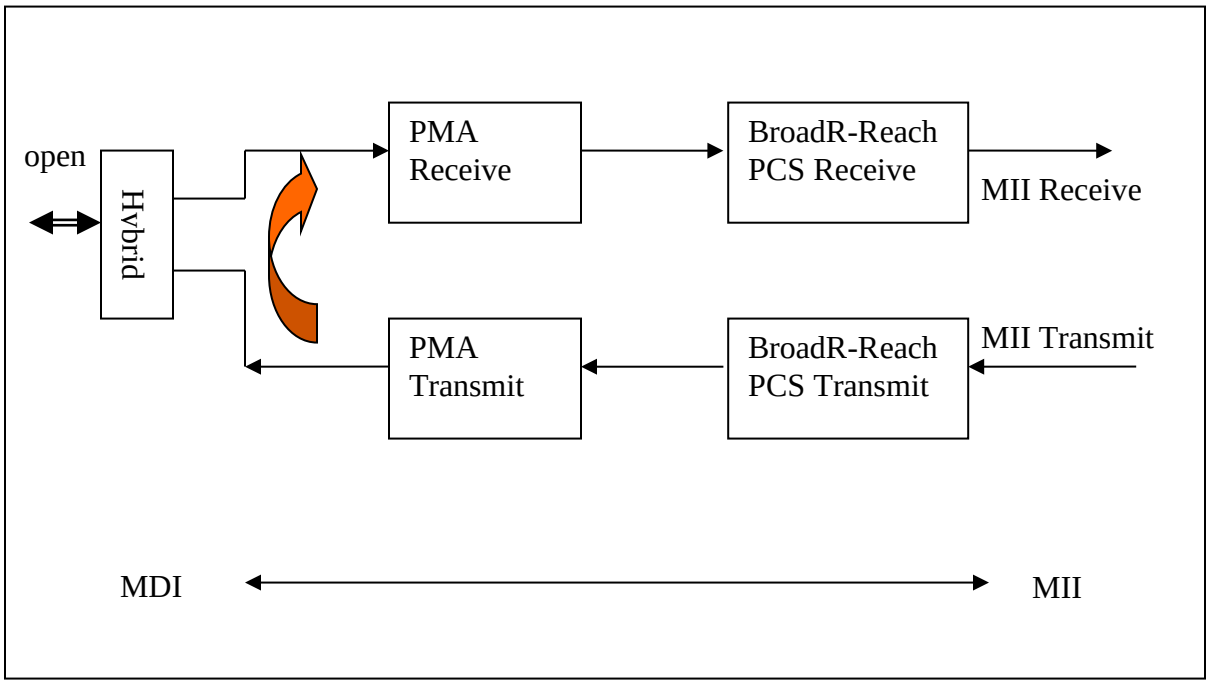


Figure 1B-0-2: External Loopback Function

The MAC compares the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the functionality of the BroadR-Reach PCS and PMA functions.

Normative References

[1] IEEE Standard 802.3-2012: IEEE Standard for Ethernet.

