Auto-Negotiation – What is it and how it fits into 1TPCE

IEEE 1TPCE – Study Group Meeting - May 2014

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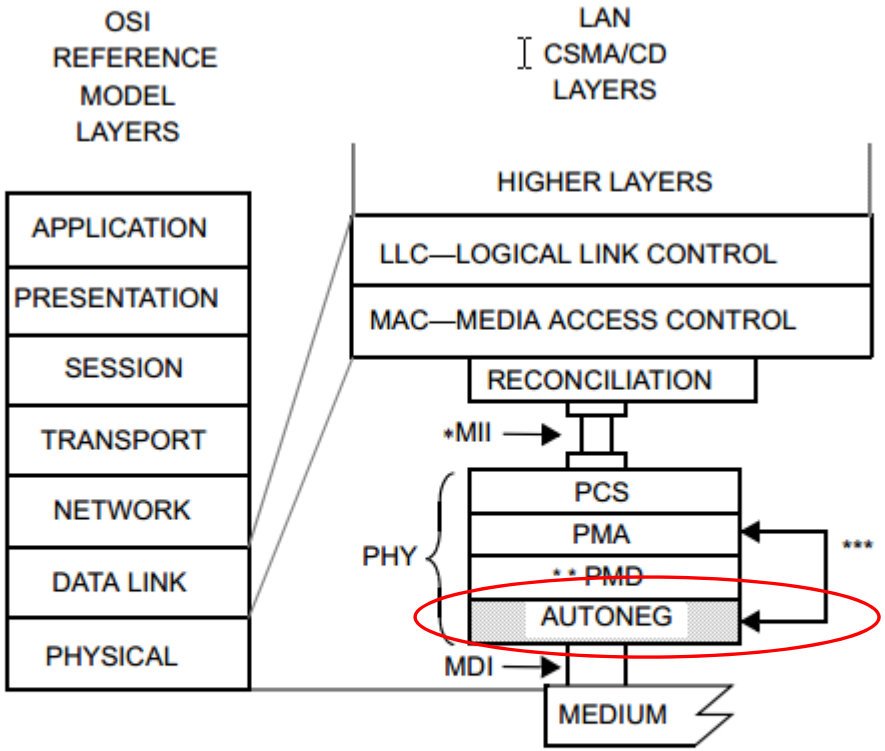
Agenda

- Describe what Auto-Negotiation does
- High level discussion of how it works
- How it fits with 1TPCE

Auto-Negotiation – What is it good for?

- **Exchange management information between 2 connected PHYs**
  - **Done before PHY commits to starting up in an operational mode**
    - **Speed: 10BASE-T, 100BASE-TX, 1000BASE-T, 10GBASE-T, etc**
    - **Master/Slave**
    - **Pause: Synchronous, Asynchronous**
    - **Duplex: Full , Half**
    - **EEE Capability**
    - **Custom exchanges**
- **Allows 2 PHYs to operate at the highest shared operational mode without user intervention (plug and play)**
- **Allows 2 PHYs to establish common start time prior to link training**
  - **Standard mechanism to timeout if link training takes too long**

Where in the ISO Stack?

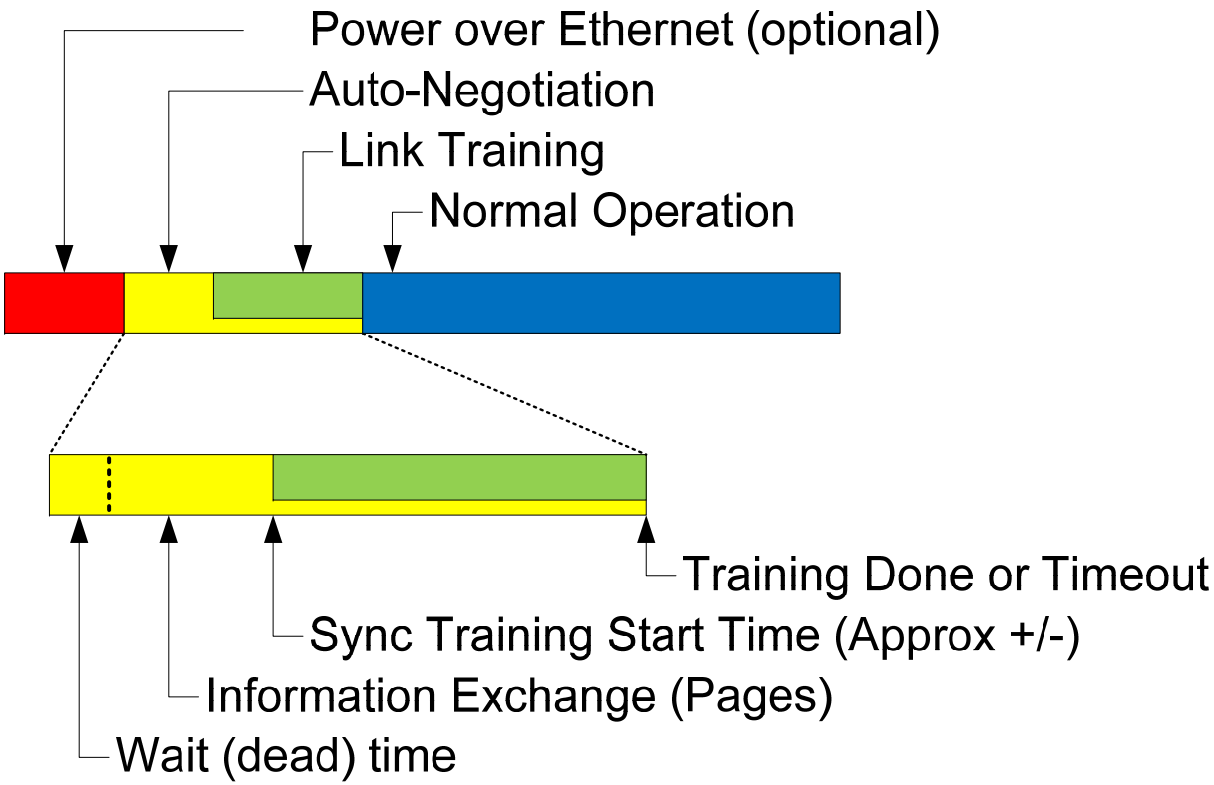


MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
AUTONEG = AUTO-NEGOTIATION

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

When is it used?

Before Link Training



Where is it defined?

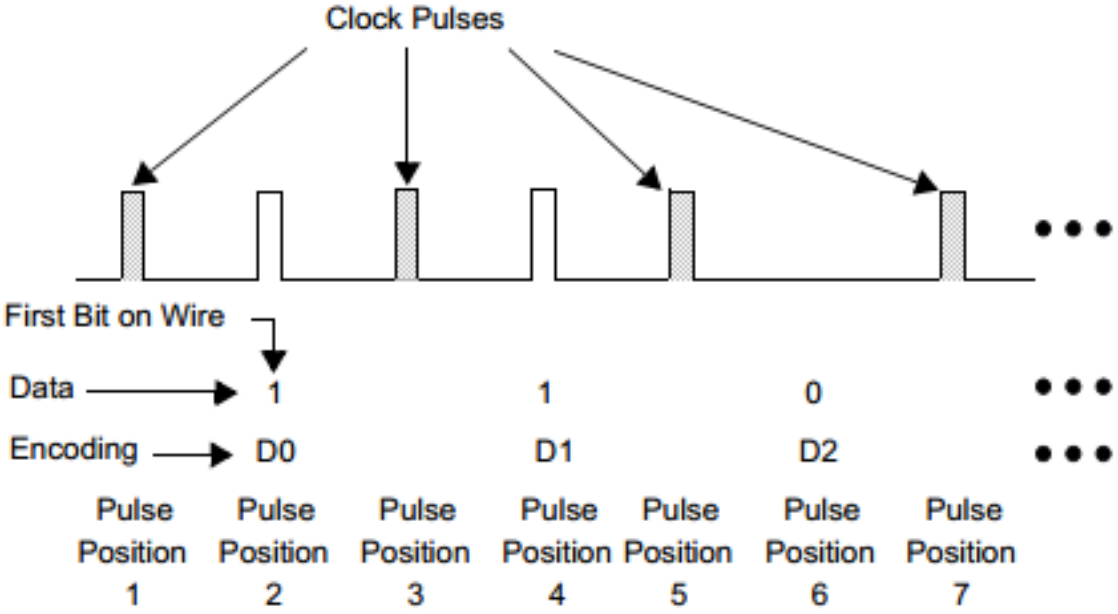
- **Clause 28 – Two twisted pairs**
  - 10BASE-T, 100BASE-TX, 100BASE-T2, 100BASE-T4, 1000BASE-T, 10GBASE-T
- **Clause 73 – Backplane – Two unidirectional lanes**
  - 1000BASE-KX, 10GBASE-KX4, 10GBASE-KR, 40GBASE-KR4, 40GBASE-CR4, 100GBASE-CR10
- **Clause 37 – 1000BASE-X – Two unidirectional lanes**
  - Raw link needs to be up before info exchange
- **All 3 share similar state machines, but are not interoperable.**
  - Electrically Incompatible
  - Different media
  - Different signaling
  - Different bit rates

How is the information exchanged?

- **Pages are exchanged following the movement of the Arbitration State Machine**
  - **Arbitration state machine similar though not exactly the same for Clause 28, 73, and 37.**
- **Pages are group of bits**
  - **Either 16 bits or 48 bits – varies with Clause 28, 73, or 37**
- **Clause 28 and 73 page bits can be recovered with oversampling.**
  - **No DSP training needed**

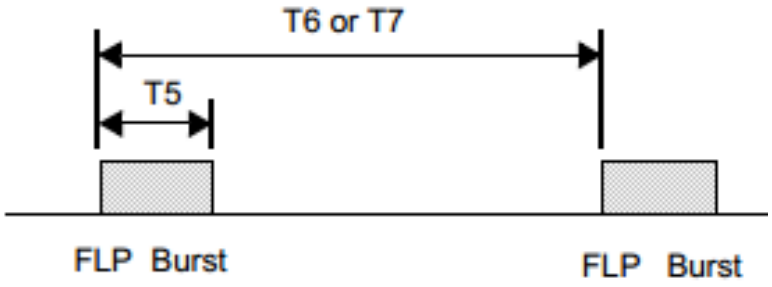
What do the pages look like? Clause 28

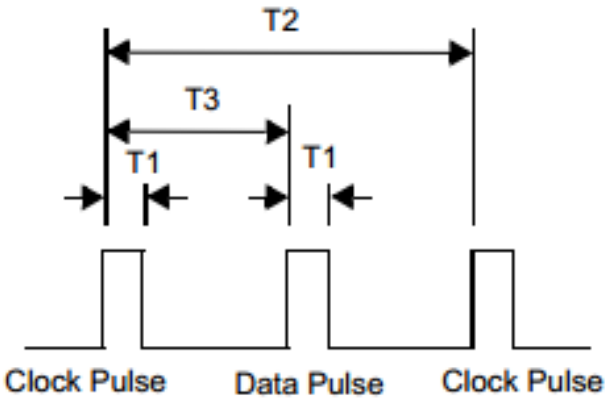
- Based on legacy 10BASE-T link pulses
- Normal Pages - 17 clock pulses and up to 16 data pulses
- Extended Pages – 49 clock pulses and 48 data pulses
- Clock and data pulse slots alternate
- Data pulse present = 1, no data pulse = 0



Pulse Spacing - Clause 28

- **FLP Burst = 1 page**

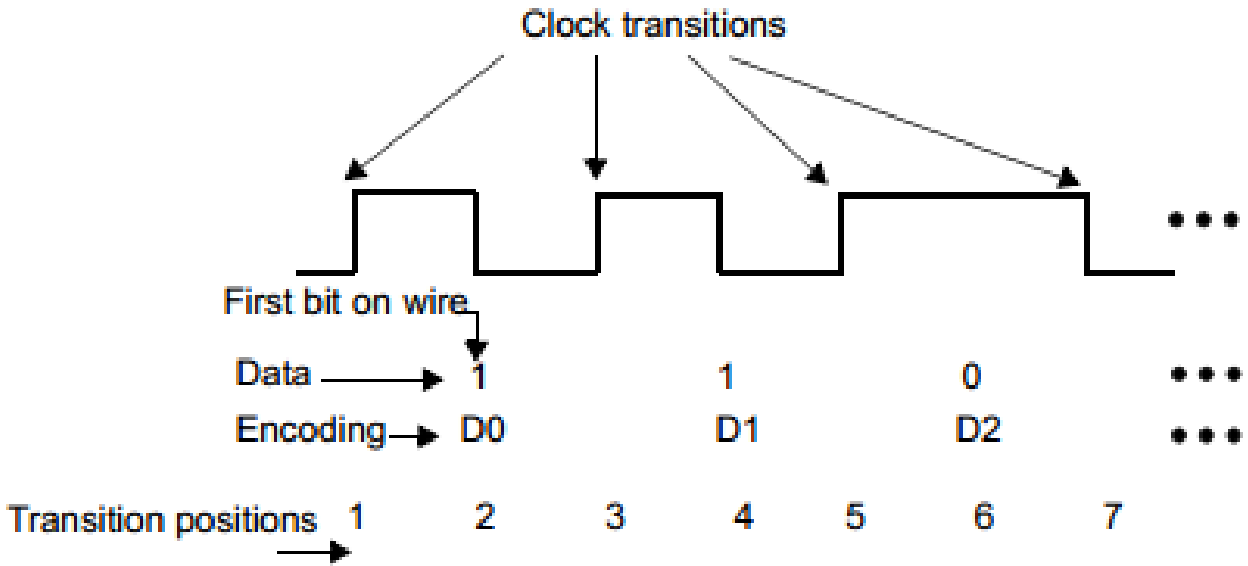




T1	Clock/Data Pulse Width	100 ns
T2	Clock Pulse to Clock Pulse	111 - 139 us
T3	Clock Pulse to Data Pulse	55.5 - 69.5 us
T5	Burst Width (16 bits)	2 ms
T5	Burst Width (48 bits)	6 ms
T6	FLP Burst to FLP Burst	8 - 24 ms
T7	Optimized FLP Burst to FLP Burst	8.0 - 8.5 ms

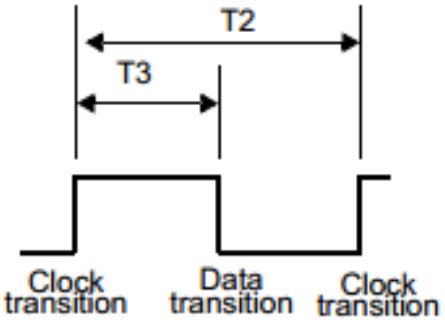
What do the pages look like? Clause 73

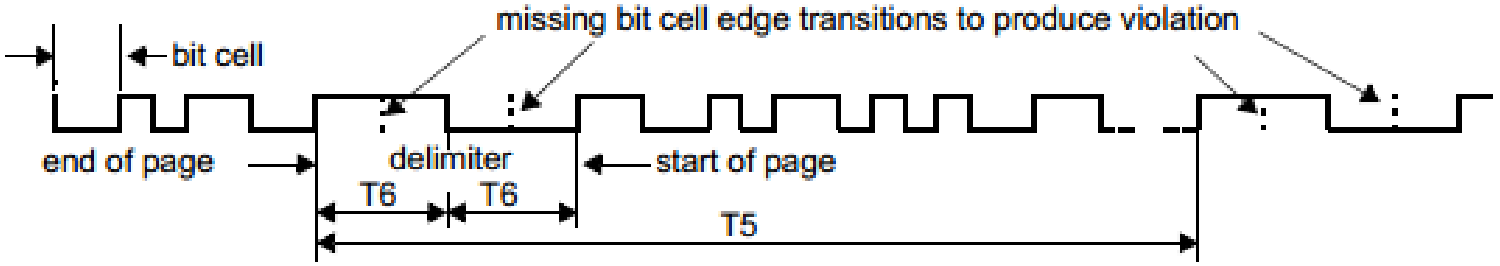
- Differential Manchester Encoding
- All Pages – 51 to 100 transitions for 48 + 1 data bits
- Additional delimiter + Transmitted non-stop
- Data transition present = 1, no data transition = 0



Pulse Spacing - Clause 73

- **DME page = 1 page**





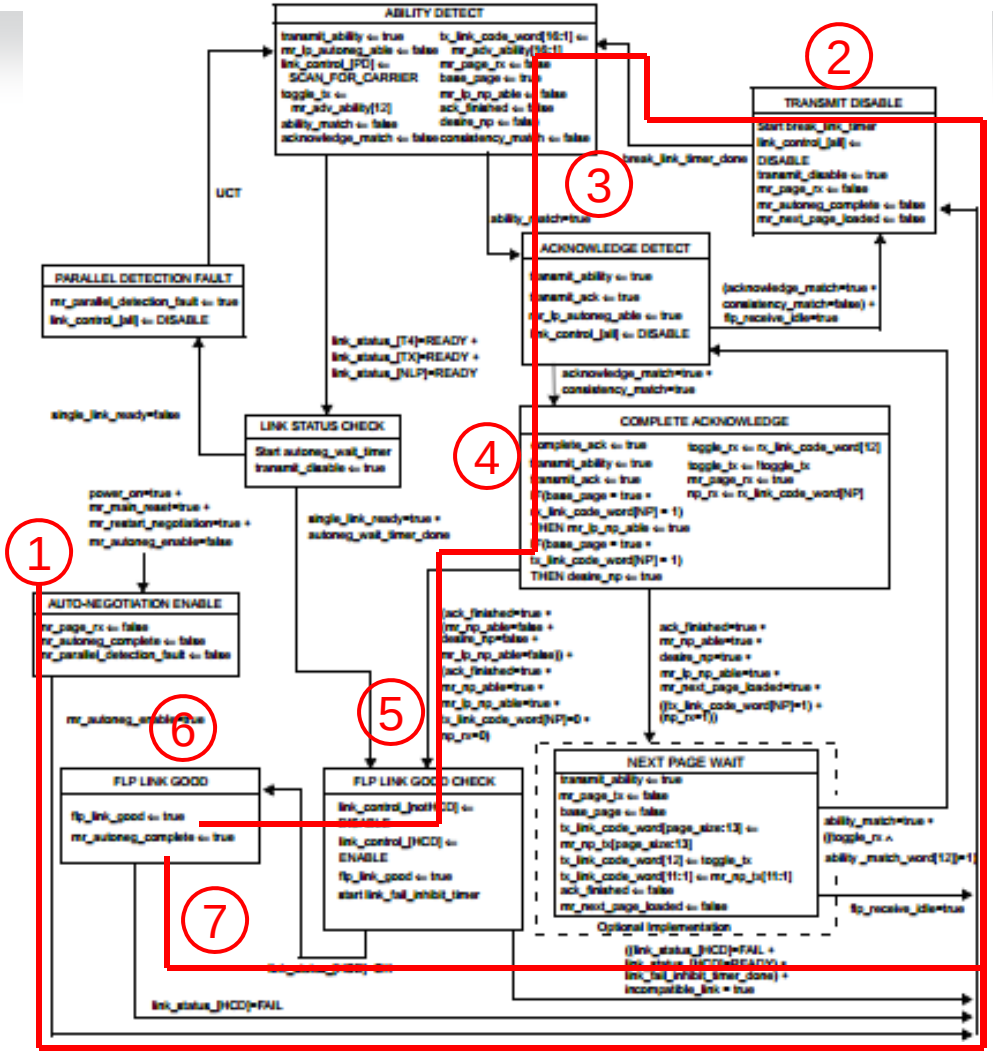
T1	Transition position spacing (period)	3.2 ns
T2	Clock transition to clock transition	6.2 - 6.6 ns
T3	Clock transition to data transition	3.0 - 3.4 ns
T5	DME page width	338.8 - 339.6 ns
T6	DME Manchester violation delimiter width	12.6 - 13.0 ns

Special bits in each page

- **Acknowledge Bit**
  - Let LP know PHY received 3 or more identical pages (not counting the acknowledge bit)
- **Next Page Bit**
  - More pages to follow after current page
- **Toggle Bit**
  - Differentiates the current page from the next one
- **Arbitration State Machine moves based on the above bits among other things**

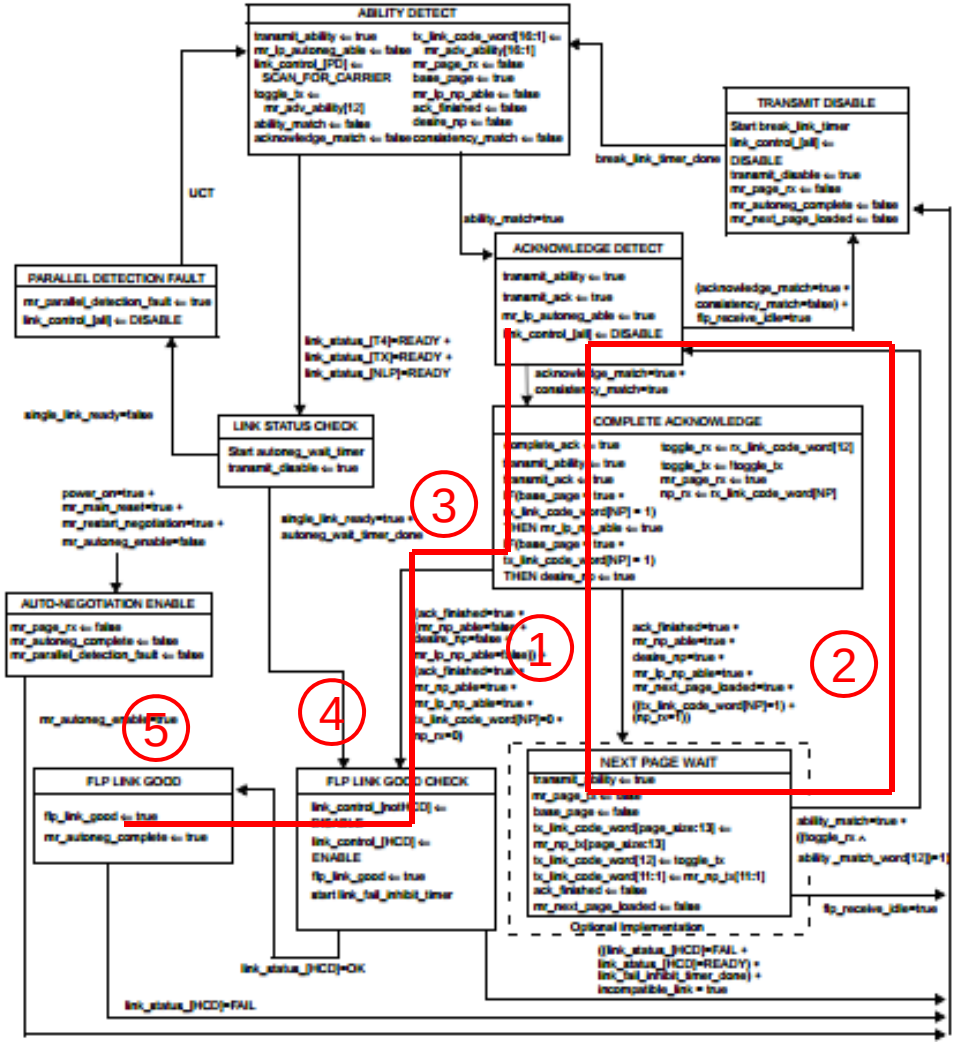
Arbitration State Machine

1) Start or Disabled
2) Wait (dead) time
3) Rx 3 identical pages (except Acknowledge bit)
4) Rx 3 identical pages with Acknowledge bit set and Next Page bit not set
5) Information exchange completed waiting for training to complete
6) Link Up
7) Lost Link



Next Page Loop

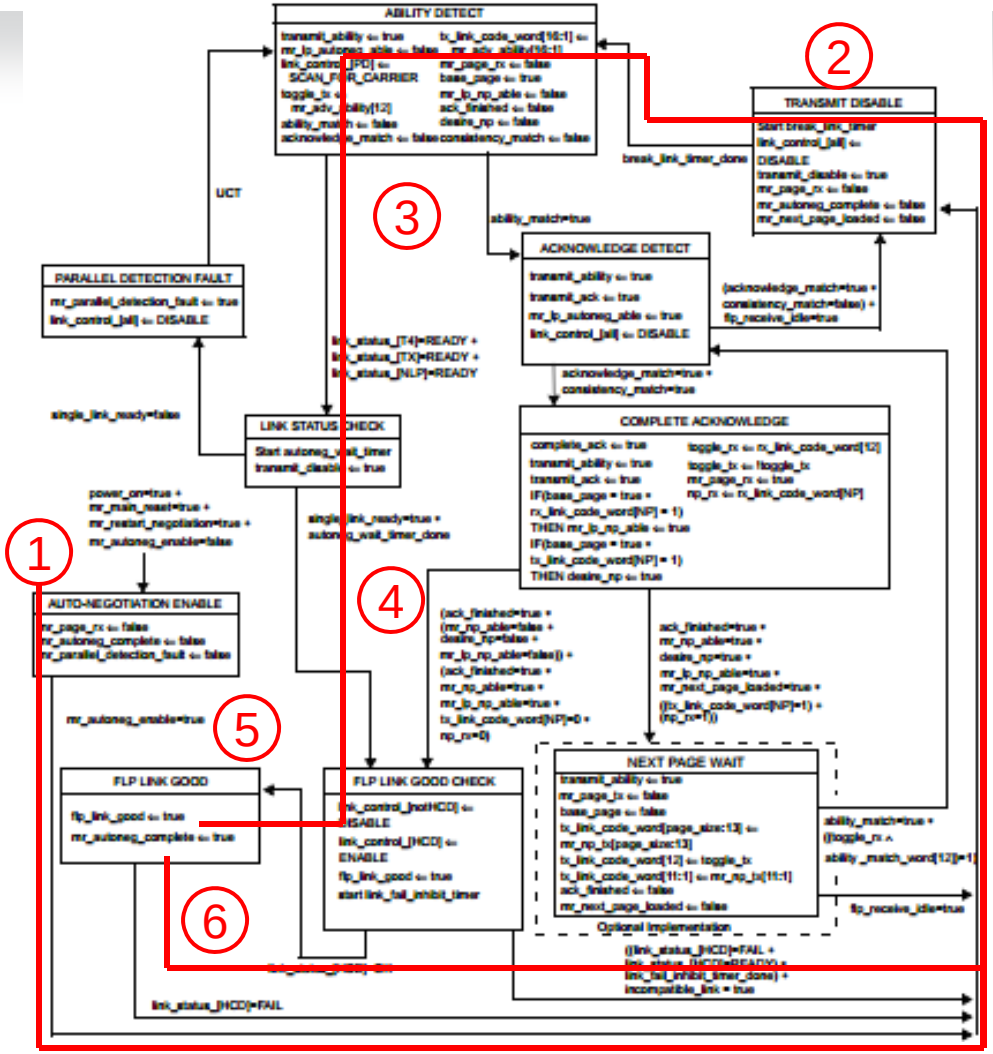
1) Rx 3 identical pages with Acknowledge bit set and Next Page bit set
2) Rx 3 identical pages (except Acknowledge bit) and Toggle bit changed
3) Rx 3 identical pages with Acknowledge bit set and Next Page bit not set
4) Information exchange completed waiting for training to complete
5) Link Up



Parallel Detect

- Detects Legacy PHY that does not support Auto-Negotiation

1) Start
2) Wait (dead) time
3) Detect activity that indicates legacy PHY
4) Single link established after some wait time
5) Link Up
6) Lost Link



Other Items

Priority Resolution

- Highest shared operational mode used

Clause 28

a) 10GBASE-T full duplex
b) 1000BASE-T full duplex
c) 1000BASE-T
d) 100BASE-T2 full duplex
e) 100BASE-TX full duplex
f) 100BASE-T2
g) 100BASE-T4
h) 100BASE-TX
i) 10BASE-T full duplex
j) 10BASE-T

Clause 73

Priority	Technology	Capability
1	100GBASE-CR10	100 Gb/s 10 lane, highest priority
2	40GBASE-CR4	40 Gb/s 4 lane
3	40GBASE-KR4	40 Gb/s 4 lane
4	10GBASE-KR	10 Gb/s 1 lane
5	10GBASE-KX4	10 Gb/s 4 lane
6	1000BASE-KX	1 Gb/s 1 lane, lowest priority

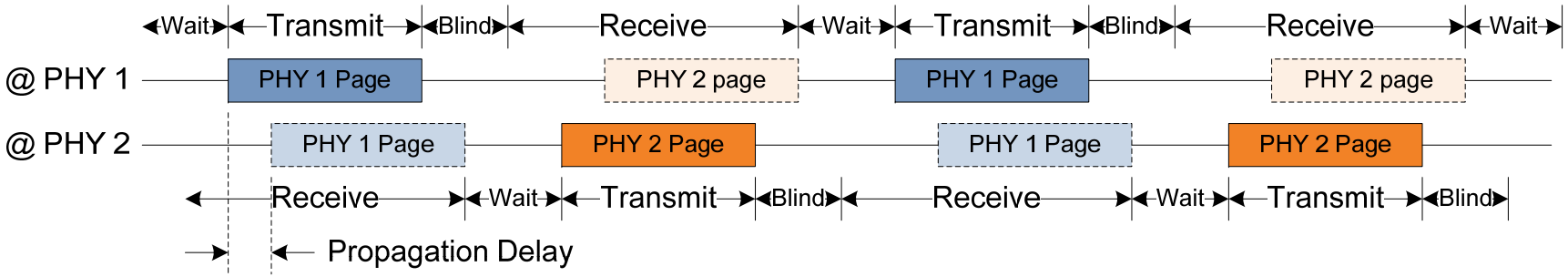
Control and Status via MDIO address space

Auto-Negotiation and 1TPCE

- Two PHYs in discussion now over single twisted pair
  - 1000BASE-T1
  - 1TPCE
- Would be good to have a mechanism to allow information exchange prior to startup
  - Similar capability to multiple twisted pair PHYs and backplane PHYs
  - Allows single pair PHYs to be deployed in application beyond closed systems where plug and play would be useful (Internet of Things)
  - Increases market potential
- Good time to make compatible with 1000BASE-T1 and 1TPCE
  - Rather than retrofit it after the fact
- No need to be compatible with multiple twisted pair Auto-Neg
  - Underlying cabling and termination are different
  - Free us to optimize design

One Twisted Pair – No Problem

- **Discussion in 1000BASE-T1 Task Force on mechanism to solve PHY startup synchronization problem**
  - **Synchronization mechanism needed to avoid potential lockup**
  - **Can get Auto-Negotiation information exchange for free**
- **Use modified Clause 73 Auto-Negotiation running half duplex**
  - **PHYs take turns sending pages on single pair**
  - **Arbitration State Machine is similar**
  - **Adapt backplane signaling (DME) to copper twister pair medium**



Auto-Negotiation is too slow – Not true

- **It is slow in Clause 28 only because it needs to be backwards compatible to legacy 10BASE-T link pulses**
- **Components to Startup Time**
  - **break_link_timer – dead wait time in beginning to break link**
  - **Actual information exchange**
  - **PHY training – technology dependent**

PHY	break_link_timer	Nominal page exchange time	Max PHY training time
100BASE-TX	1200 - 1500 ms	~ 210 ms	750 - 1000 ms
1000BASE-T	1200 - 1500 ms	~ 850 ms	750 - 1000 ms
10GBASE-T	1200 - 1500 ms	~ 220 ms	2000 - 2250 ms
10GBASE-KR	60 - 75 ms	~ 9 us	500 - 510 ms
1000BASE-T1 *	100 us	< 1 ms	99 ms
1TPCE *	100 us	< 1 ms	TBD

* With current proposed timer values

Recommendation

- **Add Auto-Negotiation to 1TPCE Objectives**

- **Increases Market Potential**
- **Small Overhead**
- **Technically Feasible**

THANK YOU