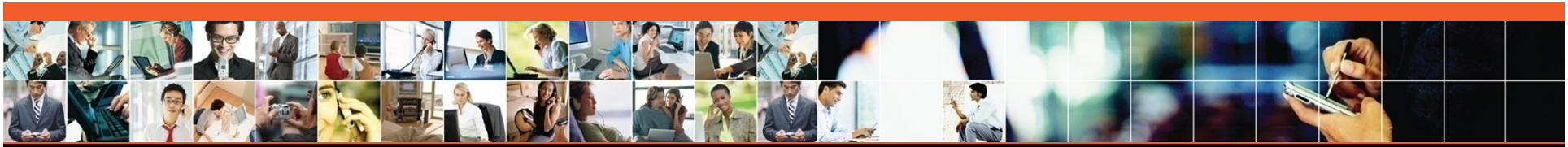


Sub-Layering for 25GbE

25G Ethernet Study Group – Nov 2014

William Lo, Venugopal Balasubramonian, Marvell

Objective

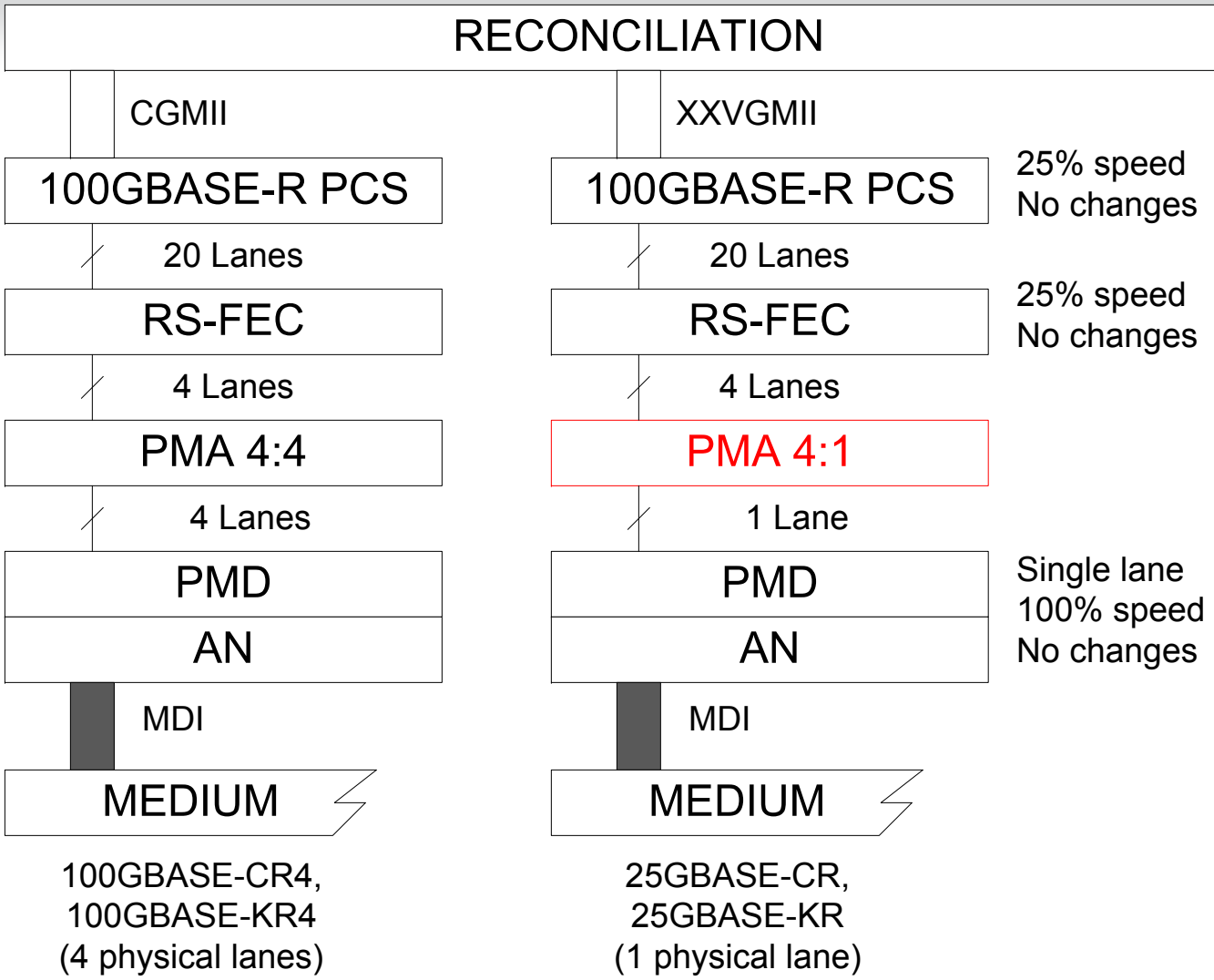
- **Support 25GBASE-* with minimal changes to existing 100GBASE-* Clauses**
- **Simple uniform changes applicable to all 100GBASE-*R4 PHYs**
  - **Slow down to 25% speed with no functional changes to RS, MII, PCS, or RS-FEC**
  - **4 lanes to 1 lane reduction in PMA, PMD keeping functional and electrical parameters unchanged**
  - **Define new PMA ratios of 20:1, 4:1, and 1:1**
  - **Add capabilities in Auto-Negotiation**
  - **Preserves EEE mechanics**

Sub-Layer Modification Summary

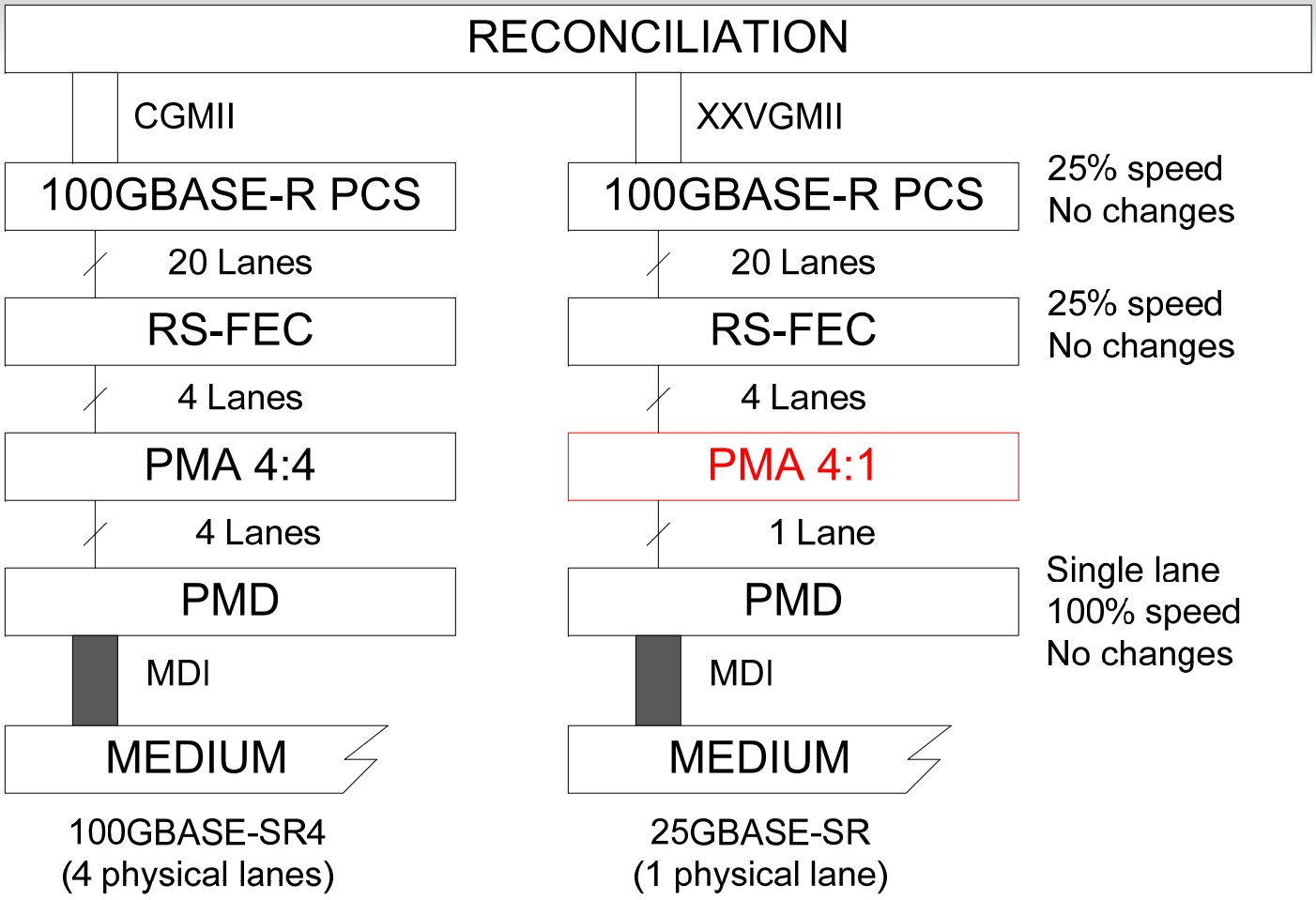
		Clause														
		73	78	81		82	83	83D	83E	88		91	92	93	94	95
Existing	Possible	Auto-Negotiation	EEE	RS	CGMII	100GBASE-R PCS	100GBASE-R PMA	CAUI	CAUI	100GBASE-LR4 PMD	100GBASE-ER4 PMD	RS-FEC	100GBASE-CR4 PMD	100GBASE-KR4 PMD	100GBASE-KP4 PMD	100GBASE-SR4 PMD
100GBASE-KR4	25GBASE-KR	Add 25G Capal	Same	Same - Slow down 4x	Same - Slow down 4x	Same - Slow down 4x	Define 4:1 PMA	Same - 1 Lane				Same - Slow down 4x		1 Lane		
100GBASE-CR4	25GBASE-CR												1 Lane			
100GBASE-SR4	25GBASE-SR								Same - 1 Lane							1 Lane
100GBASE-LR4	25GBASE-LR						Define 20:1			1 WL						
100GBASE-ER4	25GBASE-ER										1 WL					

MARVELL

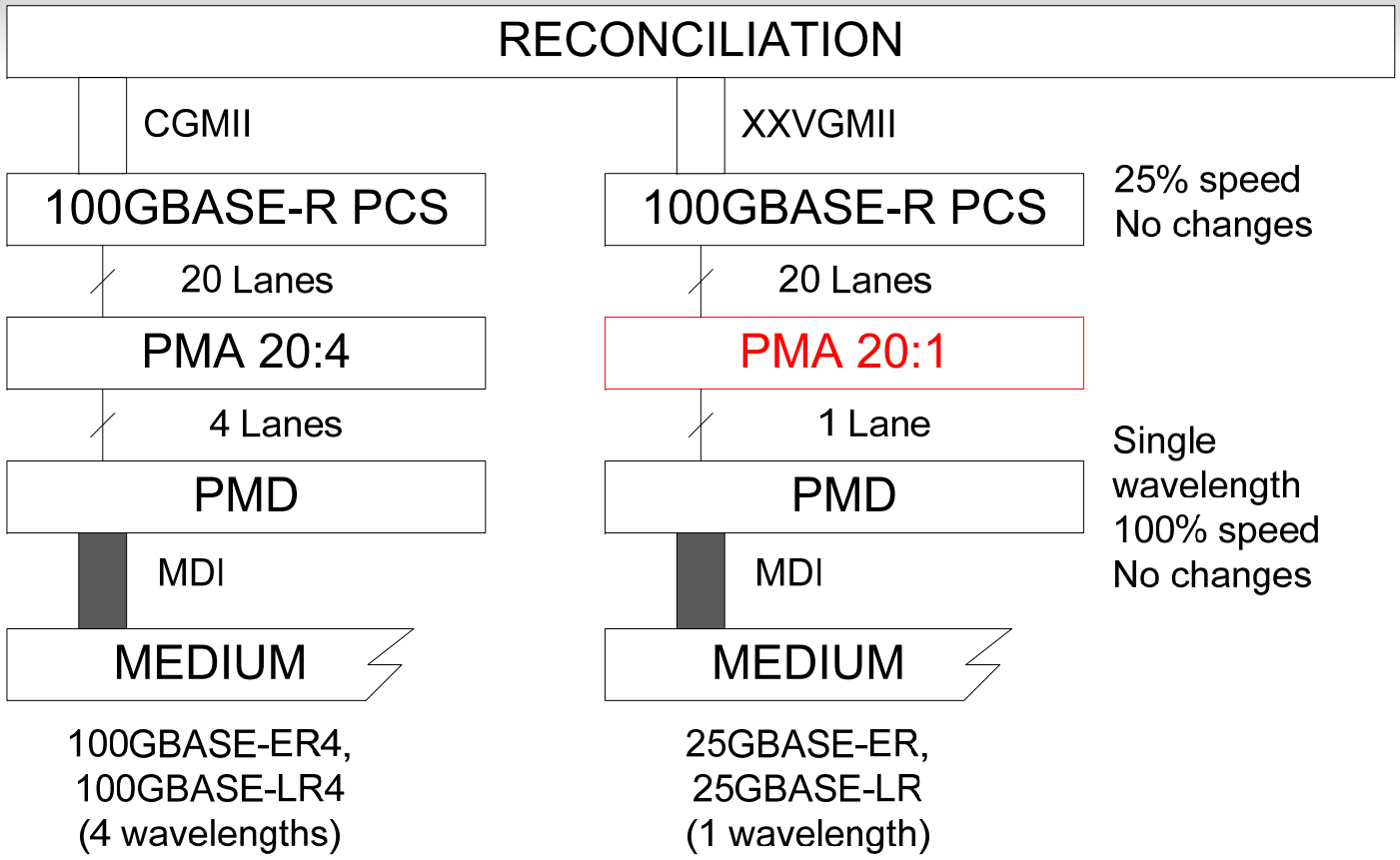
25GBASE-CR, 25GBASE-KR



25GBASE-SR

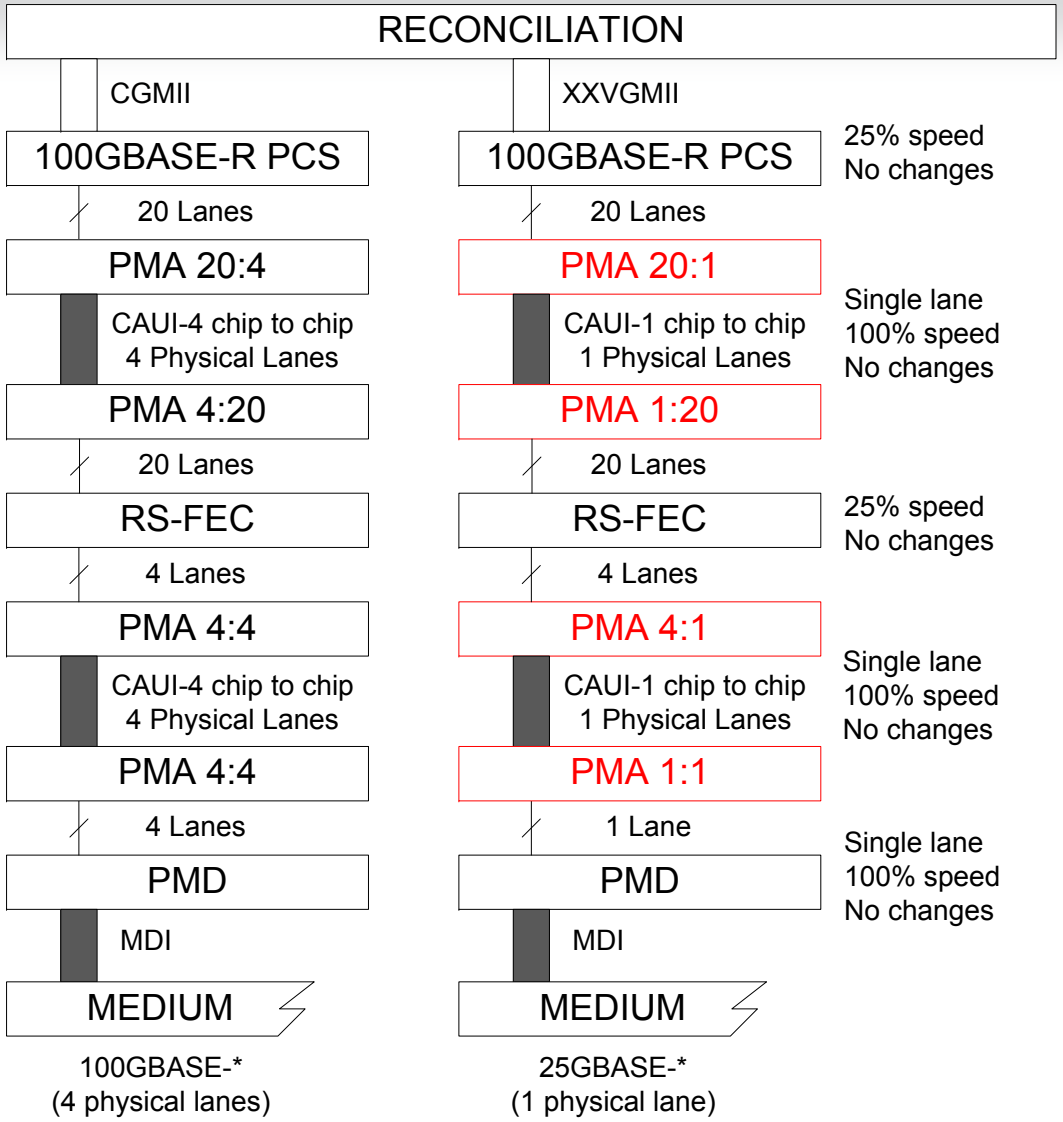

RECONCILIATION
CGMII
XXVGMII
100GBASE-R PCS
100GBASE-R PCS
25% speed
No changes
20 Lanes
20 Lanes
RS-FEC
RS-FEC
25% speed
No changes
4 Lanes
4 Lanes
PMA 4:4
PMA 4:1
4 Lanes
1 Lane
PMD
PMD
Single lane
100% speed
No changes
MDI
MDI
MEDIUM
MEDIUM
100GBASE-SR4
(4 physical lanes)
25GBASE-SR
(1 physical lane)

25GBASE-ER, 25GBASE-LR

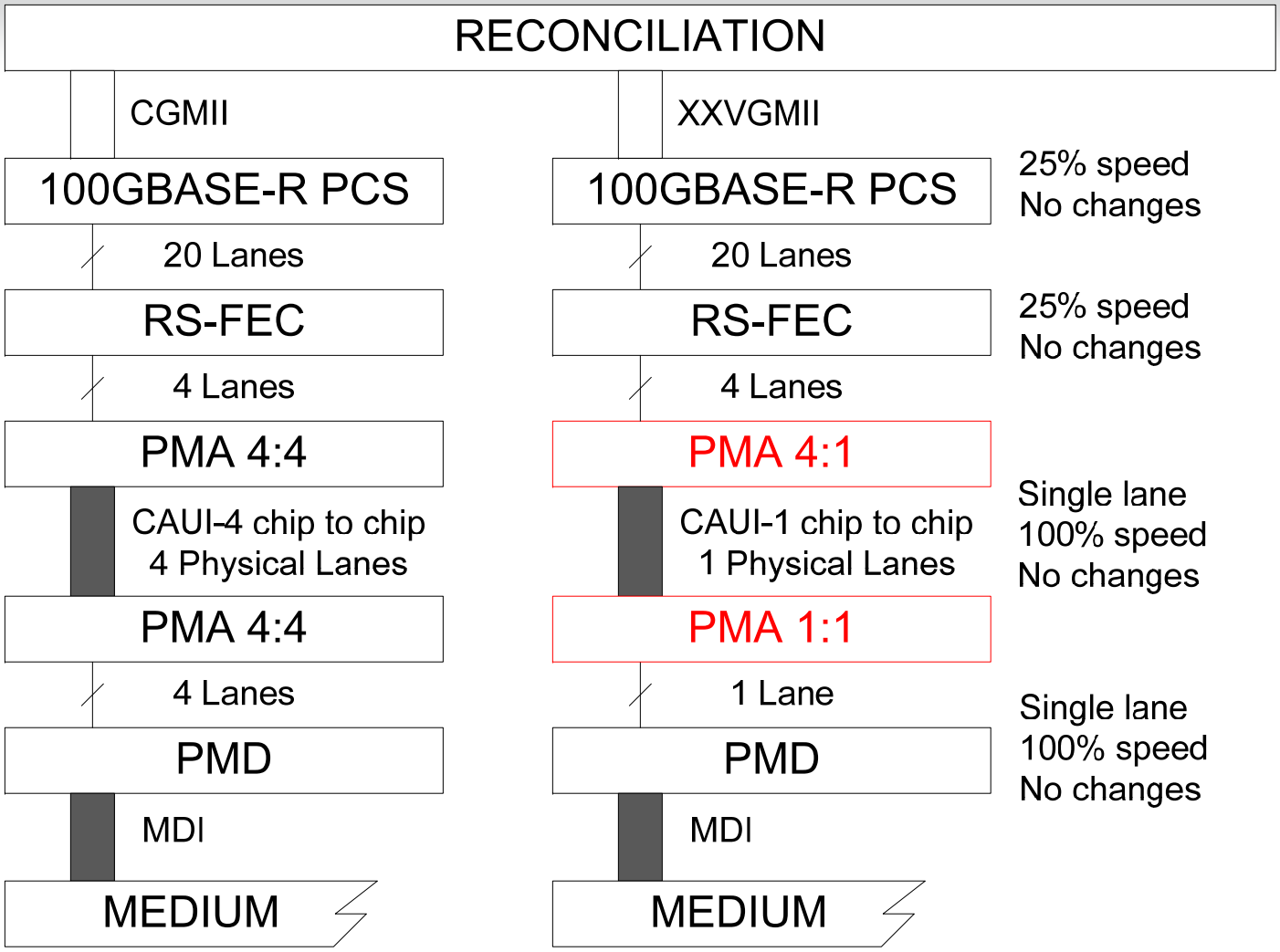


- **20:1 PMA can form XXVAUI (see later slide)**
  - **XXVAUI referenced as CAUI-1 to compare with CAUI-4**

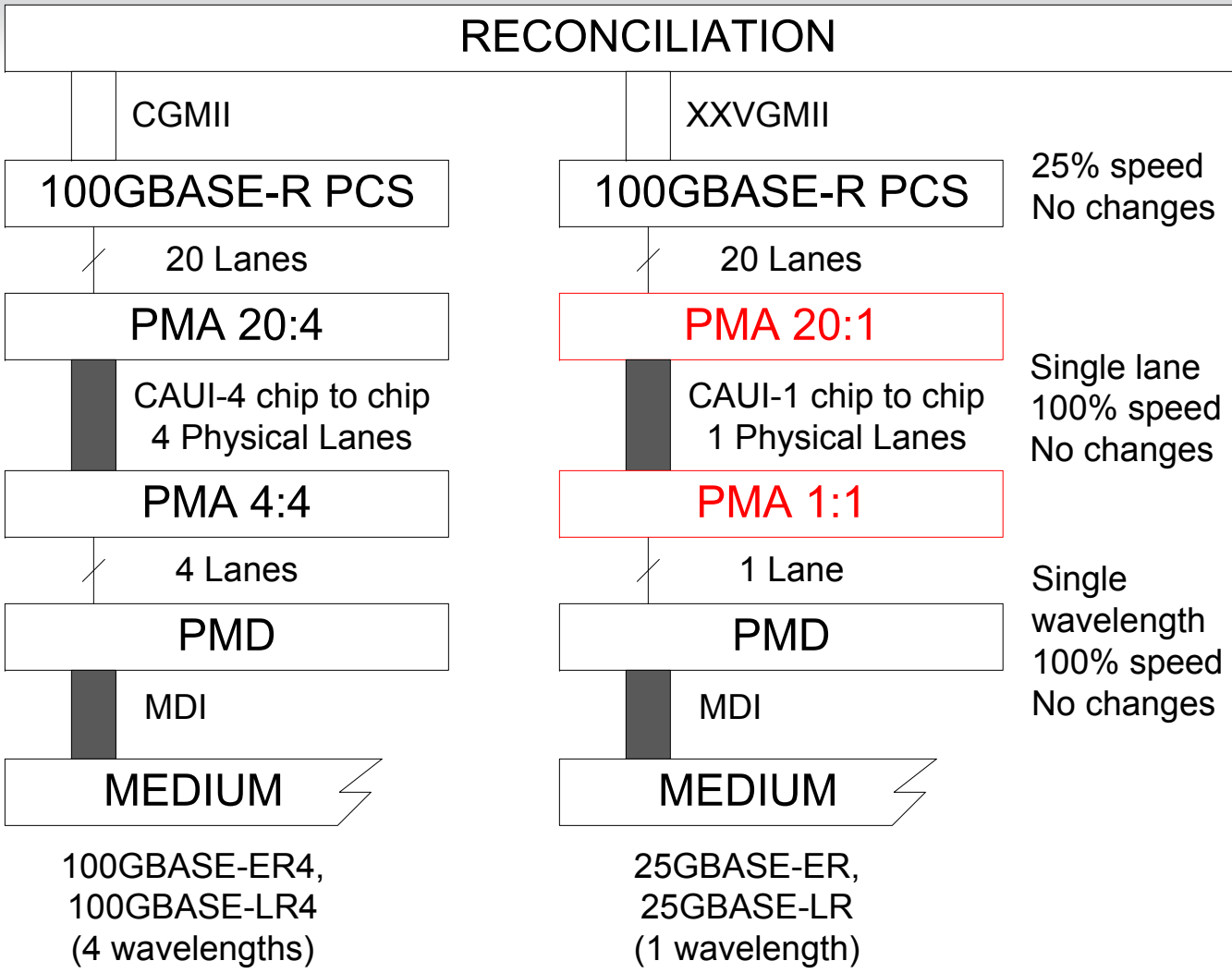
CAUI-1 Chip to Chip



CAUI-1 Chip to Module - SR



CAUI-1 Chip to Module – ER. LR



Clause 83 PMA

- Clause 83 PMA set up to easily define bit mux ratios
  - z = 20 for PCS – no change from 100G
  - z = 4 for FEC – no change from 100G
  - m, n = 1 instead of 4 for PMA, PMD
  - z:n = 20:1 or 4:1
  - m:n = 1:1
- Need to specify the lane speed for 25G

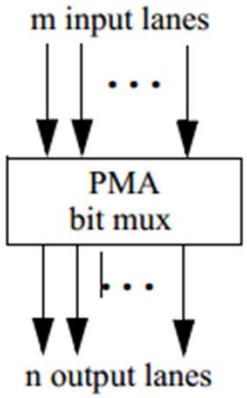


Figure 83–3—PMA bit mux used in both Tx and Rx directions

Summary

- **No changes to RS, MII, PCS, RS-FEC from 100GBASE-* except slow down to 25%**
  - **Uniform PCS implementation including alignment markers for all cases**
  - **No need for new RS-FEC framing**
- **No changes to PMA, PMD, CAUI except change from 4 lanes to 1 lane**
  - **All electrical parameters remain unchanged**
- **Fastest way to standardize 25GBASE-***
  - **Uses existing 100GBASE-* and EEE machinery**
  - **Simple addition of bit mux definitions for 20:1, 4:1, and 1:1**

THANK YOU