25 Gb/s Ethernet Study Group
CSD: Technical Feasibility

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25 Gb/s Technology Feasibility

from http://www.ieee802.org/3/cfi/0714_1/CFI_01_0714.pdf

Wealth of Prior Experience

Technology	Nomenclature	Description	Status
Backplanes	100GBASE-KR4 100GBASE-KP4	4 x 25 Gb/s (NRZ) 4 x 25 Gb/s (PAM-4)	IEEE Std 802.3bj™-2014 Ratified
Cu Twin-Axial	100GBASE-CR4	4 x 25 Gb/s	
Chip-to-Chip	CAUI-4	4 x 25 Gb/s	IEEE P802.3bm in Sponsor Ballot
Chip-to-Module	CAUI-4	4 x 25 Gb/s	
Module Form Factor	SFP28	1 x 25 Gb/s	Summary Document SFF-8402
	QSFP28	4 x 25 Gb/s	Style 1 - MDI for 100GBASE-CR4 Summary Document SFF-8665
	CFP2	4 x 25 Gb/s	
	CFP4	4 x 25 Gb/s	Style 2 - MDI for 100GBASE-CR4

from http://www.ieee802.org/3/cfi/0714_1/CFI_01_0714.pdf

25Gb/s MAC/PCS/FEC Technical Feasibility

- The MAC is feasible in existing technology, and designs can leverage a 40GbE MAC and run it slower, or run a 10GbE MAC faster (with possibly a wider bus width)
- The PCS is feasible in existing technology, some possible PCS choices are:
  - Re-use the 10GbE PCS, 64B/66B, but run 2.5x faster (at possibly a wider bus width than a current 10GbE PCS). Can re-use the 10GBASE-KR FEC if desired and if it provides enough gain for possible PMDs
  - Re-use the 10GbE PCS and re-use the 802.3bj RS-FEC sublayer (both run at 25G), use transcoding to keep the same lane rate after adding the RS-FEC. Note the latency will be longer than it is for 100GbE.
  - Re-use the 40GbE PCS with or without alignment markers and 802.3bj RS-FEC sublayer (both run at 25G), use transcoding to keep the same lane rate after adding the RS-FEC. Note the latency will be longer than it is for 100GbE.
- Possible data path widths in FPGAs: 64b @400MHz
  - Compact IP is possible, taking a small fraction of an FPGA
- Possible data path widths in ASICs: 32b @800MHz
  - Compact IP is possible
- Time-sliced MAC/PCS designs are feasible and can handle multi-rate implementations

based on http://www.ieee802.org/3/cfi/0714_1/CFI_01_0714.pdf

25Gb/s Single Lane Technical Feasibility

- SERDES Technology widely available
  - Under discussion among SERDES vendors since ~2002
  - OIF Project in July 2005
  - Several OIF CEI-25 and CEI-28 flavors in 2010/2011 time frame
  - Defined in IEEE P802.3bj as a 25Gb/s 4 lane electrical interface
  - Shipping ASIC cores for ~3 to 4 years
  - Defined channel models for circuit boards, direct attach cables, and connectors
- Technology re-use
  - Single-lane of 100GbE 4-lane PMD and CAUI-4 specifications
  - SFP28 being developed for 32G FC

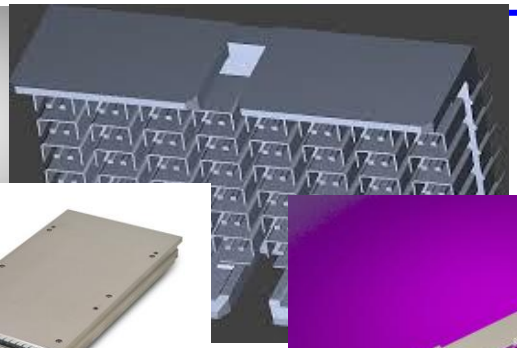
from http://www.ieee802.org/3/cfi/0714_1/CFI_01_0714.pdf

25Gb/s Optical Technical Feasibility

- Technical feasibility - 32G Fibre Channel and 802.3bm standards
  - ***No technical risk + extensive industry experience + full suite of existing standards near completion to draw from = rapid standardization***
- Incremental work needed to define a PHY for 25Gb/s over MMF
  - Single lane FEC
    - FEC option required for backplane, re-use for optics (as in 100GBASE-SR4/KR4)
  - Chip-to-module interface
    - Needed for AOCs and for pluggable optics.
    - Technology re-use of 25Gb/s lane standards e.g. clause 83E chip-to-module specs (slide 18 of *CFI_01_0714*)
  - Electrical connector
    - Re-use copper twin-ax cables MDI: SFP28, QSFP28, CFP4
  - Optical interface specs
    - Re-use 32GFC and 100GBASE-SR4, both of which include applicable ~25Gb/s optical lane specifications.
    - No new component developments.
    - <1 Watt SFP+ form factor established for early 32GFC samples
  - Optical MDI
    - Same MDI as SFP+ and QSFP optical modules: LC and MPO connectors
  - Optical modules available in SFP28, CFP/CFP2, QSFP28, and CFP4
- Summarized from king_25GE_02_0914

25Gb/s Technologies Readily Available

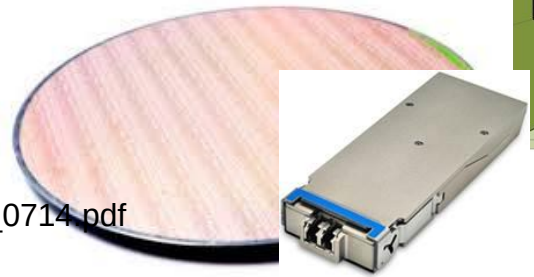


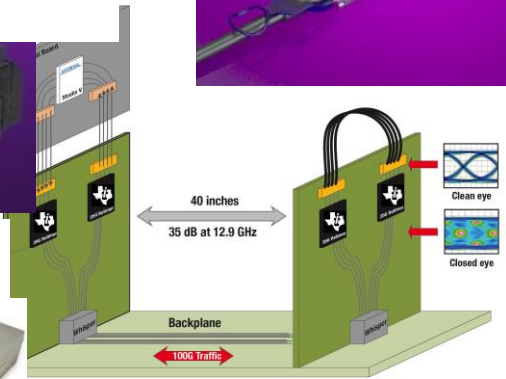










from http://www.ieee802.org/3/cfi/0714_1/CFI_01_0714.pdf

Provided by Amphenol, Molex, TE, Xilinx, Finisar

Architecture and Optical ad-hocs

- Significant discussions on options and technical feasibility
  - TF will have solutions available to them
- Summary presented earlier. See:

  http://www.ieee802.org/3/25GSG/public/Sept14/brown_25GE_02_0914.pdf

CSD: Technical Feasibility

Each proposed IEEE 802 LMSC standard shall provide evidence that the project is technically feasible within the time frame of the project. At a minimum, address the following items to demonstrate technical feasibility:

a) Demonstrated system feasibility.

b) Proven similar technology via testing, modeling, simulation, etc.

- Systems based upon 25 Gb/s technology have been demonstrated and deployed in operational networks.
- The proposed project will build on the array of Ethernet component and system design experience, and the broad knowledge base of Ethernet network operation.
- Component technology at 25Gb/s, developed for other Ethernet standard (IEEE Std 802.3bj) and project (IEEE P802.3bm), are available and in production.
- The reliability of Ethernet components and systems has been established in the target environments with a high degree of confidence.

Straw Poll & Motions

Currently planning to have a motion to adopt Technical feasibility CSD response later in meeting

For now:
Straw Poll: I support adopting CSD: ”Technical Feasibility” as written in goergen_25GE_01_0914d.pdf

Y: N: A: