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# **802.3 25 Gb/s Study Group Technical Feasibility Consistent with 802.3bj Channel Related Specifications**

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# Purpose

- Provide information related to developing the technical feasibility criteria for 802.3 25 Gb/s.
- (Five Criteria) are defined in subclause 12.5 of the 'IEEE project 802 LAN/MAN Standards Committee (LMSC) operations manual'. These are supplemented by subclause 7.2 'Five Criteria' of the 'Operating Rules of IEEE Project 802 Working Group 802.3, CSMA/CD LANs'.
  - Broad Market Potential
  - Compatibility
  - Distinct Identity
  - Technical Feasibility
  - Economic Feasibility
- 25G consistent with 802.3bj channel/system related specifications
  - Test points
  - Channel loss budget
  - Cable assembly specifications
  - Test fixture specifications
  - COMS
- MDI – SFF-8084 (see SFF-8402 Specification for SFP+ 28 Gb/s 1x Pluggable Transceiver Solution (SFP28) Rev 1.0 March 30, 2014)

# 100GBASE-CR4 PMD

- The 100GBASE-CR4 PMD has four parallel bit streams each operating at a nominal signaling rate of 25.78125 GBd

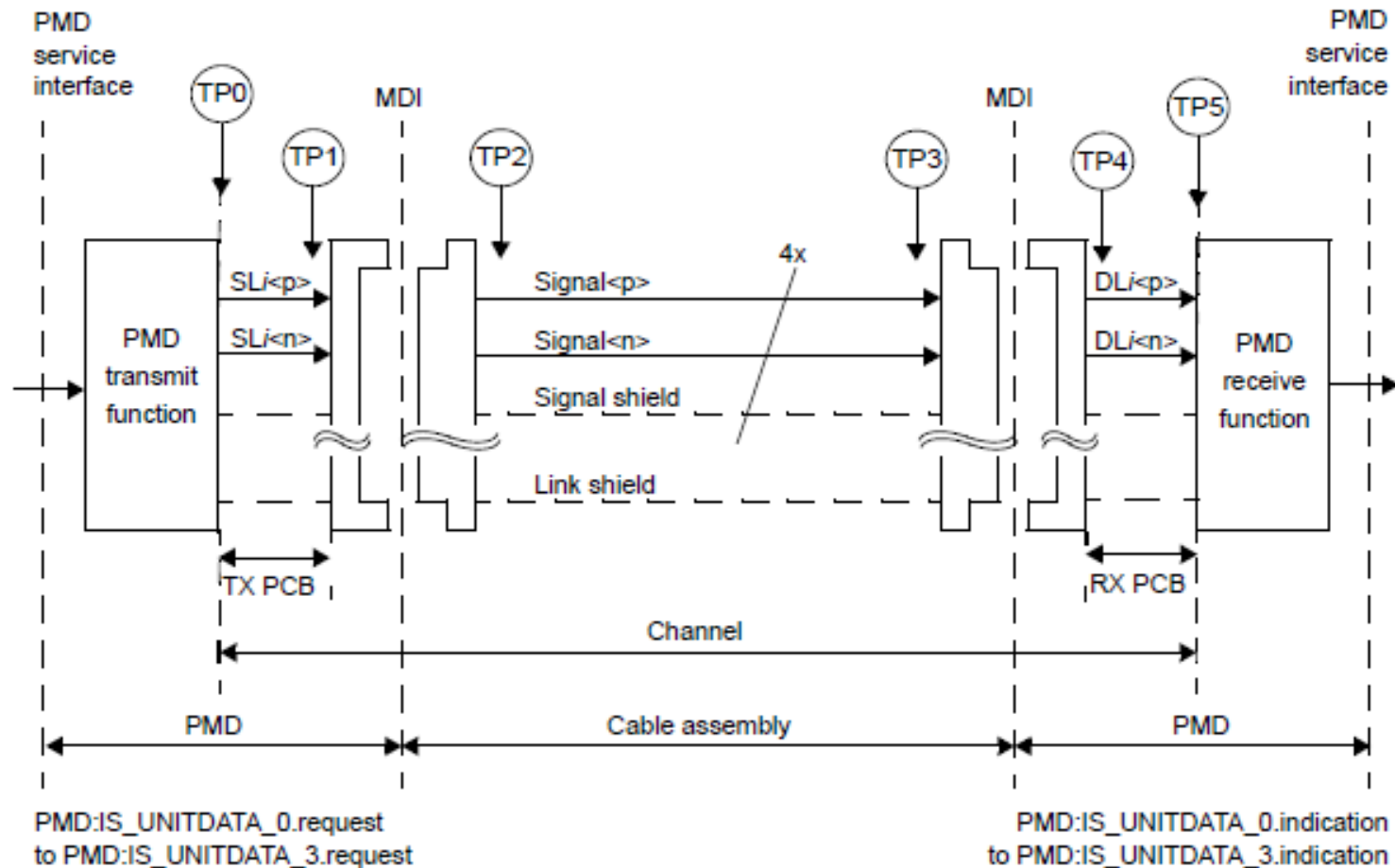


Figure 92-2—100GBASE-CR4 link (one direction is illustrated)

# 100GBASE-CR4 – Test Points

**Table 92–4—100GBASE-CR4 test points**

Test points	Description
TP0 to TP5	The 100GBASE-CR4 channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92–2. The cable assembly test fixture of Figure 92–17 or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 92.8.3 and 92.8.4. The recommended maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 92.8.3.6.
TP2	Unless specified otherwise, all transmitter measurements defined in Table 92–6 are made at TP2 utilizing the test fixture specified in 92.11.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 92.8.4 are made at TP3 utilizing the test fixture specified in 92.11.1.

# 100GBASE-CR4 - Objectives

## Objectives

- Support full-duplex operation only
- Preserve the 802.3 / Ethernet frame format utilizing the 802.3 MAC
- Preserve minimum and maximum FrameSize of current 802.3 standard
- Support a BER of better than or equal to  $10^{-12}$  at the MAC/PLS service interface
- Define a 4 lane PHY for operation over a printed circuit board backplane with a total channel insertion loss of  $\leq 35$  dB at 12.9 GHz\*\*
- Define a 4 lane PHY for operation over a printed circuit board backplane with a total channel insertion loss of  $\leq 33$  dB at 7.0 GHz\*\*
- Define a 4-lane 100 Gb/s PHY for operation over links consistent with copper twin-axial cables with lengths up to at least 5m.
- To define optional Energy-Efficient Ethernet operation for 100G Backplane and Twinaxial cable PHYs specified in P802.3bj\*
- To define optional Energy-Efficient Ethernet operation for 100GBASE-CR10\*\*\*
- To define optional Energy-Efficient Ethernet operation for 40GBASE-CR4 and 40GBASE-KR4\*\*\*

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IEEE P802.3bj 100Gb/s Backplane  
and Copper Cable Task Force

Objectives approved by IEEE 802.3 WG July 2011 IEEE 802 Plenary

\* Objective approved by IEEE 802.3 WG Nov 2011 IEEE 802 Plenary

\*\* Objectives approved by IEEE 802.3 WG Mar 2012 IEEE 802 Plenary

\*\*\* Objectives approved by IEEE 802.3 WG July 2012 IEEE 802 Plenary

- Operation over links consistent with copper twin-axial cables with lengths up to at least 5m at a nominal signaling rate of 25.78125 GBd supported.

# 25 Gb/s CFI - Technical Feasibility

## 25Gb/s Single Lane Technical Feasibility

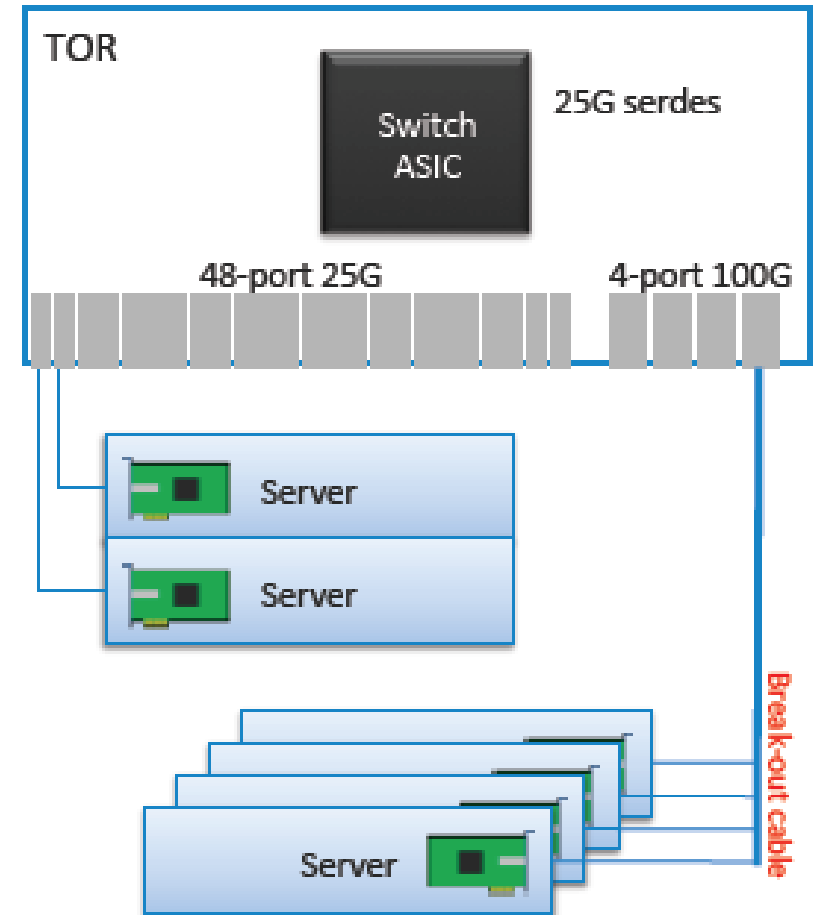
- SERDES Technology widely available
  - Under discussion among SERDES vendors since ~2002
  - OIF Project in July 2005
  - Several OIF CEI-25 and CEI-28 flavors in 2010/2011 time frame
  - Defined in IEEE P802.3bj as a 25Gb/s 4 lane electrical interface
  - Shipping ASIC cores for ~3 to 4 years
  - Defined channel models for circuit boards, direct attach cables, and connectors
- Technology re-use
  - Single-lane of 100GbE 4-lane PMD and CAUI-4 specifications
  - SFP28 being developed for 32G FC

*Source: 25 Gb/s Ethernet Over a Single Lane for Server Interconnect Call For Interest Consensus IEEE 802 July 2014 Plenary, San Diego, CACFI\_01\_0714*

# 25 Gb/s Ethernet Connectivity

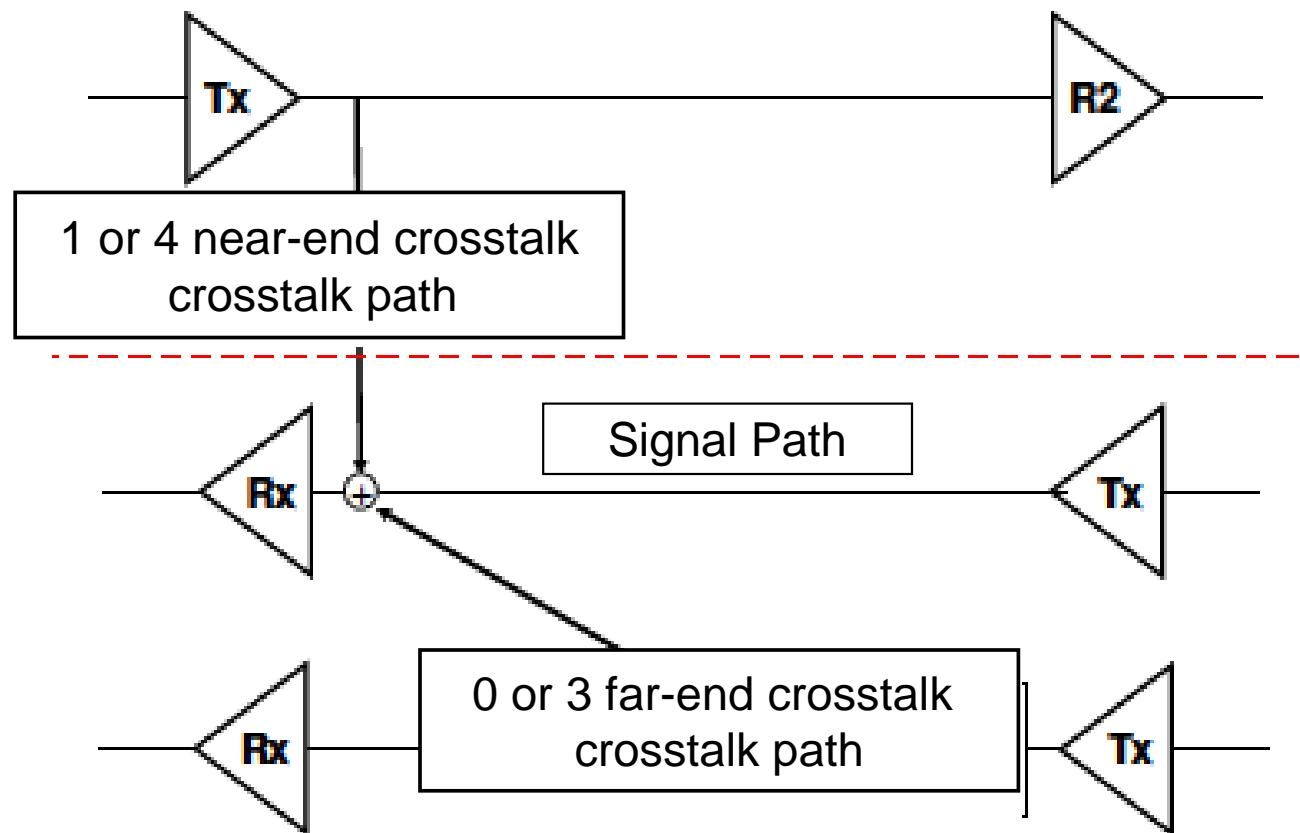
## 25Gb/s Ethernet Connectivity

- Enables similar topology as 40Gb/s & 10Gb/s
  - Single 25Gb/s SFP28 port implementation or Quad 25Gb/s QSFP28 breakout implementation possible
  - Maximizes ports and bandwidth in ToR switch faceplate
  - Dense rack server
  - Within rack, less than 3m typical length



Source: 25 Gb/s Ethernet Over a Single Lane for Server Interconnect Call For Interest Consensus IEEE 802 July 2014 Plenary, San Diego, CACFI\_01\_0714.pdf

# 25 Gb/s Ethernet Connectivity– crosstalk paths



- 1 port to 1 port – Consistent with 802.3bj
- 4 port to 4x1 port breakout – Consistent with 802.3bj
- 4 port to 4 port - Consistent with 802.3 bj



# 25 Gb/s Ethernet – Cable assembly

## 92.10 Cable assembly characteristics

92.10.1 Characteristic impedance and reference impedance

92.10.2 Cable assembly insertion loss

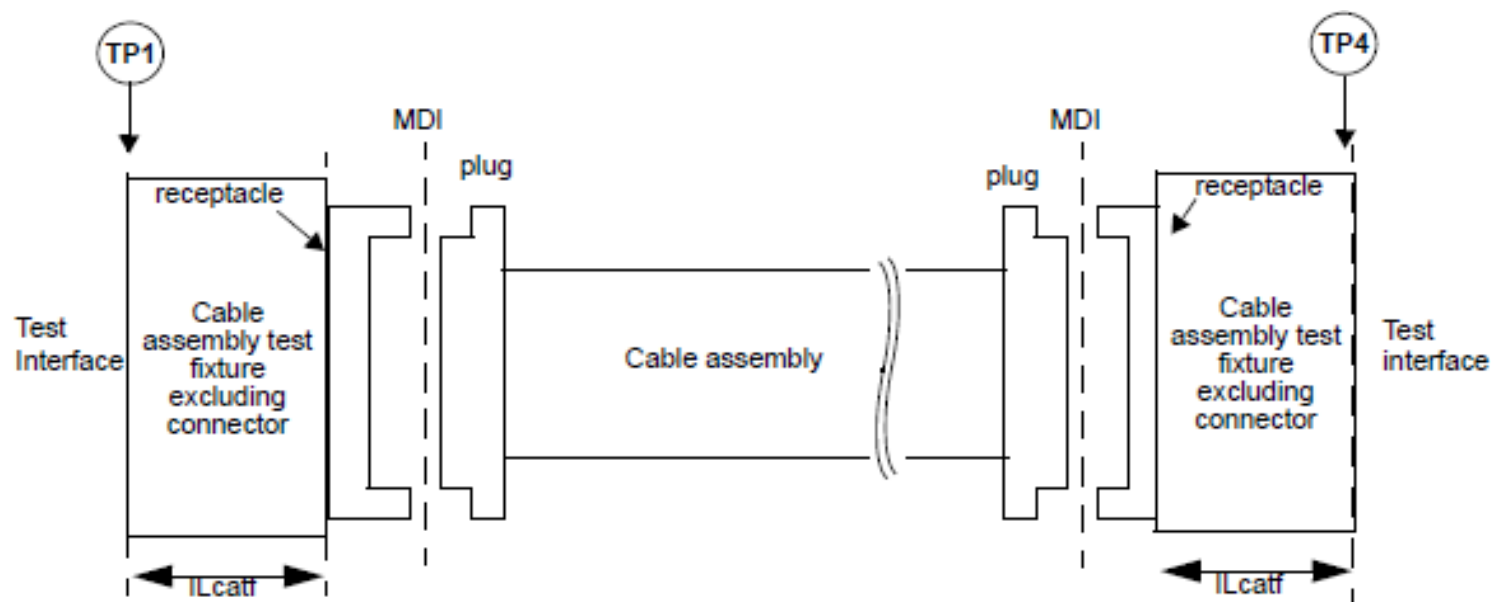
92.10.3 Cable assembly differential return loss

92.10.4 Differential to common-mode return loss

92.10.5 Differential to common-mode conversion loss

92.10.6 Common-mode to common-mode return loss

92.10.7 Cable assembly Channel Operating Margin



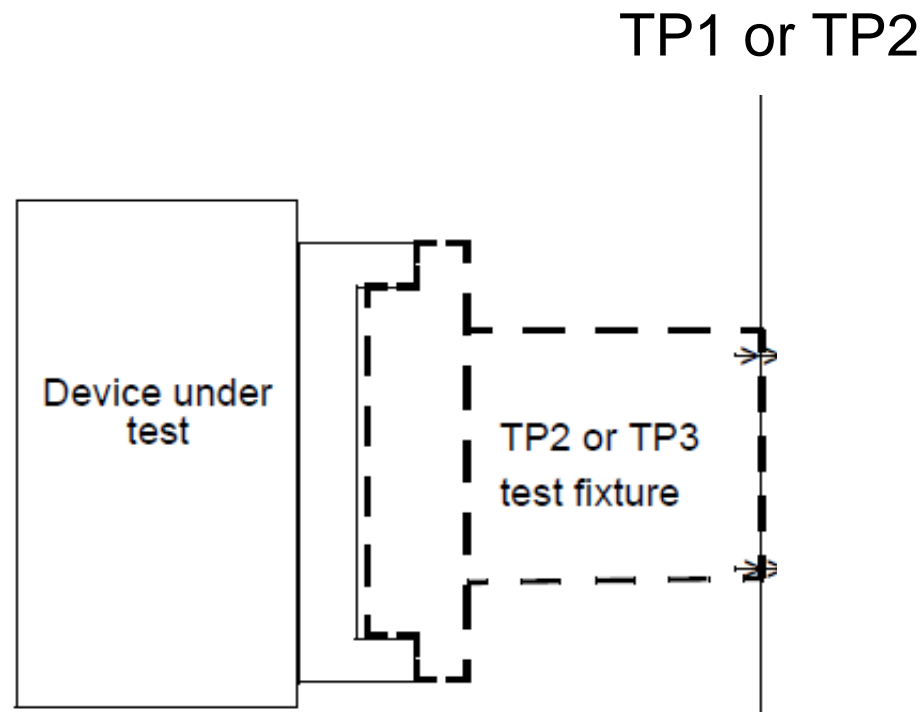
# 25 Gb/s Ethernet – Test Fixtures

## 92.11 Test Fixtures

### 92.11.1 TP2 or TP3 test fixtures (Host Compliance Boards)

#### 92.11.1.1 Test fixture return loss (Mated)

#### 92.11.1.2 Test fixture insertion loss (PCB reference insertion loss)



# 25 Gb/s Ethernet – Test Fixtures

92.11.2 Cable assembly test fixture (Module Compliance Board)

>>>PCB reference insertion loss

92.11.3 Mated test fixtures

92.11.3.1 Mated test fixtures insertion loss

92.11.3.2 Mated test fixtures return loss

92.11.3.3 Mated test fixtures common-mode conversion loss

92.11.3.4 Mated test fixtures common-mode return loss

92.11.3.5 Mated test fixtures common-mode to differential-mode return loss

92.11.3.6 Mated test fixtures integrated crosstalk noise

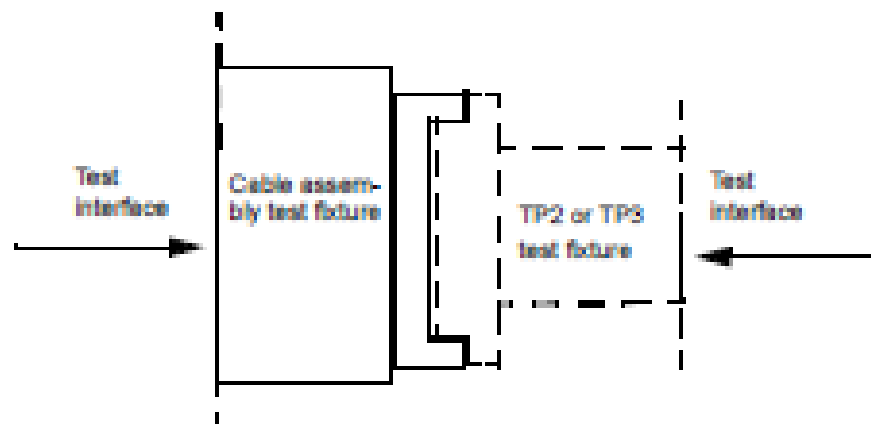


Figure 92-18—Mated test fixtures

# Channel characteristics

92A.1 Overview

92A.2 Transmitter characteristics at TP0

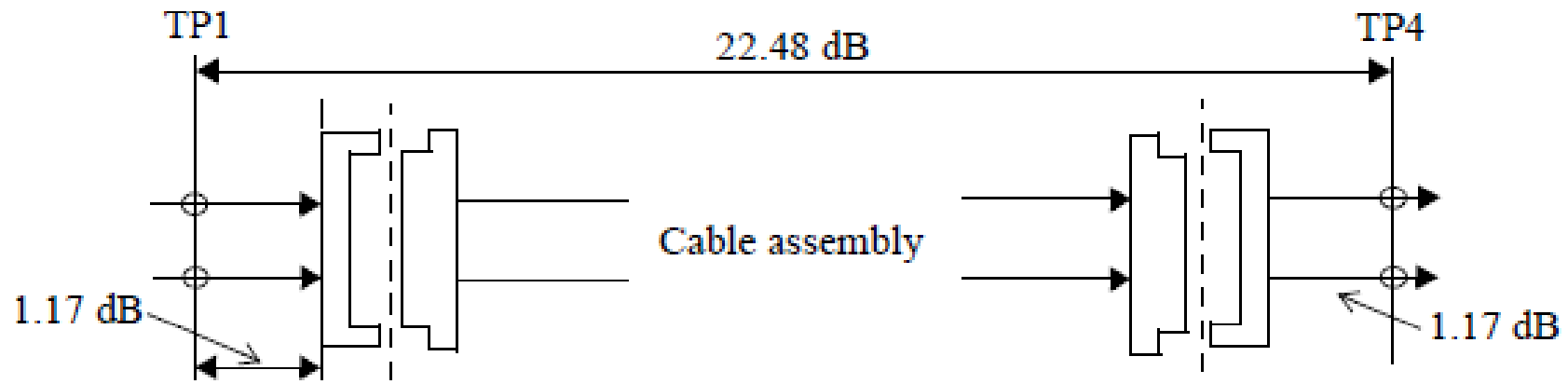
92A.3 Receiver characteristics at TP5

92A.4 Transmitter and receiver differential printed circuit board trace loss

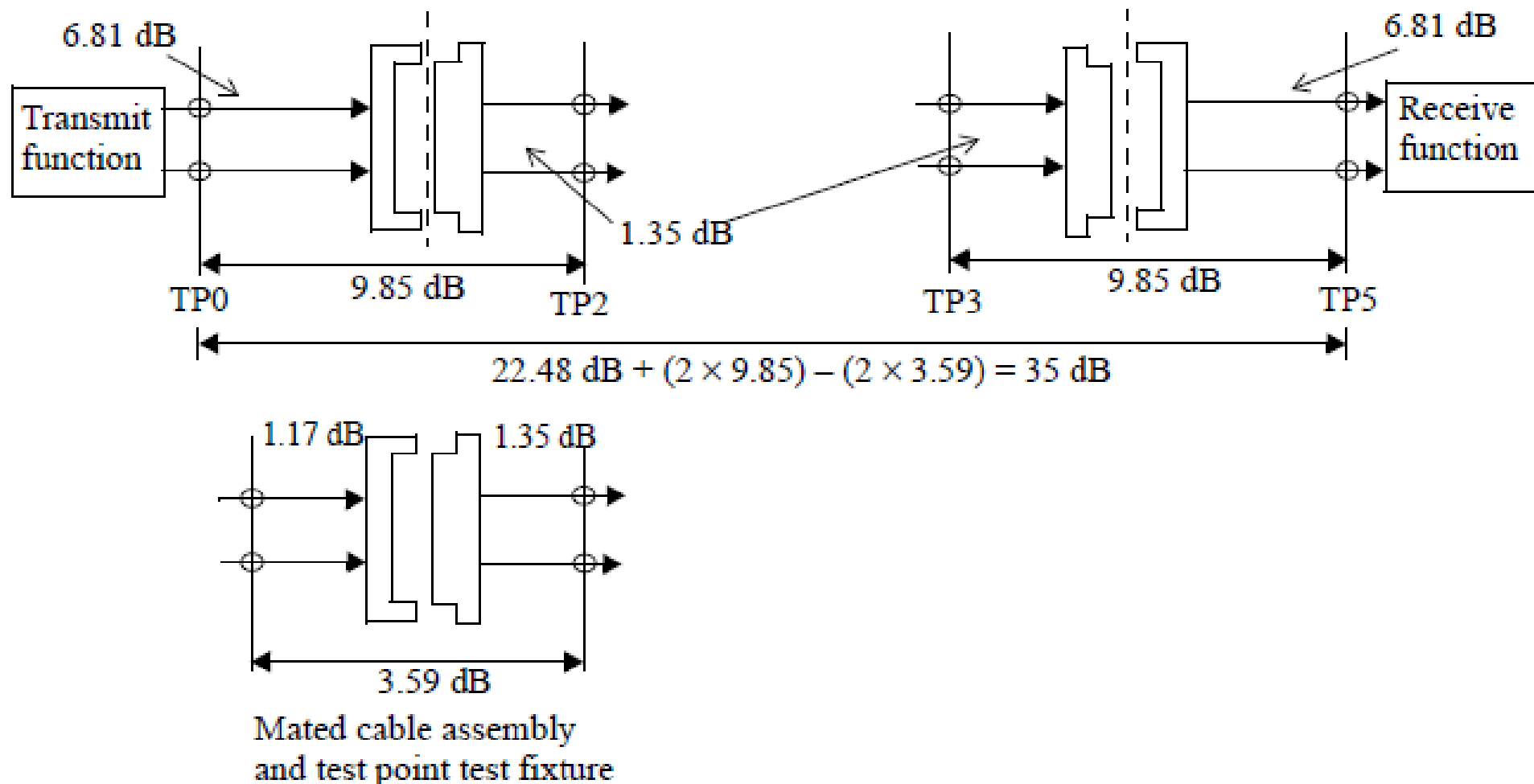
92A.5 Channel insertion loss

92A.6 Channel return loss

92A.7 Channel Operating Margin (COM)



# Channel characteristics – Mated Fixtures



NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

# 802.3bj 35 dB Channel IL @12.8906 GHz

Description	dB (@12.8906 GHz)
Host connector allocation	1.69
Host PCB	6.81
(TP2/TP3) HCB PCB	1.35
Total Host IL	9.85
CATF PCB	1.17
(TP2/TP3) HCB PCB	1.35
Host connector allocation	1.07
Total MTF	3.59
Bulk cable assumed	20.24
CATF PCB IL	1.17
Host connector allocation	1.07
Total Cable Assembly	22.48
802.3bj 35 dB channel IL@12.8906 GHz	35

802.3bj Channel      $22.48 + (2 \times 9.85) - (2 \times 3.59) = 35$  dB

# Technical Feasibility – 802.3bj

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- Systems with an aggregate bandwidth of greater than or equal to 100 Gb/s have been demonstrated and deployed in operational networks.
- The proposed project will build on the array of Ethernet component and system design experience, and the broad knowledge base of Ethernet network operation.
- Component vendors have presented data on the feasibility of the necessary components for this project. Proposals, which either leverage existing technologies or employ new technologies, have been provided.
- The reliability of Ethernet components and systems can be projected in the target environments with a high degree of confidence.

# Technical Feasibility – 802.3 25 Gb/s

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- Systems with an aggregate bandwidth of greater than or equal to 25 Gb/s (100 Gb/s) have been demonstrated and deployed in operational networks.
- The proposed project will build on the array of Ethernet component and system design experience, and the broad knowledge base of Ethernet network operation.
- Component vendors have presented data on the feasibility of the necessary components for this project. Proposals, which either leverage existing technologies or employ new technologies, have been provided.
- The reliability of Ethernet components and systems can be projected in the target environments with a high degree of confidence.



# Summary

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- Provided information related to developing the technical feasibility criteria for 802.3 25 Gb/s.
  - Proposal for 802.3 25 Gb/s Technical Feasibility
- 802.3 25G consistent with 802.3bj channel/system related specifications
  - Test points
  - Channel loss budget
  - Cable assembly specifications
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