Minutes 25Gb/s Ethernet Architecture ad-hoc meeting 8/12/14

Proposed agenda:

- IEEE patent policy reminder
  - http://www.ieee802.org/3/patent.html
- Approval of the Agenda
- Presentations:
  - project – Mark Nowell, Cisco
  - architecture – Matt Brown, APM
  - PCS/FEC – Mark Gustlin, Xilinx
  - FEC/latency – Adee Ran, Intel
  - copper cable channels and test fixtures – Chris Diminico, ???
- Discussion

Matt presented the agenda slides.
Matt reminded everyone of the IEEE patent policy (http://www.ieee802.org/3/patent.html).
Matt asked if anyone had any objection to the agenda as presented. There were no objections.

Presentations posted at:
http://www.ieee802.org/3/25GSG/public/adhoc/architecture/index.html

Mark Nowell – Project update
- reviewed slides
- draft language for objectives, CSD responses shared

Matt Brown – Architecture
- reviewed slides
- potential architectures and Sources of specifications that could be leveraged
- discussion on MDI – is this the SFP28 connector – single lane MDI

Mark Gustlin – PCS/FEC Architectures
- reviewed slides
- architectural options exist
- strong leverage and re-use from past clauses
- no issues substantiating technical feasibility

Adee Ran – FEC/latency
- reviewed slides
- raised options for minimizing latency

- discussed MTTFPA trap – turning off FEC to save latency – unknown MTTFPA impact
- suggested considering latency objective, MTTFPA objective. Feedback was that they may not be necessary and would be considered in TF regardless

Chris DiMinico – Copper Cable channels & fixtures

- reviewed slides
- Provided information related to developing the technical feasibility criteria for 802.3 25 Gb/s.
    - Proposal for establishing 802.3 25 Gb/s Technical Feasibility •
- Reuse of 802.3bj channel/system related specifications for 802.3 25 Gb/s
    - Test points
    - Channel loss budget
    - Cable assembly specifications
    - Test fixture specification
    - COMS

Discussion

- limited time for discussions after Chris' presentation
- request for presentation requests for next week to Matt by Friday

Attendees (from Webex attendance)

Ghani Abbas ghani.abbas@ericsson.com
Scott Feller scott.feller@cortina-systems.com
Vipul Bhatt vbhatt@inphi.com
Matt Brown mbrown@apm.com
Rita Horner rhorner@synopsys.com
Arthur Marris - Cadence arthurm@cadence.com
Andy Zambell andrew.zambell@fci.com
sam sambasivan sam_sambasivan@labs.att.com
Mark Pilip mpilip@ezchip.com
Frank Straka fms@panduit.com
Joel Goergen jgoergen@cisco.com
chris diminico cdiminico@ieee.org
Adee Ran adee.ran@intel.com
Megha Shanbhag megha.shanbhag@te.com
Steve Trowbridge steve.trowbridge@alcatel-lucent.com
Mark Nowell mnowell@cisco.com
Mark Gustlin mgustli@xilinx.com
rashid rashid@synopsys.com
Tom Brown tkbrown@vitesse.com
Piers piersd@mellanox.com
mike dudek mike.dudek@qlogic.com
Myles myles.kimmitt@emulex.com
Ingvar Froroth ingfro@marvell.com
Rich (Intel) richard.mellitz@intel.com
Erdem Matoglu erdem.matoglu@amphenol-tcs.com
Nathan Tracy ntracy@te.com
Vineet vineets@cisco.com
Marty martins@vitesse.com
Dave Brown dbrown@semtech.com
Peter Anslow panslow@ciena.com
Bob Wagner rwag@panduit.com
Jeffery Maki jmaki@juniper.net
Adam Healey adam.healey@avagotech.com
Paul Kolesar pkolesar@commscope.com
David Ofelt ofelt@juniper.net
Tony Zortea tony.zortea@pmcs.com
Ron Muir muirr@jae.com
john petrilla john.petrilla@avagotech.com
Derek Cassidy derek.cassidy@bt.com
Pirooz Tooyserkani pirooz@cisco.com
Beth Kochuparambil edonnay@cisco.com
Gary Nicholl gnicholl@cisco.com
Xinyuan Wang wangxinyuan@huaweri.com

David Chalupsky (Intel) david.chalupsky@intel.com
Shankar shhariha@cisco.com
Jeffery Maki jmaki@juniper.net
Shankar shhariha@cisco.com
Jacky Chang jacky.chang@hp.com
Shankar shhariha@cisco.com
Shankar shhariha@cisco.com