

OTN Support for 25GbE

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Recap – What is implied by “Appropriate Support for OTN”

- See presentation “[OTN Support – What is it and why is it important?](#)”
- Key elements:
 - Clarity that line code is not a playground for proprietary extensions, creating confidence in transcoding implementations if necessary to get the signal to fit (unlisted control block types shall not be transmitted and shall be considered an error if received)
 - Single PCS or OTN mapping reference point for mapping a given rate of Ethernet into OTN
 - Mapped Ethernet signal FITS into the expected capacity within an optical transport network
 - Ethernet Optics can be reused for OTN client interfaces at the same rate

Line code not a playground for proprietary extensions

- Assuming that 25GbE reuses clause 91 FEC (or something similar) with transcoding, 25GbE will have to restrict the control block types that are used so they don't break its own transcoding. No real danger that this won't be met. While clause 49 doesn't say explicitly that non-listed control block types can't be used and clause 82 does, the 25GbE PCS will need to specify that non-listed 66B control block type values shall not be transmitted and shall be considered an error if received

OTN Reference Point

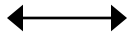
- There should be a point in the stack common to all 25GbE PMDs that can be used for the mapping format of 25GbE into OTN. The same PMD need not be used at the OTN ingress and egress.
- For 40GbE and 100GbE, this format is the serialized and deskewed PCS lanes with lane alignment markers without FEC (trans-decoded back to 64B/66B if necessary)
- If there are FEC and non-FEC 25G PMDs, the OTN-mapped format should be the same. If one has an alignment marker, they both should. Idle insertion/deletion shouldn't be required to convert between the FEC and non-FEC formats
- Note that 64B/66B with a marker and no FEC has exactly the same bit-rate as 256B/257B with a marker and RS(528,514) FEC, so this can be suitable for SYNC-E even if different PMD types are used at the OTN ingress and egress

Which PMDs require OTN mapping?

- Electrical PMDs normally wouldn't be terminated on an OTN box
- On the other hand, you shouldn't constrain or make too many assumptions about what people will build with the tinker-toys available
- Since the 25GbE architecture may support both FEC and non-FEC PMDs, architecturally it should be clear how each is handled mapping over OTN even if all non-FEC PMDs defined by P802.3by are electrical and unlikely to be mapped over OTN

Treatment of Ethernet FEC in an OTN environment

Ethernet FEC is designed to correct
all of the errors that may occur across this link

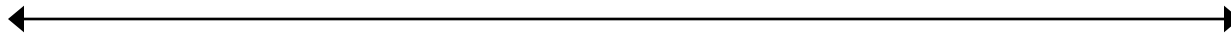


Enterprise
Ethernet
Switch

OTN
Operator A

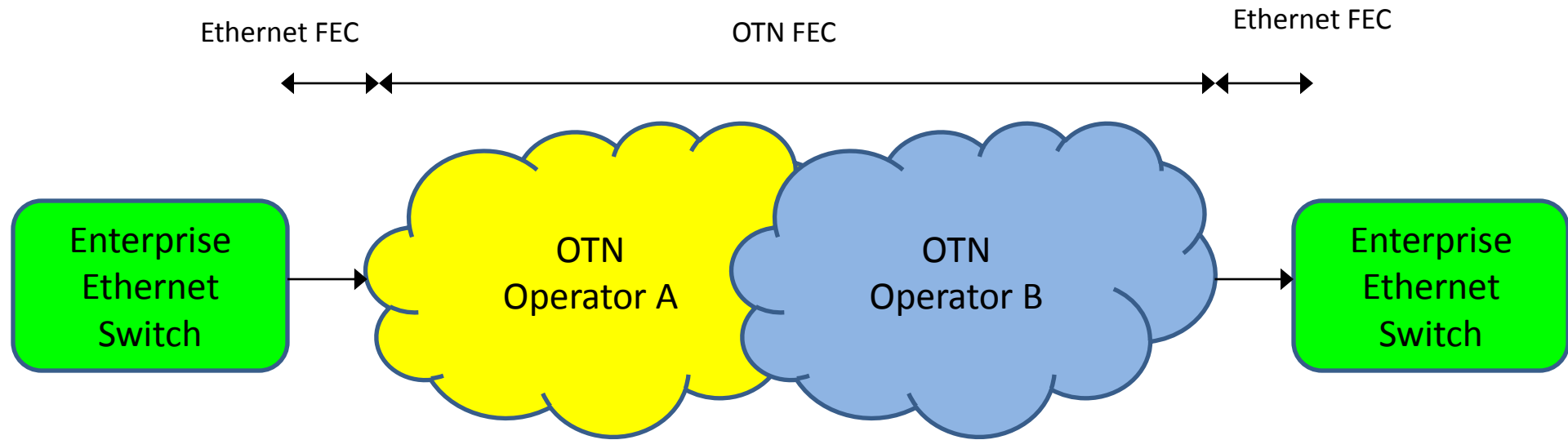
OTN
Operator B

Enterprise
Ethernet
Switch



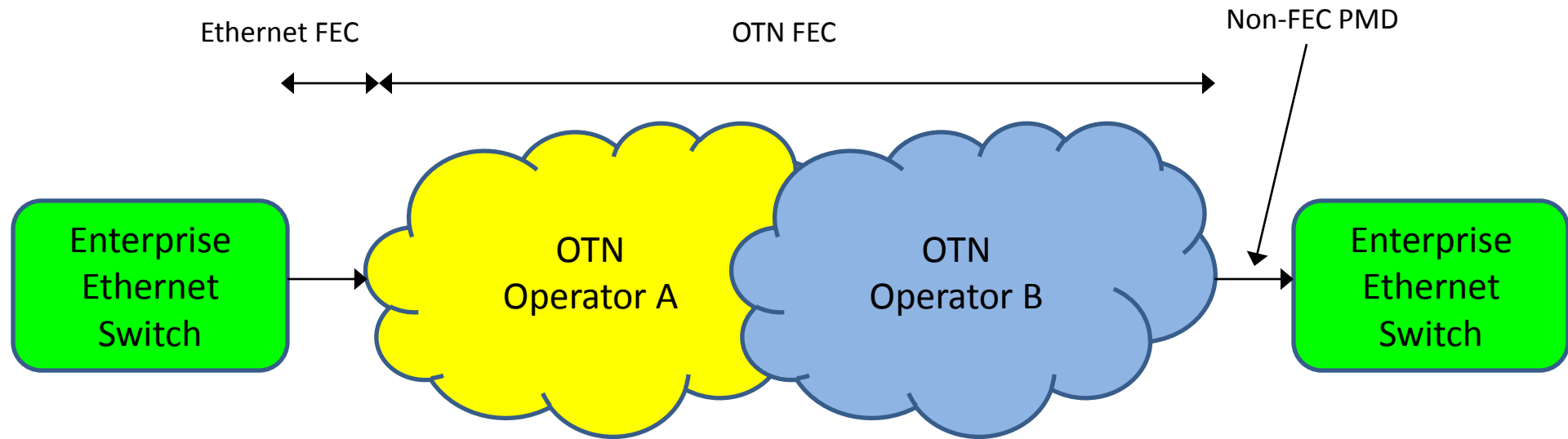
Ethernet FEC is NOT designed to correct
all of the errors that may occur across this link

Treatment of Ethernet FEC in an OTN environment - continued



Ethernet FEC must be terminated and regenerated separately for the ingress and egress link

Treatment of Ethernet FEC in an OTN environment - continued



Separating Ethernet FEC for the ingress and egress links allow mix/match of PMD types used at ingress and egress

Does the format fit the expected capacity in OTN networks?

- Mapping into 20 tributary slots of OPU4 or 21 tributary slots of OPU3 is straightforward as long as the encoded bit-rate of 25GbE without FEC does not exceed 26.033 Gb/s. Current proposals for what is likely to be mapped over OTN (64B/66B with or without a marker) have a bit-rate of 25.78125 Gb/s which does not exceed this limit
- 25GbE does not fit into 20 (of 32) tributary slots of OPU3 even if 256B/257B encoded. Not a significant issue since you can't fit two 25GbE into 40G
- It would be an issue if four 25GbE would not fit into OPU4

Reuse of 25G Ethernet interfaces for 25G OTN interfaces

- Not applicable, since there is no standardized 25G OTN physical interface

More thoughts on “alignment markers”

- What are called “Alignment Markers” (AMs) in the 802.3ba, 802.3bg, 802.3bj, and 802.3bm interfaces actually provide three functions:
 - Lane alignment for parallel interfaces (not applicable for P802.3by)
 - BIP error monitoring (may be applicable for P802.3by non-FEC interfaces, not useful for FEC interfaces due to the “cliff” behavior introduced by the FEC)
 - FEC block frame alignment (may be applicable for P802.3by FEC interfaces)
- It seems useful to have such a bit-pattern as part of P802.3by interfaces, although a different name than “alignment marker” could be used since the other two functions are the *raison d’être* for these bits in P802.3by and lane alignment is not a necessary function

THANKS!