

FEC and Architecture

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IEEE 802.3 400 Gb/s Ethernet Study Group

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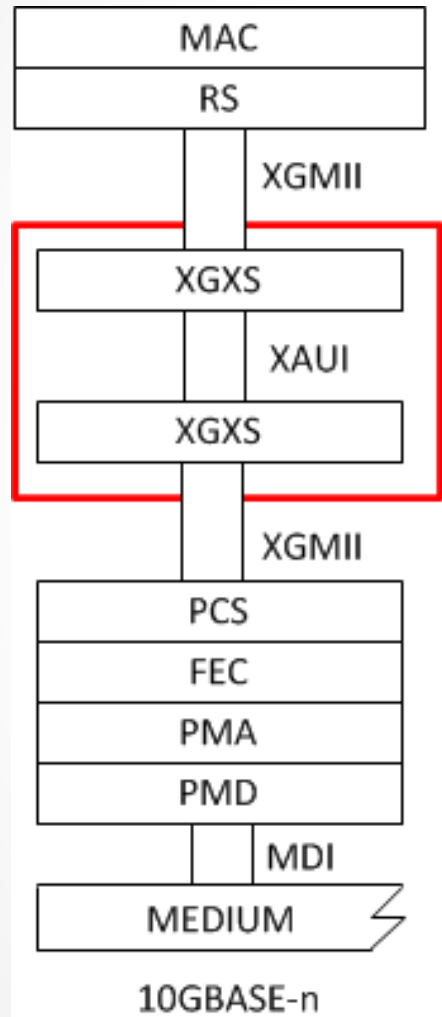
Supporters

- Hugh Barrass, Cisco
- Gary Nicholl, Cisco
- Mark Gustlin, Xilinx
- David Law, HP
- Adam Healey, LSI

Introduction

- **FEC has been discussed for**
 - **PMD support**
 - **CDAUI support**
- **This presentation starts initial exploration of architectural impact**

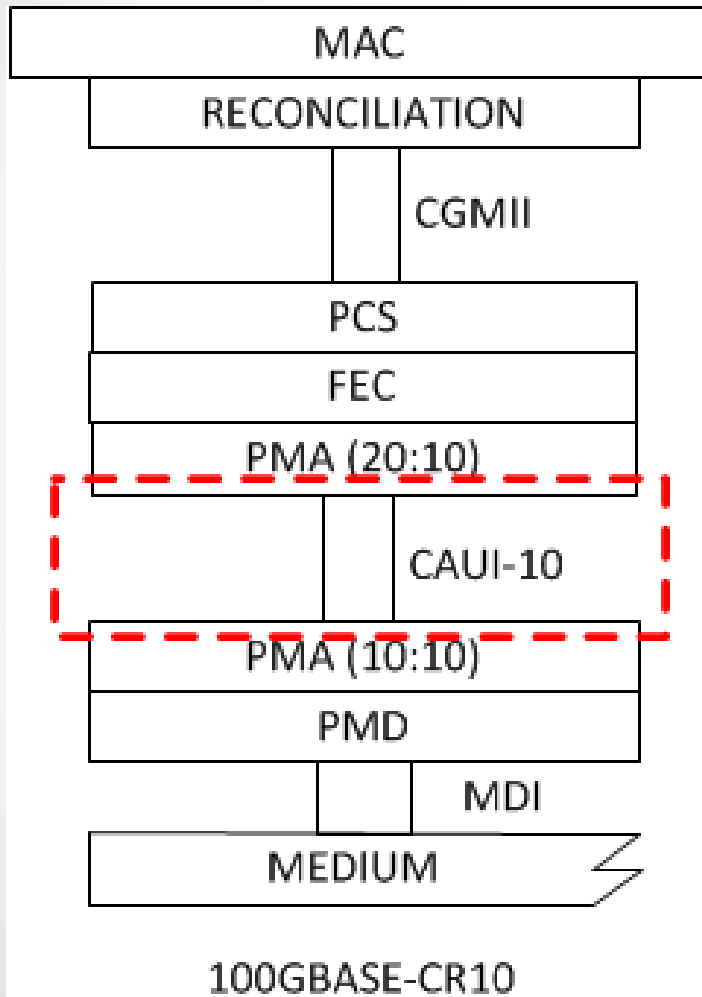
10 GbE Architecture



XGXS Sub-layer

- XGMII Extender contains XAUI
- 8B / 10B encoding / decoding
- Clock / data recovery in XGXS
- XGXS encoding does not match 10GBASE-R (64b/66b) PCS
- Added complexity
- Limited flexibility

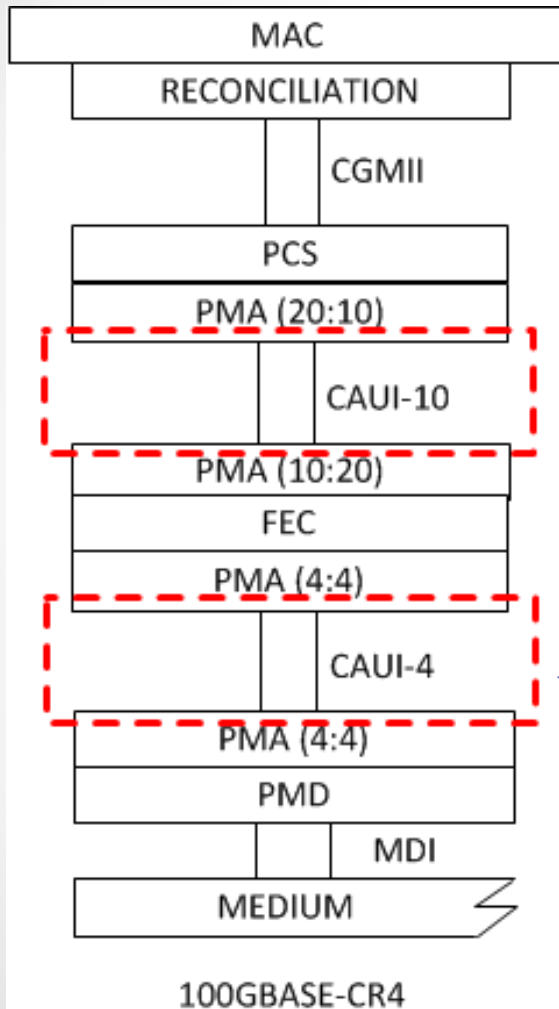
802.3ba 40 / 100 GbE Architecture



CAUI-10

- No extender sublayer
- No additional encoding
- Can move between sub-layers in PHY
- Increased flexibility
- Reduced complexity

100GBASE-CR4 Architecture



CAUI-10

- No extender sublayer
- No additional encoding
- Can only be between PCS and top FEC

FEC

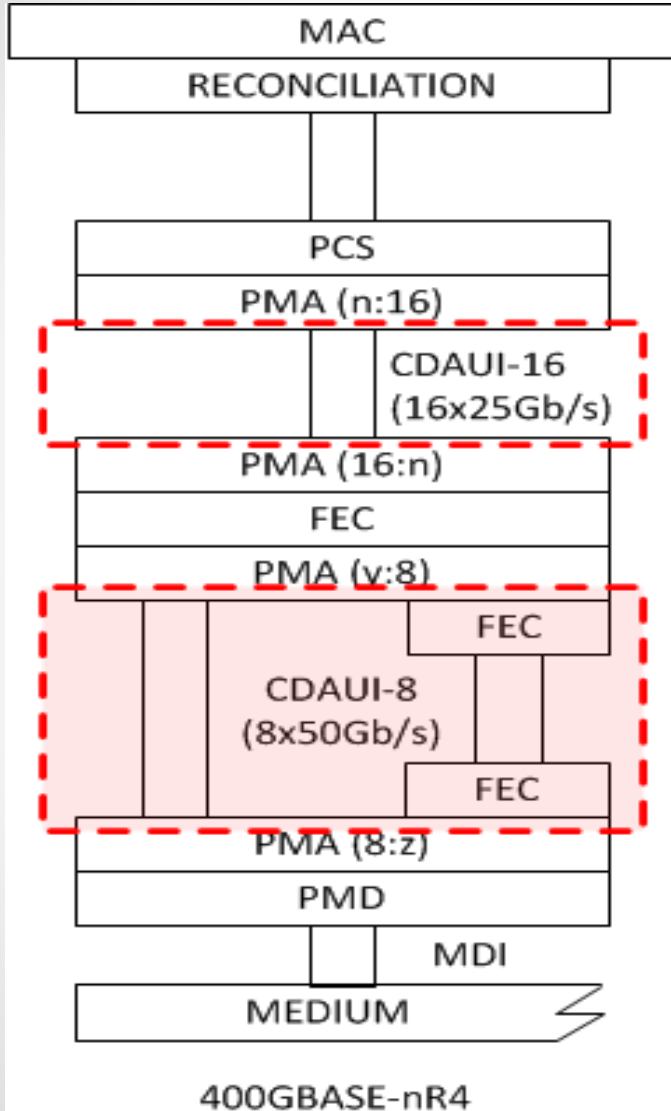
- Transcoding
- FEC encoding
- 4 lanes

CAUI-4

- No extender sublayer
- No additional encoding
- Can be between any sub-layers in PHY

- Added complexity / rules

For Discussion



CDAUI-16

- No extender sublayer
- No additional encoding
- Is FEC needed to meet interface channel requirements?
- Placement dependent on FEC

FEC

- TBD

CDAUI-8

- Will FEC be needed for this interface channel requirement?
- Do we need to reconsider an extender sub-layer concept?

Summary

- Reminder: This presentation is focused on highlighting questions to be asked, not providing answers!
- FEC for PMDs is being debated now
- FEC for a CDAUI could have architectural implementations that will need to be considered and thought through.
- Potential impact on EEE support may need to be addressed as well.
- Any FEC proposals will need to address
 - Specifics of FEC
 - Architectural issues
- We should strive to keep flexibility high and complexity low.